Transparent OLED Lighting Panel Design Using Two-Dimensional OLED Circuit Modeling

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In this work, we develop a simulation method to predict a two-dimensional luminance distribution method using a circuitry simulation. Based on the simulation results, we successfully fabricate large area (90 mm × 90 mm) transparent organic light-emitting diode panels with high luminance uniformity.

Keywords: Organic light-emitting diode (OLED), transparent, lighting, panel, simulation, design.

I. Introduction

Organic light-emitting diodes (OLEDs) are a promising light source for lighting applications. OLED lighting can offer distinct features, such as transparency, color tunability, and a high color rendering index [1]-[5]. In particular, transparent OLEDs (TOLEDs) have been actively investigated for large-size OLED displays, TOLED displays, and TOLED lighting [1], [2], [6]-[9]. A typical TOLED structure consists of a transparent anode composed of indium-tin-oxide (ITO), organic layers, and a transparent cathode. In TOLEDs, a transparent cathode with a LiF\Al\Ag structure is frequently used. However, the low transparency and high sheet resistance of a cathode limit their size and performance capability. Recent research activities have focused on an improvement of the transmittance and sheet resistance of a cathode [6]-[9]. The sheet resistance across the anode and cathode causes nonuniformity in the luminance distribution. To design high-quality large-area TOLED panels, the luminance distribution of the panels must be known. The luminance distribution in larger area panels is determined by the interplay between the current distribution of the anode and cathode, making it rather difficult to predict the distribution. Previous OLED simulations have mainly focused on the mathematical modeling of electrical characteristics of OLEDs [10]-[13] without showing the luminance distribution across the emitting surface. In this work, we use a two-dimensional circuitry simulation method to predict the luminance distribution in TOLEDs. The simulation results are successfully applied to predict the luminance distribution of a large area (90 mm × 90 mm) TOLED lighting panel.

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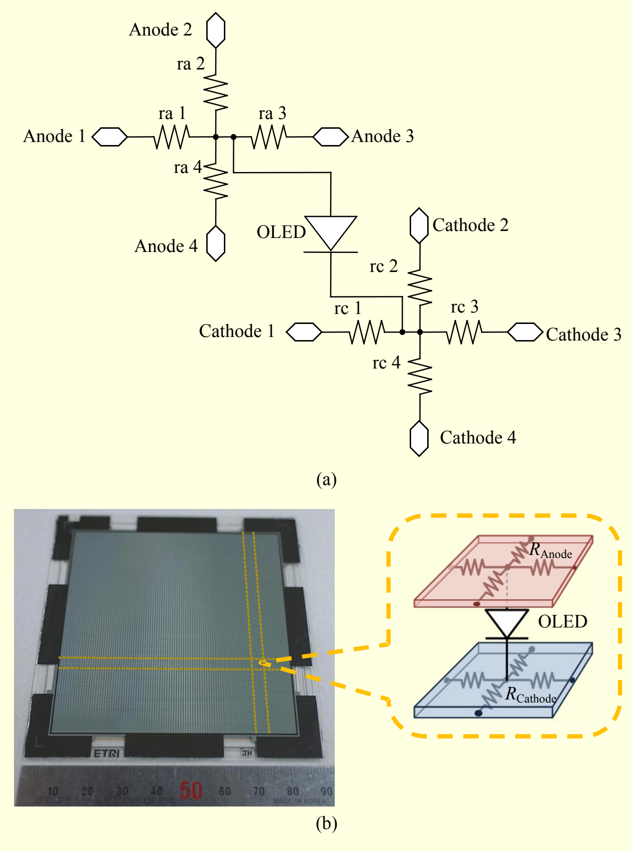
II. Modeling and Simulation

1. Two-Dimensional OLED Circuit Modeling

In this work, we aim to investigate the luminance uniformity of white TOLED lighting panels. We used a two-dimensional OLED circuit model, shown in Fig. 1, in conjunction with a circuit simulator, SMART-SPICE. The simulation cell is composed of connected resistive components distributed in a two-dimensional fashion. The crossed resistors represent unit area of the anode and cathode planes. Each node, Anodes 1 through 4 and Cathodes 1 through 4, is connected to an adjacent node of a nearby simulation cell. The input variable is the applied voltage, and the outputs are the current distributions and luminance in the simulation cell. The simulator uses a diode model, which mimics the electrical configuration of OLEDs. We use 100 cells and 1,171 resistor elements, including outer electrodes. Each resistor has half the value of the sheet resistance of the electrodes. In this scheme, the current distribution is obtained by calculating each diode's electrical response to the applied voltage. Because the current distribution is directly proportional to the emission uniformity, the luminance distribution of the given OLED panel can be deduced.



(a)

(b)

Fig. 1. (a) Schematic circuitry diagram and (b) its perspective view of two-dimensional OLED model.

2. Extracting Luminance from Current Density

In SMART-SPICE simulations, we do not obtain the luminance (*L*) distribution, but rather the current distribution. There is therefore a need to correlate the current density (*J*) to the luminance. To establish the *L*-*J* relation, we fabricate and measure the actual white OLEDs, which have an emission area of 2 mm × 2 mm. The white OLEDs have a stacking of a glass substrate (0.7 mm), an ITO anode (70 nm), organic layers (210 nm), and a LiF-Al cathode (100 nm). The current density-voltage-luminescence (*JVL*) characteristics are measured with a source/measure unit (Keithley 238) and a spectroradiometer (Minolta CS-2000). The *JVL* characteristics obtained from the OLED with an emission area of 2 mm × 2 mm are used as the starting data for obtaining the *L*-*J* relation. Figure 2 shows that it is possible to fit the current density accurately in the voltage range of interest. An electroluminescence curve fitting is performed in a voltage range of 0 V to 5.5 V at under 3,000 cd/m^2. During the fitting process, to avoid the complexity of physical SPICE modeling, we adopt an electrical curve fitting method to obtain the current density profile. In the next step, using the fitted *JV* characteristics, the *LV* characteristics are simulated. The simulated *LV* characteristics closely match the measured *LV* characteristics. The simulated *L* curve lies within an error range of 5% of the measured *L*. In our luminance range, the output luminance is found to be directly proportional to the output current. Based on these results, we draw a conclusion that our approach can be implemented to properly predict *L* by using the *JV* characteristics.

3. OLED Panel and Anode Design

Because the luminance distribution is determined by the electrical uniformity and sheet resistance of the cathode and

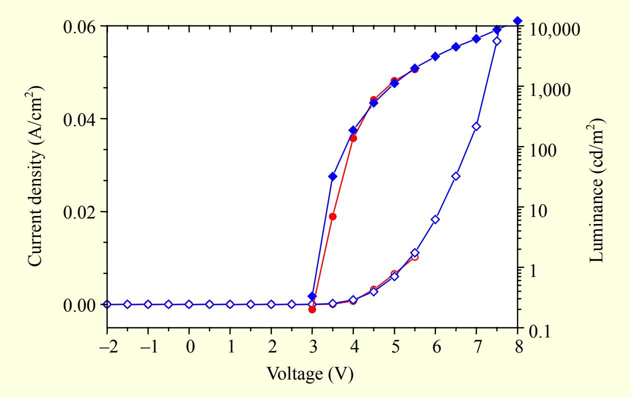


Fig. 2. OLED JVL characteristics and fitted electrical (open red) and simulated luminance (solid red) curves. Blue lines are measured values.

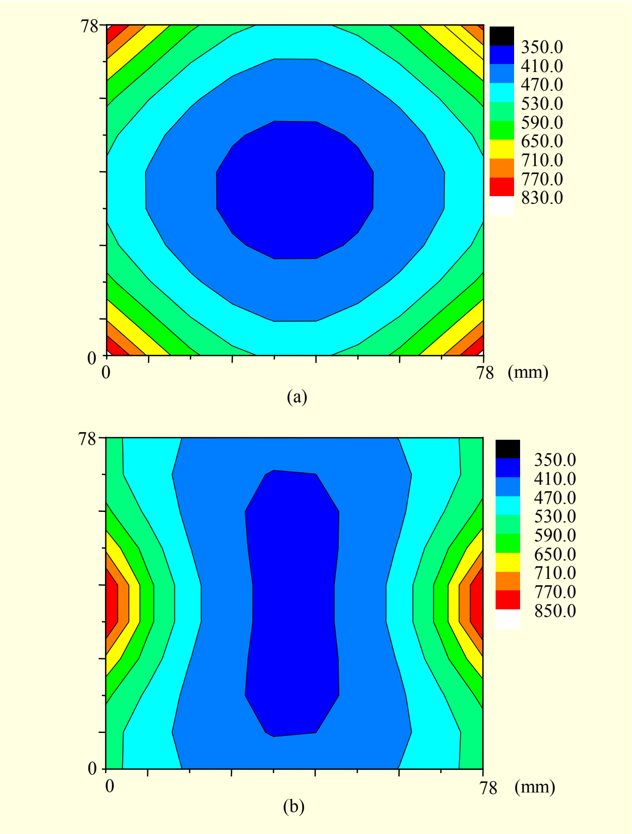


Fig. 3. Simulated luminance contour diagrams at each type of OLED external electrode: (a) four pairs of anodes and cathodes and (b) two pairs of anodes and cathodes.

anode, it is important to optimize both components. Subsections II.3 and II.4 are mainly concerned with this task. In this work, we choose an OLED panel of 90 mm × 90 mm, which has eight external electrodes on the edges for applying voltage.

Figure 3 shows two compositions of electrodes and their simulated luminance distributions. The first OLED tile, shown in Fig. 3(a), has two pairs of anodes and cathodes, in which electrodes of the same polarity are facing each other. Figure 3(b) shows an OLED tile that has a complex outline, composed of eight electrodes. Starting from a cathode at the corner, cathodes and anodes are positioned in an alternating fashion. This type of outline has a luminance distribution of an inverted dome shape. The distribution shown is uniformly symmetric with a low directional bias.

Owing to the sheet resistance of an ITO anode, the anode of a large area OLED panel requires electrical compensation. This can be achieved through the use of auxiliary metal layers, which leads to a marked improvement in luminance uniformity. The design parameters of the metal meshes are the width and spacing of the mesh lines and the fill factor. The sheet resistance and luminance uniformity are directly dependent upon these parameters. In this work, we consider a Mo/Al/Mo mesh configuration. Based on the resistivity calculations, we design a metal bus to have a thickness of 600 nm, a width of 26 μm, and a bus line spacing of 750 μm. This gives a fill factor of 95%.

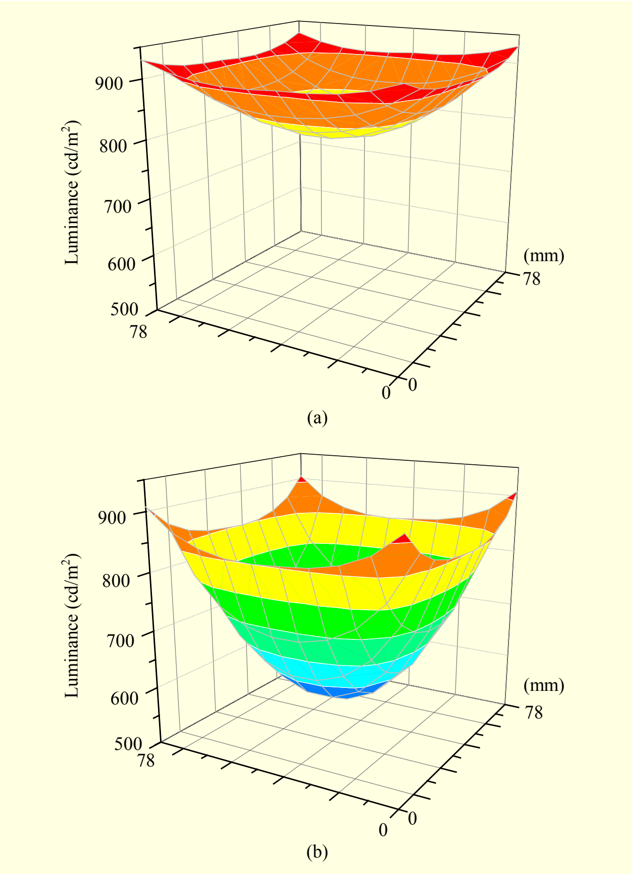


Fig. 4. Simulated two-dimensional luminance distribution diagram at each type of cathode with sheet resistance of (a) 1 Ω/sq and (b) 5 Ω/sq.

4. Cathode Electrode Design

The luminance distribution of a TOLED is strongly influenced by the sheet resistance of the transparent electrode. Obviously, from a transmittance perspective, it is desirable to have a thin transparent cathode. However, from an electrical perspective, because a high sheet resistance is expected, a thin cathode is not preferred. As a result, a highly transparent TOLED has a rather poor luminance distribution compared with conventional bottom emission OLED panels. Figure 4 compares the simulated bottom luminance distribution of two TOLED panels, which have different sheet resistances of 1 Ω/sq and 5 Ω/sq. In both cases, because the central region is the most remote from the electrode, the luminance distribution has an inverted dome shape. As the sheet resistance increases,

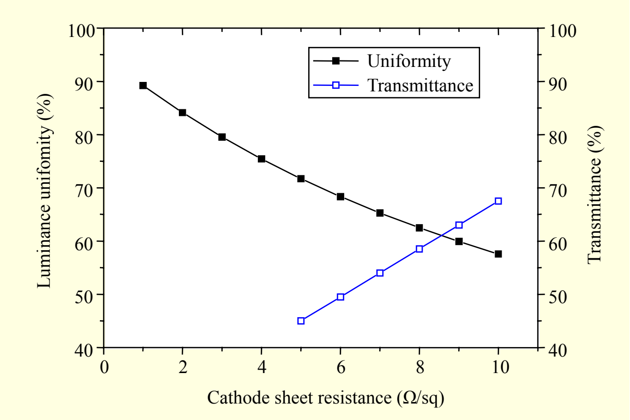


Fig. 5. Simulated luminance distribution uniformity and pseudo-transmittance of TOLED with cathode variation.

not only is the average luminance value lower but the distribution uniformity is also low, with a steeper rate of luminance decrease toward the central region. The overall uniformities of the 1-Ω/sq and 5-Ω/sq cathodes are 93% and 80%, respectively. The luminance uniformity (U_L) is obtained from the average luminance value ($L_{\text{Av.}}$) and standard deviation of luminance distribution, $L_{\text{S.D.}}$ ($U_L = [1 - L_{\text{S.D.}}/L_{\text{Av.}}] \times 100$).

To obtain uniformity as a function of sheet resistance, we perform simulations in the same manner shown in Fig. 4. As the sheet resistance increases, the uniformity deteriorates, as shown in Fig. 5. During electrical simulations, it is not possible to obtain an optical transmittance. We therefore used literature information to deduce the relationship between sheet resistance and optical transmittance [1], [2], [6]-[9]. As expected, the transmittance improves as the sheet resistance increases. Because there exists a tradeoff between electrical conductivity and optical transmittance, one must choose a cathode thickness that gives an acceptable luminance uniformity and transparency. Because the transmittance can be optically improved through the use of a capping layer (CL), we focus on the uniformity or cathode sheet resistance. To have a uniformity of higher than 70%, the sheet resistance must be lower than 6 Ω/sq, as shown in Fig. 5. Based on our previous work on TOLEDs, we choose a LiF/Al/Ag cathode (1 nm, 1.5 nm, and 15 nm, respectively), which has a measured sheet resistance of 5 Ω/sq [6].

III. Experiments and Simulations on Transparent OLED Lighting Panels

1. Fabrication of OLED Lighting Panels

Based on the optimized cathode and anode designs, we fabricate white OLED panels of 90 mm × 90 mm in external size and 78 mm × 78 mm in luminescence size. Each panel has eight external electrodes. Each panel is fabricated using the following configuration: a glass substrate (0.7 mm), an ITO anode (140 nm), organic layers (210 nm), a cathode (17.5 nm), and a CL (60 nm). The residue on the ITO surface is cleaned off using a standard oxygen plasma treatment. The ITO anode is furnished with an auxiliary metal mesh, as previously described in subsection II.3. The OLED grade materials are purchased and used without further purification. All organic layers are deposited in a high vacuum chamber below 6.6×10^{-5} Pa. Thin films of LiF, Al, and Ag are deposited as a cathode electrode. The CL is introduced to improve the transmittance for a given sheet resistance [6]. The capping layer has an optical function of inducing an interference effect in the OLED. The OLED panels are transferred directly from the vacuum into an inert environment glove box, in which they are encapsulated using a UV-curable epoxy and a glass cap with a moisture getter. Figure 6 shows an actual image of the fabricated TOLED and auxiliary metal meshes. The transparency is high enough to discern the letters on a business card.

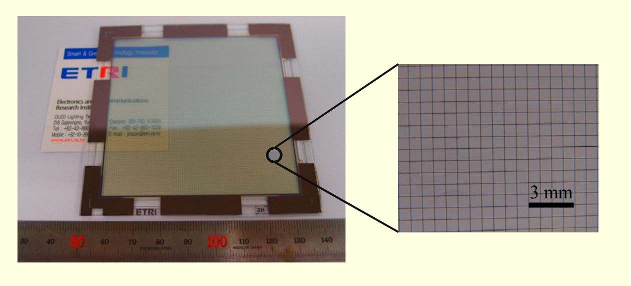


Fig. 6. Image of fabricated TOLED panel and auxiliary metal meshes.

2. Simulations versus Measurements

Figure 7 shows the simulated and measured luminance distribution in the TOLED panel shown in Fig. 6. The simulated distributions in Fig. 7(a) are remarkably similar to those shown in Fig. 4(b), but the distribution diagram is steeper.

The main difference between Fig. 7(a) and Fig. 4(b) is the simulation condition of the driving luminance. Figure 7(a) shows a simulated distribution under a high luminance condition, whereas Fig. 4(b) shows a simulated distribution under low luminance. Under a high luminance condition, an OLED requires higher current density than when under low luminance. Accordingly, the problem of having an IR drop is more severe in a high luminance condition, leading to a steeper distribution, as reflected in the diagram in Fig. 7(a). Generally, under a high luminance condition, the nonuniformity caused by an IR drop is more serious than the case under a low luminance condition. Figure 7(b) shows the measured

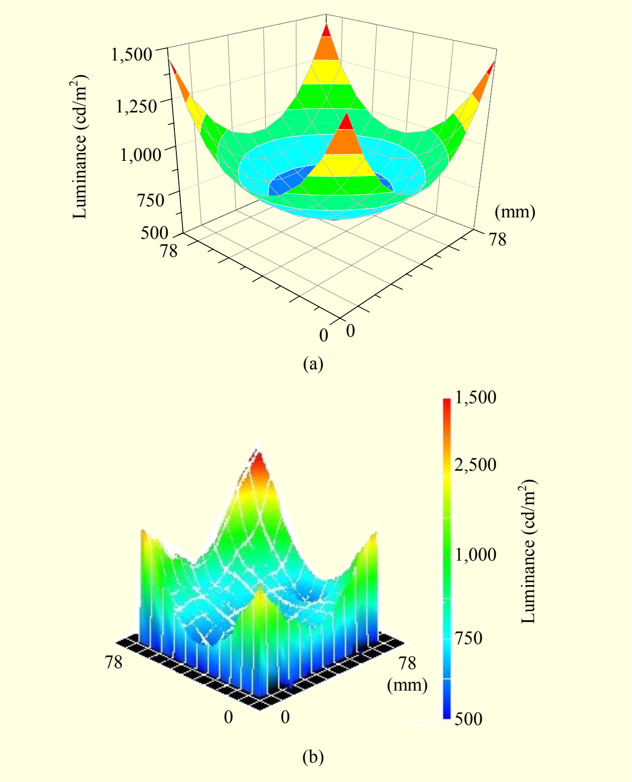


Fig. 7. (a) Two-dimensional simulation and (b) measurement results of transparent OLED lighting panel.

Fig. 8. Snapshot of transparent OLED lighting window.

luminance distribution of a TOLED panel. A voltage of 5.3 V is applied to the panels during both the simulation and measurement. The measured luminance distribution is in accordance with the simulated distribution. The luminance uniformities of the simulated and fabricated OLED panels are 78.6% and 79%, respectively.

Figure 8 shows TOLED tiles fabricated based on the simulation and optimization results. Clearly, the overall emission is very uniform. The results reflected in Figs. 7 and 8 show that our simulation method and electrode optimization approach are very useful in predicting the luminance distribution and uniformity of large-area TOLED panels.

IV. Conclusion

Predicting the overall uniformity of large-area OLED panels is very important. In this work, we developed an effective method to predict the luminance distribution of OLED panels. To be specific, by combining a two-dimensional OLED circuit model and a SMART-SPICE simulator, the current density distributions across an OLED panel of 90 mm × 90 mm were obtained. Using the luminance-current density relationship, the luminance distribution was obtained. In this study, we suggested and demonstrated a practical method for establishing the luminance-current density relationship. The usefulness of our method was verified using TOLED lighting panels with external electrodes. Our work suggests a new approach that can be applied to predict and design large-area OLED panels.

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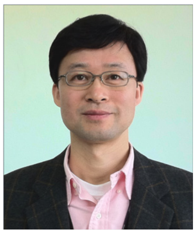

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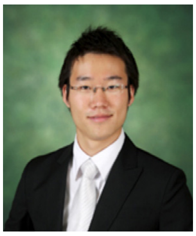

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