Electrical Characteristics of Triple-Gate RSO Power MOSFET (TGRMOS) with Various Gate Configurations and Bias Conditions

Kyoung Il Na, Jongil Won, Jin-Gun Koo, Sang Gi Kim, Jongdae Kim, Yil Suk Yang, and Jin Ho Lee

In this paper, we propose a triple-gate trench power MOSFET (TGRMOS) that is made through a modified RESURF stepped oxide (RSO) process, that is, the nitride_RSO process. The electrical characteristics of TGRMOSs, such as the blocking voltage (BV_{DS}) and on-state current ($I_{D,MAX}$), are strongly dependent on the gate configuration and its bias condition. In the nitride_RSO process, the thick single insulation layer (SiO_2) of a conventional RSO power MOSFET is changed to a multilayered insulator (SiO_2/SiN_x/TEOS). The inserted SiN_x layer can create the selective etching of the TEOS layer between the gate oxide and poly-Si layers. After additional oxidation and the poly-Si filling processes, the gates are automatically separated into three parts. Moreover, to confirm the variation in the electrical properties of TGRMOSs, such as BV_{DS} and $I_{D,MAX}$, simulation studies are performed on the function of the gate configurations and their bias conditions. BV_{DS} and $I_{D,MAX}$ are controlled from 87 V to 152 V and from 0.14 mA to 0.24 mA at a 15-V gate voltage. This $I_{D,MAX}$ variation indicates the specific on-resistance modulation.

Keywords: Superjunction (SJ), RSO process, TDMOS, power MOSFET, multigate.

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I. Introduction

Applying superjunction (SJ) concepts to a power device is the most promising way to overcome the tradeoff between the blocking voltage (BV_{DS}) and the specific on-resistance ($R_{ON,SPEC}$) [1]-[7], which indicates a breakthrough of the "silicon limit" for discrete power devices with inherent characteristics, such as a low $R_{ON,SPEC}$ and high-speed switching. SJ power MOSFETs are generally fabricated using a charge compensation [1]-[5] or vertical field plate method [6]-[8]. Ideally, the charge compensation method is applied using alternatively-stacked p and n layers with multi-implantation/epitaxial growth or deep etching/epitaxial growth [3]-[5] technologies without a charge imbalance issue. A vertical field plate is fabricated using the local oxidation of silicon (LOCOS) vertically or RESURF stepped oxide (RSO) processes. In particular, trench power MOSFETs created using LOCOS or RSO can have two gate regions (a "control gate" and "split gate" in the channel and drift regions, respectively) through an intentional modification of the fabrication process. The electrical characteristics of these devices, such as BV_{DS}, $R_{ON,SPEC}$, and gate charge (Q_{gd}), are strongly dependent on the split gate bias condition [9], [10].

In this paper, we propose the use of a triple-gate RSO MOSFET (TGRMOS) generated using a modified RSO process and investigate the variation of electrical properties based on the configuration of three separated gates and their bias conditions.

II. Device Fabrication and Gate Configuration

To make the RSO-type SJ power MOSFET with three gate

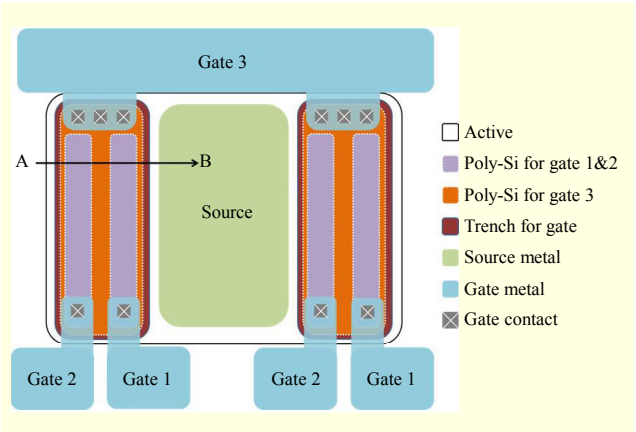

Fig. 1. Schematic of top layout for fabrication of TGRMOS.

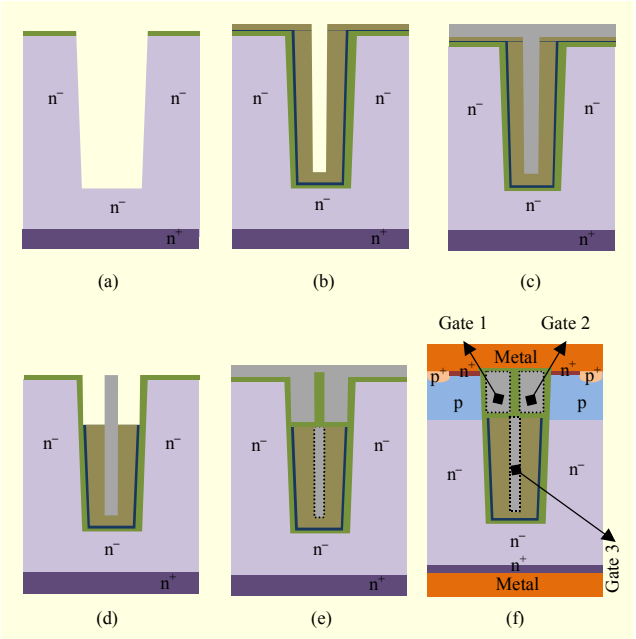

Fig. 2. Diagrams of TGRMOS process flows: (a) trench etch, (b) SiO_2/SiN_x/TEOS deposition, (c) first poly-Si filling, (d) poly-Si and TEOS etch-back to channel length, (e) thermal oxidation to gates' separation and second poly-Si deposition, and (f) implantation and metallization.

electrodes, we use the nitride_RSO process [11], which allows the thick single insulation layer (SiO_2) of a conventional RSO power MOSFET to be converted to a multilayered insulator (SiO_2/SiN_x/TEOS). This conversion allows us to easily control the thickness of the insulation layer, since the insertion of SiN_x film during the nitride_RSO process has an advantage in terms of the etching selectivity between the SiO_2 and SiN_x layers. Figure 1 shows the top layout of the TGRMOS unit cell with the three gate parts in one trench region. The process flows proposed to fabricate the TGRMOS are shown in Fig. 2. First, a deep trench is formed using a reactive ion etching process

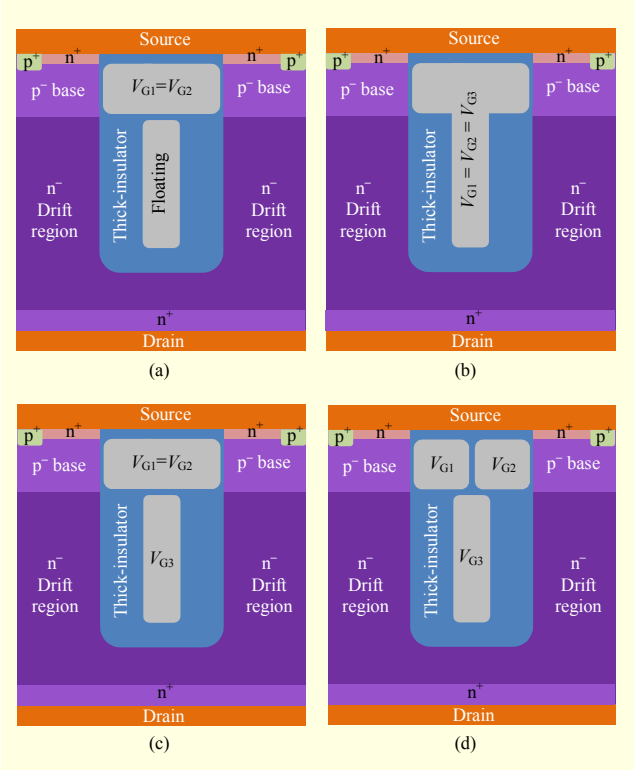

Fig. 3. Schematic cross-sectional views of TGRMOS with gate bias configuration: (a) S&FG_mode, (b) SG_mode, (c) DG_mode, and (d) TG_mode.

(Fig. 2(a)). The SiO_2/SiN_x/TEOS layers are then deposited (Fig. 2(b)). The electrical properties of TGRMOS are strongly dependent on the final thickness of the SiO_2/SiN_x/TEOS layers. The initially doped void-free poly-Si is filled using low pressure chemical vapor deposition (Fig. 2(c)). The poly-Si is etched to open the TEOS layer, and the etching rate of the TEOS layer is delicately controlled because the final channel length is defined by this step (Fig. 2(d)). The thermal oxidation process is then performed to separate the three gate regions. Next, the second doped poly-Si is deposited again (Fig. 2(e)). Finally, such fabrication processes as channel implantation, drive-in, source and p+ region definition, wafer thinning, and metallization are performed (Fig. 2(f)).

Figure 3 shows the four gate bias configurations of TGRMOS. Figure 3(a) shows the single-gate mode with a floating gate (called "S&FG_mode"), that is, $V_{G1} = V_{G2}$ and V_{G3} = floating. Figure 3(b) shows the single-gate mode (called "SG_mode") $V_{G1} = V_{G2} = V_{G3}$, which is the same as that of a conventional RSO MOSFET [6]-[8]. Figure 3(c) shows the double-gate mode (called "DG_mode"), as V_{G3} is separated from the V_{G1}=V_{G2} common bias, which is the same as that of the split gate RSO MOSFET [9]-[10]. Finally, the triple-gate mode (called "TG_mode") configuration is shown in Fig. 3(d). Tree gates can be operated independently.

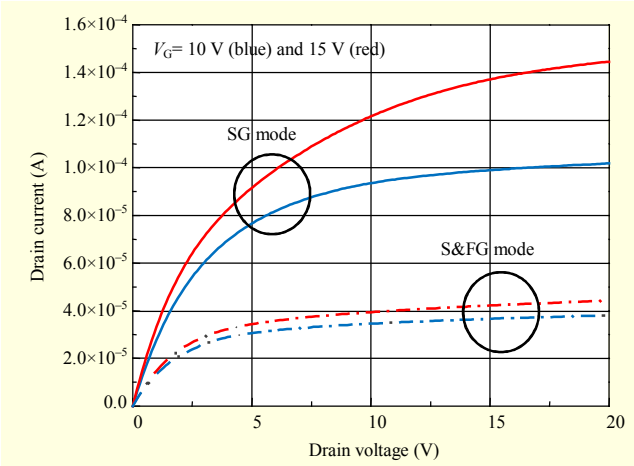

Fig. 4. Drain current vs. drain voltage properties between S&FG_mode and SG_mode in TGRMOS.

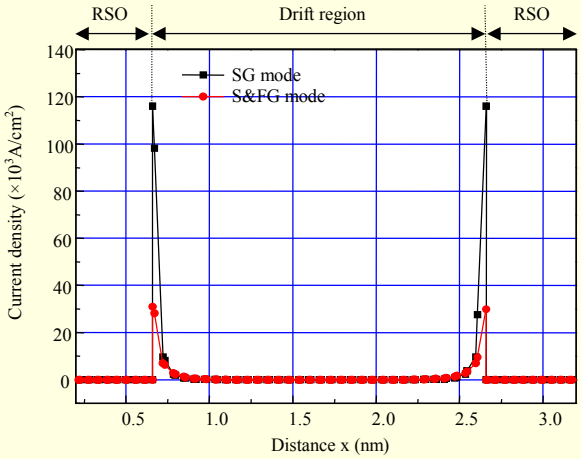

Fig. 5. Current density of TGRMOS with SG_mode and S&FG_mode operation.

III. Simulation Results of TGRMOS Operation

1. Single-Gate Mode vs. Single- and Floating-Gate Mode

To compare the electrical characteristics of the S&FG _mode operations in TGRMOS to those of the SG_mode operations in TGRMOS, the BV_{DS}, threshold voltage (V_{TH}), and I_D (V_D) are investigated using a Silvaco TCAD simulator based on an 8-μm/0.8-Ω·cm epitaxially grown substrate. The properties of V_{TH} and BV_{DS} in the S&FG_mode and the SG_mode in TGRMOS are similar, and their values are about 3.5 V and 118 V, respectively. However, the drain-current drivability is different in the two modes, as shown in Fig. 4. At V_G = 15 V and V_D = 20 V, the drain-current level of the S&FG_mode and the SG_mode is about 4×10^{-5} A and 1.4×10^{-4} A per unit cell pitch, respectively, which is a 3.5-fold improvement achieved during the SG_mode operation. In the SG_mode in TGRMOS, several electrons are accumulated along the RSO region during an on-state, owing to the highly positive bias supplied in the deep trench region. These electron accumulations with the x-direction cutline in the RSO region are the cause of the increasing current density in the RSO and drift interface region, as shown in Fig. 5. However, in the S&FG_mode, the electron accumulation is relatively decreased by the floating gate.

2. Double-Gate Mode

For the case of the DG_mode bias condition, the potential distributions of the TGRMOS in the drift region with various V_{G3} bias conditions are shown in Fig. 6. When the drain bias is changed from 0 V to BV_{DS}, V_{G3} is maintained at 0 V, 40 V, and –40 V, and V_{G1} and V_{G2} are connected to the ground. In the case of V_{G3} = 0 V, as shown in Fig. 6(a), the potential lines are pushed toward the substrate, resulting in a highly electrical

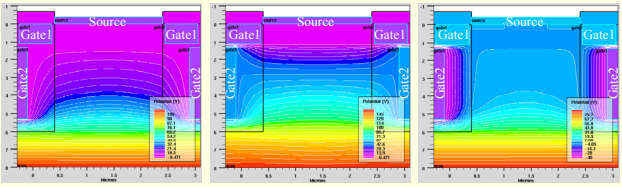

Fig. 6. At blocking mode, potential distribution in drift region of DG_mode TGRMOS with various V_{G3} bias conditions: (a) $V_{G1} = V_{G2} = V_{G3} = V_S = 0$ V (BV_{DS}=116 V), (b) $V_{G1} = V_{G2} = V_S = 0$ V and V_{G3} = 40 V (BV_{DS} = 152 V), and (c) $V_{G1} = V_{G2} = V_S = 0$ V and V_{G3} = –40 V (BV_{DS} = 87 V).

field focused at the trench bottom (BV_{DS} = 116 V). As V_{G3} is applied with a highly positive bias (V_{G3} = 40 V), the potential is focused at the trench bottom and the drift junction, as shown in Fig. 6(b). This effect improves the BV_{DS} property to 152 V, owing to an increase in the vertical field effect along the RSO region. On the contrary, Fig. 6(c) shows that as a negative bias is supplied at V_{G3} (V_{G3} = –40 V), the potential lines at the trench bottom region are more concentrated than in the V_{G3} = 0 V or V_{G3} = 40 V condition, which indicates the lowering of BV_{DS} (BV_{DS} = 87 V).

Figure 7 shows that the drain current drivability of the TGRMOS strongly depends on the V_{G3} bias condition. At this time, V_{G1} and V_{G2} are supplied 15 V. In the cases of V_{G3} = 0 V, 40 V, and –40 V, the drain currents are about 4.0×10^{-5} A, 2.4×10^{-4} A, and 2.0×10^{-13} A, respectively. This large difference from the V_{G3} bias condition can be explained by the electron concentration in the drift region, as shown in Fig. 8. In the case of V_{G3} = –40 V, the electron concentration in the drift region has a convex shape, and its level is too low compared to the other conditions, which means a lower drain current. In the case of V_{G3} = 0 V, however, the electron concentration is not

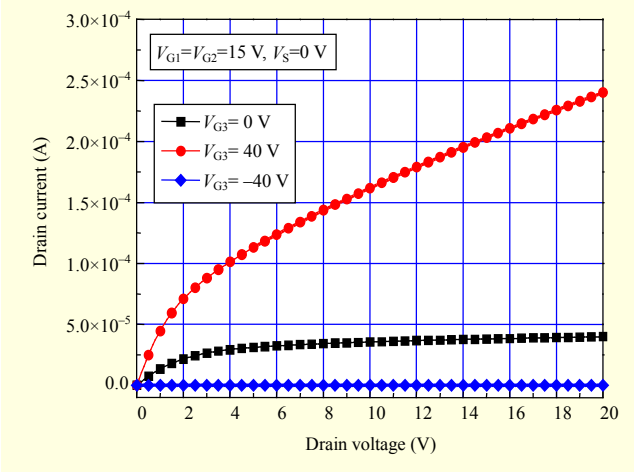

Fig. 7. Drain current vs. drain voltage of TGRMOS with various V_{G3} bias conditions in DG_mode. V_{G1} and V_{G2} are supplied 15 V.

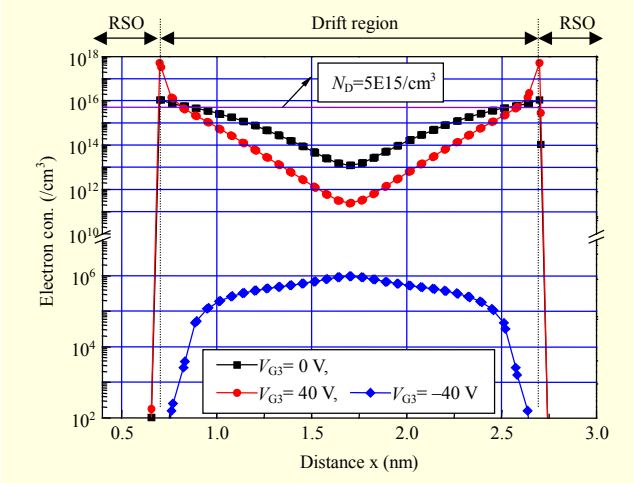

Fig. 8. Electron concentration of TGRMOS in drift region with various V_{G3} bias conditions and V_{G1} = V_{G2} = 15 V.

limited by a strong negative bias. A large portion of the electron concentration is located in the central drift region. The electrons flow through the overall drift region. When V_{G3} is 40 V, an approximately tenfold electron concentration is also accumulated at the RSO and drift interface region. This phenomenon becomes the main evidence of an improvement in the drain current. In contrast, the electron concentration in the central region of the device decreases relatively.

3. Triple-Gate Mode

In the TGRMOS, the V_{G1} and V_{G2} are independently operated, which means that the negative bias can be intentionally supplied at V_{G1} or V_{G2}. The hole current at this configuration can be effectively controlled using a negative

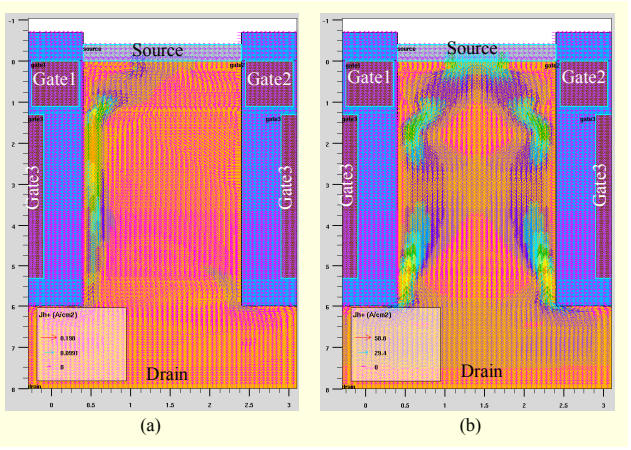

Fig. 9. Hole current density in device on-state: (a) DG_mode and (b) TG_mode with negative bias.

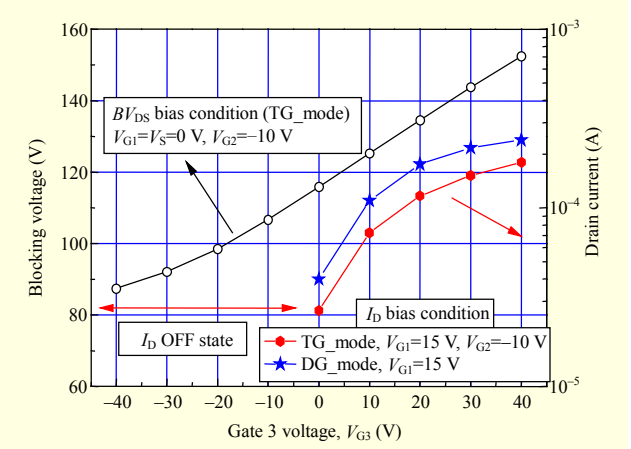

Fig. 10. BV_{DS} and $I_{D,MAX}$ properties in TGRMOS with TG_mode and DG_mode under various V_{G3} bias conditions.

bias, as shown in Fig. 9. In spite of this bias condition, the BV_{DS} is still maintained at a similar level compared to the DG_mode, as shown in Fig. 10. However, the drain current is decreased by about 50% compared with the DG_mode operation because only one side-channel is turned on. For an improvement of the switch properties of the power device, these results show that the generated electron and hole pairs from the thermal and impact ionization effects can be quickly exhausted to the drain and P^+ region through separate paths.

IV. Conclusion

We proposed a triple-gate vertical power MOSFET (TGRMOS) that is made through a modified RSO process. This device can be operated in various operation modes, such as single- and floating-gate mode (S&FG_mode), single-gate mode (SG_mode), double-gate mode (DG_mode), and triple-gate mode (TG_mode). BV_{DS} and $I_{D,MAX}$ are strongly

dependent on the gate configurations and their operation voltages, owing to a modulation of the electric potential in the drift region. The simulation results show that the maximum value of BV_{DS} and $I_{D,MAX}$ are attained in the DG_mode and TG_mode operations as V_{G3} is applied to 40 V. In the case of the TG_mode operation, in particular, the hole and electron paths can be separated when V_{G1} or V_{G2} electrodes supply a negative bias.

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