A Power-Efficient CMOS Adaptive Biasing Operational Transconductance Amplifier

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This paper presents a two-stage power-efficient class-AB operational transconductance amplifier (OTA) based on an adaptive biasing circuit suited to low-power dissipation and low-voltage operation. The OTA shows significant improvements in driving capability and power dissipation owing to the novel adaptive biasing circuit. The OTA dissipates only 0.4 μW from a supply voltage of ±0.6 V and exhibits excellent high driving, which results in a slew rate improvement of more than 250 times that of the conventional class-AB amplifier. The design is fabricated using 0.18-μm CMOS technology.

Keywords: Adaptive biasing, CMOS operational transconductance amplifier (OTA), class-AB amplifiers, low power, low voltage.

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I. Introduction

The operational transconductance amplifier (OTA) is the most widely used type of amplifier in analog and switching (sampled-data) applications. To achieve high driving capability and fast settling, much power is consumed. Although the basic class-AB amplifier gives a better tradeoff between power and slew rate, the driving capability of the amplifier is reduced by decreasing both supply voltage and input bias current to decrease short channel and power dissipation effects [1]. This problem is a critical issue for implementing an amplifier with high driving capability and with very low standby power dissipation. There are several modified class-AB amplifiers that have been presented to achieve the mentioned approaches [2]-[10]. However, most of them require an additional current circuitry based on conventional current mirrors to boost the tail current dynamically when a large differential input voltage is applied [2]-[5].

This current source circuit suffers from mismatched effects due to process variations resulting in limited output current that lacks control. Although an increase in the ratio of output transistors of the class-AB stage is often a possible way to overcome the slew rate limitations [3]-[5]; this increase affects both the power dissipation and active area of the OTA and often results in extra stray capacitances connected to the output nodes, which degrade the frequency response. The topologies presented in [2] use the two additional current sources based on the basic current mirrors by which currents can be dynamically increased if a large differential voltage is applied to the input terminals of the OTAs. The positive feedback loop increases the tail current and improves the driving capability. These current sources also generate extensive distortion for small input signals. Since positive feedback loop gain is limited by

mismatched effects, more distortion is created than when using an amplifier without an adaptive biasing circuit. The other topologies [6]-[8] need more than two additional MOS amplifier stages and higher quiescent current, which results in increased power dissipation and requires more silicon area.

In this work, a new class-AB amplifier using an adaptive biasing circuit, which eliminates the drawbacks previously specified, is proposed. Analysis and experiment results show that reducing the mismatched effects of the positive feedback loop of the amplifiers presented in [2] increases the output current and decreases the distortion of small input signals efficiently [9], [10]. Furthermore, the symmetric switching behavior of the new current sources at transients is verified. This causes the amplifier to be very sensitive in the adaptive biasing operation due to the reduction in mismatched effects and increment in the positive feedback loop factor, even when a small-signal differential input voltage is applied and the bias current is very small. The sensitivity becomes a critical necessity when the amplifier is used to drive biological applications in which the amplitude of the input signals is typically in the range of 1 μV to 100 mV [11].

Additionally, reducing the distortion of small input signals leads to improved small-signal characteristics, such as CMRR, PSRR, and so on. To enhance these characteristics, the circuit will suffer from mismatched offset, noise, area, and power due to using additional circuitry.

The rest of the paper is organized as follows. The principle circuit configuration is described in section II. Section III shows small-signal behaviors of the amplifier. Section IV presents the analysis of the simulation and measurement results. Finally, the conclusions of this work are drawn in section V.

II. Design Principles

1. Conventional OTA

Figure 1 shows the structure of the conventional amplifier. The slew rate is indicated in (1) [3].

$$SR = K\frac{I_B}{C_L}. \quad (1)$$

Here, K is the current mirror ratio, C_L is the capacitive load, and I_B is the quiescent bias current. A possible way to enhance the slew rate to achieve fast settling time characteristics is to increase the power consumption (increase in K and I_B). In other words, to enhance driving capability, the K and the quiescent bias current should be increased. An increase in K not only results in larger parasitic capacitances being added at the output stage, which degrades the response frequency, but results in increased power dissipation.

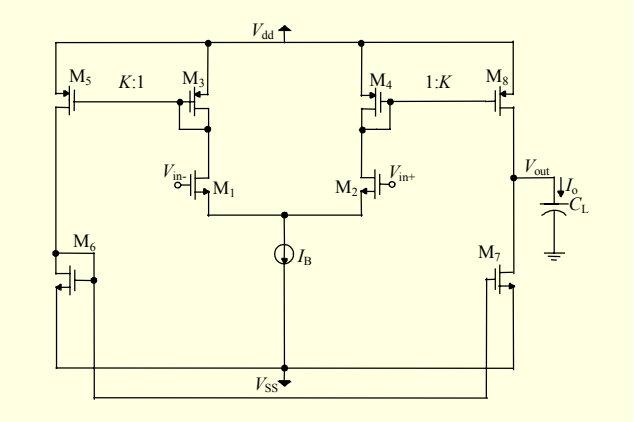

Fig. 1. Conventional OTA.

The slew rate can be enhanced and the driving capability of the amplifier can be increased through adaptive biasing circuits [2]-[5]. These topologies can boost the tail current dynamically if a large differential input voltage is applied. The main problem of these topologies is that the driving capability of the amplifiers is usually determined by increasing the ratio of the output transistors, which degrades their stability and requires extra power and silicon. Also, when the amplifiers are biased in weak inversion or moderate inversion regions, these structures cause a considerable amount of distortion for small input signals because of mismatched effects. Therefore, it is difficult to achieve an OTA with high driving capability and low power dissipation. In the following section, a method to possibly achieve the desired circuit performance is described in detail.

2. Current Source Circuits

As mentioned above, a current source circuit that provides an additional current dynamically for the tail current to enhance the slew rate plays the leading role in optimizing the performance and managing the power dissipation of an amplifier. The design in this work is structured to solve the aforementioned issues.

Figure 2 shows a current source circuit in which ML1, ML2, ML3, and ML4 transistors make up a translinear loop (TL) topology. Thus, by using Kirchhoff's voltage law, (2) can be derived.

$$V_{GSL1} + V_{GSL2} = V_{GSL3} + V_{GSL4}. \quad (2)$$

Since the currents of the ML1 and ML3 transistors are equal, the currents of the ML2 and ML4 transistors are identical. If $I_1 < I_2$ or $I_1 = I_2$, the current source does not provide any current, as shown in Fig. 3. The current source shown in Fig. 2 executes the operation of $A(I_1-I_2)$ only if $I_1 > I_2$, where A is the aspect ratio of the ML5 and ML6 transistors.

Figure 3 shows the output current of ML3 versus the ratio of

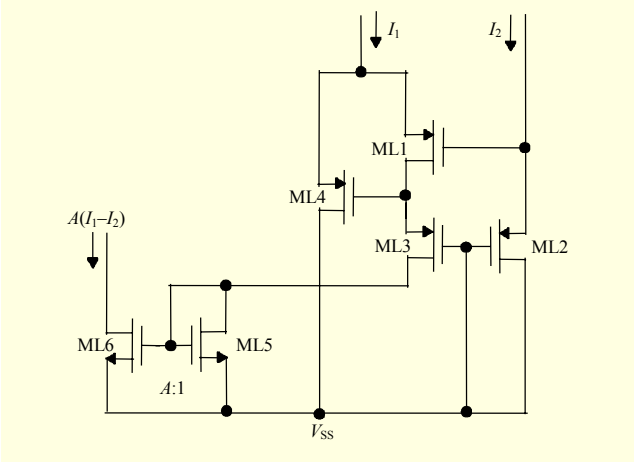

Fig. 2. Current source circuit realizing $A(I_1–I_2)$.

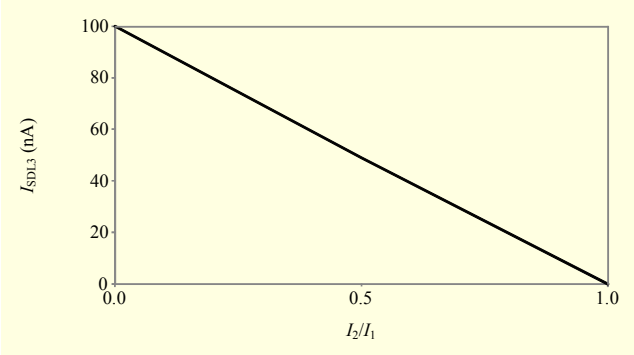

Fig. 3. Output current I_{SDL3} vs. ratio of I_2 / I_1.

I_2/I_1 in the case that I_1 has a constant value of 100 nA (I_1 = 100 nA) and I_2 can change from 0 nA to 100 nA. If the ratio of I_2/I_1 is equal ($I_1 = I_2$ = 100 nA), then no current will flow through ML3 (ML1). If the ratio of I_2/I_1 becomes 0 (I_2=0), then the value of ML3 (ML1) will reach the maximum value of the I_1 current ($I_{SDL3} = I_1$ =100 nA). Figure 3 also reveals that even though the difference between I_1 and I_2 is ultimately minimal, the proposed current source can realize this current. To improve the tail current, two current source circuits are utilized in parallel with the tail current of the conventional amplifier, as shown in Fig. 4.

The current provided by each of the current source circuits is equal to $A|\Delta I|$, where $|\Delta I|$is the absolute value of the difference between the current of I_1 and the current of I_2. The A parameter denotes the current feedback factor given in (3).

$$A = \frac{(W/L)_{T6,L6}}{(W/L)_{T5,L5}}. \tag{3}$$

The output current of the OTA operating in a weak inversion can be calculated as follows [2]:

$$\begin{aligned} I_o &= K \cdot (I_2 - I_1) \\ &= \frac{I_B(\exp(V_{in}/(nV_T)) - 1)}{(A+1) - (A-1)\cdot\exp(V_{in}/(nV_T))} \cdot K. \end{aligned} \tag{4}$$

Here, I_B is the quiescent bias current and V_{in} is the differential input voltage ($V_{in} = V_{in+} - V_{in-}$).

Suppose that all possible mismatches are taken into account in the current source and assume that the matching factor is defined as

$$m = 1 - \alpha_{mismatch}. \tag{5}$$

Here, m is the match factor and $\alpha_{mismatch}$ is the mismatch factor.

The currents of I_{S1} and I_{S2} delivered by each of the current sources of MT1 through MT6 and ML1 through ML6 can be derived as in (6) and (7), respectively.

$$I_{S1} = A \cdot (I_1 - m_2 \cdot I_2). \tag{6}$$

$$I_{S2} = A \cdot (I_2 - m_1 \cdot I_1). \tag{7}$$

Therefore, the output current can be derived as

$$\begin{aligned} I_o &= K \cdot (I_2 - m \cdot I_1) \\ &= \frac{I_B(\exp(V_{in}/(nV_T)) - m)}{(mA+1) - (A-1)\cdot\exp(V_{in}/(nV_T))} \cdot K. \end{aligned} \tag{8}$$

Thus, the minimum voltage required for the amplifier to operate in adaptive mode is as follows:

$$V_{min} = nV_T \cdot \ln(m). \tag{9}$$

Equation (10) highlights the conditions when the OTA does not slew and the output current tends to go to infinity.

$$\begin{aligned} V_{escape} &= nV_T \cdot \ln\left(\frac{Am+1}{A-1}\right) \\ &= nV_T \cdot \ln\left(\frac{A+1}{A-1} - \frac{A\alpha_{mismatch}}{A-1}\right). \end{aligned} \tag{10}$$

In addition, when a differential input signal (small or large signal) is applied, only one of the current sources is guaranteed by the TL topologies to realize current (Figs. 3 and 4), which leads to extremely reduced mismatched effects. Therefore, steady-state output current of the amplifier can be derived as in (11), ($A\alpha_{mismatch} << 1$):

$$I_o = K \cdot \frac{I_B}{1 - A\alpha_{mismatch}}. \tag{11}$$

Equation (11) clearly indicates that under steady-state conditions only one of the current sources should be turned on and its output current should be inclined to the maximum value, which can be verified by the proposed current source, as shown in Fig 3. Figure 3 also reveals that even though the difference

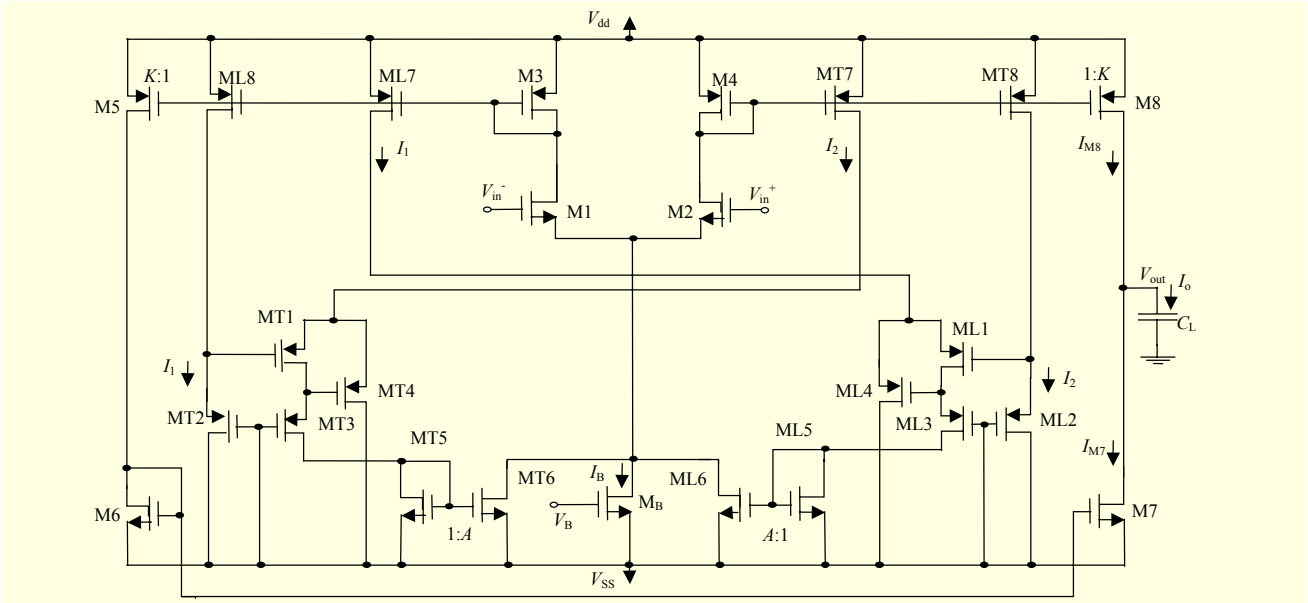

Fig. 4. Proposed adaptive biasing OTA. Two current source circuits of ML1- ML6 and MT1- MT6 realizing currents of $A(I_1–I_2)$ if $I_1 > I_2$ and $A(I_2–I_1)$ if $I_2 > I_1$, respectively.

between I_1 and I_2 becomes very small (that is, for a small-signal input), the proposed current source can utilize this current. So, this current source can decrease the distortion of the small-signal inputs significantly.

For $V_{in} > 0$, the current source of MT1 through MT6 realizes $A(I_2–I_1)$; consequently, through the positive feedback loop of M2, M4, MT7, and MT1 through MT6, the tail current increases, whereas the current source of ML1 through ML6 does not produce current. Similarly, for $V_{in} < 0$, the current source of ML1 through ML6 delivers $A(I_1–I_2)$ current, then through the positive feedback loop of M1, M3, ML7, and ML1 through ML6, the tail current increases by the same amount while the current source of MT1 through MT6 is turned off, as shown in Fig. 4. In principle, for the case in which $I_2 > I_1$, current I_1, which flows through MT4 (MT2), decreases, forcing the current that flows through MT1 (MT3) to increase. As a result, V_{SGT3} increases and MT4 (MT2) turns off. Similarly, when $I_1 > I_2$, current I_2, which flows through ML4 (ML2), tends to decrease, which causes the current that flows through ML1 (ML3) to increase by the same amount, therefore increasing V_{SGL3} and turning off ML4 (ML2).

Hence, the current produced by each of the current sources is always being offset by the TL topologies of ML1 through ML4 and MT1 through MT4 (Fig. 3), which leads to improved matching and decreases the mismatch factor ($\alpha_{mismatch}$) efficiently. For this reason, the positive feedback loop gain ($A\alpha_{mismatch}$) can increase without encountering stability problems (stability of the frequency response and stability of the positive feedback loop), as stated in (11). Additionally, as

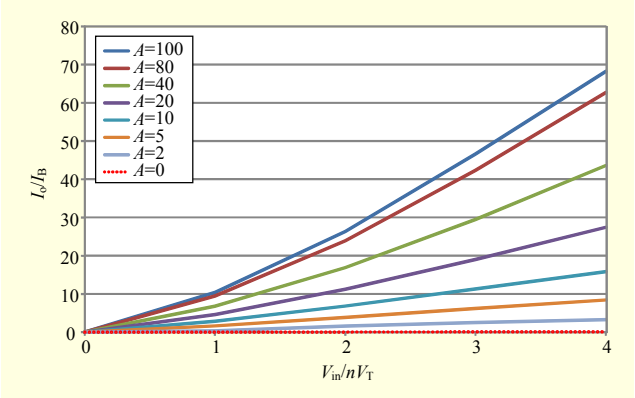

Fig. 5. Calculated output current vs. differential input voltage for different values of A and K=1, without adaptive biasing (dotted line) and with adaptive biasing (solid line).

(9) and (10) explain, when $A >> 1$, this reduces the minimum voltage and escape voltage to zero ($V_{min} \approx V_{escape} \approx 0$ V), meaning that the OTA does not slew except in the case that $V_{in} = 0$ V. However, when V_{in} goes up, the OTA operates in the adaptive mode and the output current drastically increases (Fig. 5). This means that the OTA will operate in the adaptive mode when a small-signal differential voltage is applied to the input, thereby helping to decrease the distortion of the small-signal input. This is a critical necessity of biological applications for which the input signal's amplitude is very small (V_{in} <<100 mV) [11]. Reducing the escape voltage not only decreases the distortion of small-signal inputs but allows the amplifier to operate with very small bias currents. However, the A factor of the circuits presented in [2] is limited by the mismatched

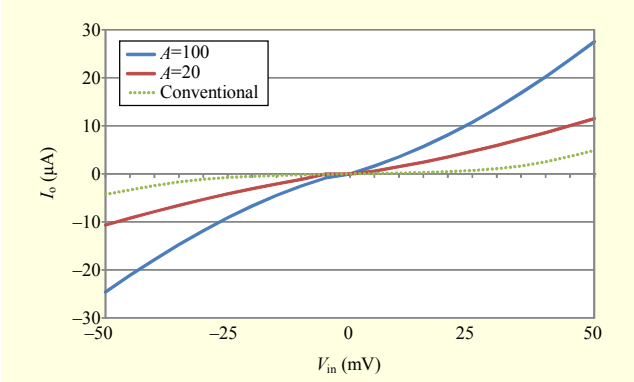

Fig. 6. Output current as function of small-signal inputs (I_B = 0). Conventional adaptive biasing amplifier (dotted line) and proposed adaptive biasing amplifier (solid line).

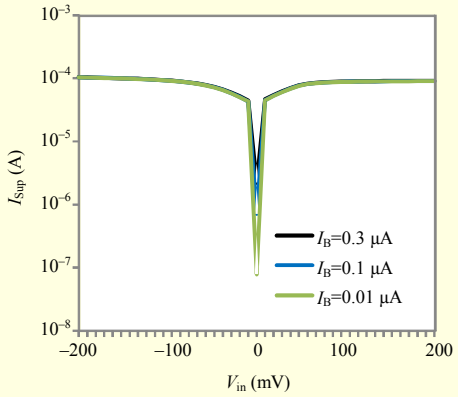

Fig. 7. Supply current as function of input voltage, A=20.

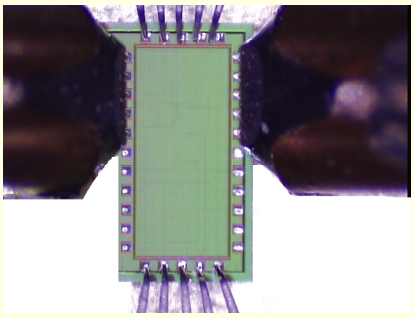

Fig. 8. Chip micrograph.

effects of their current sources, thereby increasing the mismatch factor ($\alpha_{mismatch}$). As a result, the output current is limited and not well controlled. Equation (11) and Fig. 5 show that the output current for $A < 10$ slightly increases and for $A > 10$ drastically increases.

Additionally, the output current for $A > 100$ slightly increases and almost reaches maximum. The calculated output currents in Fig. 5 are based on K=1 and different values of A (assuming ML1 through ML6 and MT1 through MT6 are matched and the input transistors are biased in weak inversion).

III. OTA Small-Signal Behavior

To enhance the slew rate and to reduce distortion of the small-signal inputs, two current sources using TL topologies are utilized in the positive feedback loops. Reducing mismatched effects causes the A factor to increase because the size of the currents delivered by each of the TL topologies is the same. As a result, the switching behavior between these two current sources at transients becomes faster since the current of the positive feedback loop can be amplified more. Figure 6 shows the output current as a function of the small-signal differential input voltage for $I_B = 0$. The escape voltage of the proposed adaptive biasing amplifier becomes very small, even though there is no bias current ($I_B = 0$). Therefore, for $A = 100$ and $A = 20$, the escape voltage is about 0.002 mV and 0.025 mV, respectively, whereas this voltage is about 40 mV for the conventional adaptive biasing op-amp. Indeed, for $I_B = 0$ and $V_{in} = 0$, only leakage currents flow in the OTA. As a differential voltage is applied, those leakage currents are fed back, resulting in a significant increase in the current level of the amplifier [2]. Therefore, the maximum output current is only determined by the A, K factors, and supply voltage. In practice, an increase in the A without decreasing the mismatch factor ($\alpha_{mismatch}$) is impossible because the positive feedback loop becomes unstable, as indicated in (11).

Figure 7 shows the supply current as a function of differential input signal (V_{in}) for three different values of bias current (I_B) and $A = 20$. Biased at 10 nA, the input transistors operate in weak inversion. When the input differential voltage increases up to 10 mV, the current consumption increases to about 30 μA; thus, the input transistors leave a weak inversion operation and the current increases so that (8) will no longer be valid. In the case that $V_{in} = 10$ mV, the total power consumption almost becomes independent of bias current (I_B).

IV. Measurement Results

The proposed amplifier is fabricated using 0.18-μm n-well CMOS technology. The amplifiers are tested with a supply voltage of ±0.6 V, an input bias current of 100 nA, and a capacitive load of 1 pF at room temperature (27ºC). The chip micrograph of the amplifiers is shown in Fig. 8.

The measurement results show that the total power consumption of the amplifier is only 0.44 μW. Figure 9 represents the output current of the proposed adaptive biasing amplifier as a function of V_{in}. The output current at 250 mV of the differential input voltage almost reaches the maximum. Additionally, the distortion of small-signal inputs is extremely

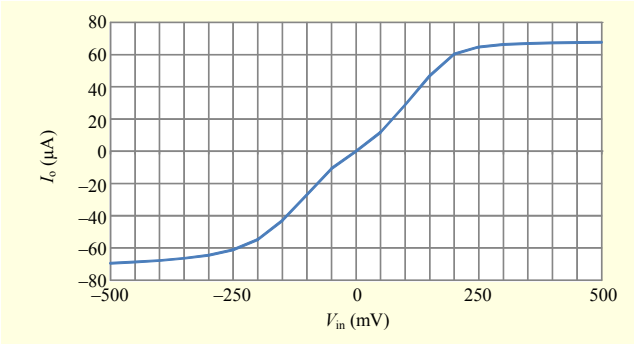

Fig. 9. Output current vs. differential input voltage, A=20.

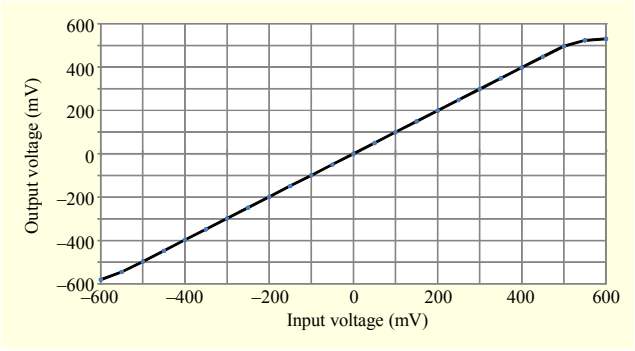

Fig. 11. DC transfer characteristic of amplifier in unity gain.

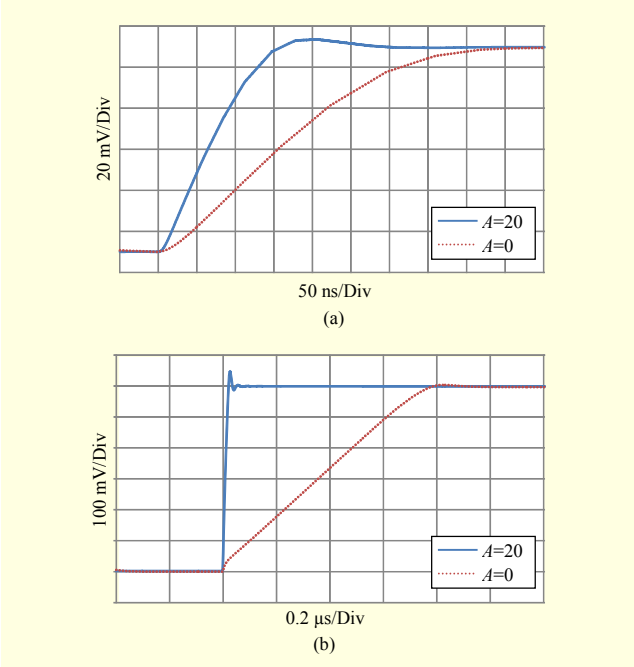

Fig. 10. Transient response of amplifier with adaptive biasing circuit (solid line) and without adaptive biasing circuit (dotted line): (a) small signal behavior of OTA; (b) large signal behavior of OTA; A=20.

Table 1. OTA's performance.

	Simulated value	Measured value
Supply voltage (V)	±0.6	±0.6
Capacitive load (pF)	1	1
Open loop gain (dB)	42.5	44
GBW (kHz)	605	590
Phase-margin	70°	68°
SR+ (V/μs)	68	71
SR– (V/μs)	–68	–72
Input offset voltage (mV)*	1.3	< 0.7
THD@1 kHz, 600 mV_{pp} (dB)	–50.5	–52
Settling time (0.1%) @ V_{in}=100 mV_{pp} (ns)	180	160
Settling time (0.1%) @ V_{in}=600 mV_{pp} (ns)	70	45
Maximum bias current (nA)	100	≤ 100
Power dissipation (μW)	0.5	≤ 0.44

*From measurement of five fabricated prototypes

reduced by enhancing the A. The escape voltage and minimum voltage are 0 V.

The response frequency shows that the amplifier has an open loop gain of 44 dB and a gain bandwidth (GBW) of 590 kHz. The compensation of the amplifier is done only with the original dominant pole capacitive load of 1 pF. Reducing the mismatched effects of the OTA and the size of the current sources, the active area is fairly small (204 μm^2).

The transient response of the amplifier with adaptive biasing circuit and without adaptive biasing circuit in a source-follower configuration is shown in Fig. 10. The measurement results show that the 0.1% settling time for a small input step (100 mV_{pp}) is improved from 1 μs to 160 ns (Fig. 10(a)), whereas the 0.1% settling time for a large input step (600 mV_{pp}) is improved from 2.6 μs to 45 ns by the adaptive biasing circuit (Fig. 10(b)). Also, the slew rate is improved by a factor of 270. Additionally, under these conditions and with a nominal voltage for the 0.18-μm CMOS process (that is, V_{dd}–V_{ss}= 1.8 V), the amplifier has a slew rate of 200 V/μs. The total harmonic distortion (THD) is computed for the linear input signal swing in unity gain when a sinusoidal signal with a 1-kHz frequency and 600 mV_{pp} is applied to the input. The corner simulations show that the proposed adaptive biasing amplifier has a THD of −50 dB, which is a satisfactory result for a strongly nonlinear biased operation of the OTA (the deep weak inversion operation). Furthermore, since sink and source currents are always being regulated by the TL topology circuits, the CMRR is significantly improved.

The DC transfer characteristic of the amplifier is shown in

Table 2. Comparison of measurement results.

	This work	[2]	[3]	[4]	[6]	[7]	[8]
CMOS process	0.18 µm	5 µm	0.5 µm	0.5 µm	0.35 µm	0.5 µm	0.13 µm
Supply voltage	±0.6 V	5 V	±1 V	±1 V	3.3 V	±1.25 V	±0.65 V / ±1 V
Capacitive load	1 pF	5 pF	80 pF	80 pF	13 pF	25 pF	1 nF
Phase-margin	68°	NA	90°	56°	61°	NA	45°
Input offset	< 0.7 mV	3.68 mV ±4 mV	NA	NA	29.1 mV	NA	NA
SR+	71 V/µs	23.5 V/µs	42 V/µs	10 V/µs	200 V/µs	2.7 V/µs	24.3 V/µs
SR–	–72 V/µs	NA	–80 V/µs	–15 V/µs	NA	–3.3 V/µs	NA
Power dissipation	0.44 µW	NA	140 µW	220 µW	4.8 mW	437.5 µW	1.2 mW
$FOM_1=I_{Lmax}/I_{Supply}$	193. 63	NA	48	7.3	1.78	6.4	33.3
$FOM_2= I_{Lmax}/I_B$	710	117.5	336	80	NA	112	NA
CMRR	110 dB	62 dB	69 dB	85 dB	NA	NA	NA
PSRR+	73 dB	63 dB	57 dB	41 dB	> 60 dB	67.3 dB	NA
PSRR–	48 dB	44 dB	46 dB	52 dB	NA	NA	NA
THD	–52 dB (0.6 V_{pp}, 1 kHz)	NA	–41 dB (0.9 V_{pp}, 100 kHz)	–37 dB (0.9 V_{pp}, 100 kHz)	–59 dB (0.4 V_{pp}, 700 kHz)	NA	–84 dB
GBW	590 kHz	NA	470 kHz	3.27 MHz	90 MHz	4.9 MHz	NA
Die area	204 µm^2	0.075 mm^2	0.042 mm^2	0.054 mm^2	0.0291 mm^2	0.0295 mm^2	0.1 mm^2

Fig. 11. The OTA has a linear input swing from −400 mV to 500 mV as shown in Fig. 11, which indicates that the measured value is in accordance with the simulated value.

Although the design has been implemented to charge large capacitive loads (≥ 100 pF) with A=20, it is possible to choose a larger value for A, if a higher driving capability is needed, without affecting the stability, as shown in (11). The comparison between simulated results and measured performances is drawn in Table 1. The experiment results are in accordance with the simulated ones due to reducing mismatched and distorted effects of the OTA.

Table 2 shows the performance comparison of this work with other works in the literature. The figures of merit (FOMs) shown in Table 2 are important quality factors reflecting the driving capability and power dissipation of an amplifier. FOM_1 [3], [7], [8] and FOM_2 [3] are defined as follows:

$$FOM_1 = \frac{I_{L\max}}{I_{Supply}}, \quad (12)$$

$$FOM_2 = \frac{I_{L\max}}{I_B}. \quad (13)$$

Here, I_{Lmax} is the maximum output current provided to the load, I_{Supply} is the total quiescent current of the supply voltage, and I_B is the quiescent bias current. In this work, these factors have been greatly improved.

V. Conclusion

In this paper, a novel adaptive biasing OTA was presented. Experiment results show significant performance improvements regarding the large/small signal and power dissipation properties. This amplifier consumes only 0.4 µW from a power supply voltage of ±0.6 V. Having a high slew rate and low power dissipation, this amplifier can be used to handle portable devices and biomedical applications for which the low power dissipation and fast settling time properties are critical necessities.

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