Data Randomization Scheme for Endurance Enhancement and Interference Mitigation of Multilevel Flash Memory Devices

Jaewon Cha and Sungho Kang

In this letter, we propose a data randomization scheme for endurance and interference mitigation of deeply-scaled multilevel flash memory. We address the relationships between data patterns and the raw bit error rate. An on-chip pseudorandom generator composed of an address-based seed location decoder is developed and evaluated with respect to uniformity. Experiments performed with 2x-nm and 4x-nm NAND flash memory devices illustrate the effectiveness of our scheme. The results show that the error rate is reduced up to 86% compared to that of a conventional cycling scheme. Accordingly, the endurance phenomenon can be mitigated through analysis of interference that causes tech shrinkage.

Keywords: Flash memory, reliability, raw bit error rate, endurance, interference, pseudorandom generator.

I. Introduction

As cell sizes become smaller, NAND flash faces a serious credibility problem when used in multilevel cells [1]. NAND flash memory also suffers from undergoing a large number of erase/write (E/W) cycles during its lifetime. Every cycle causes tunnel oxide degradation, which limits the endurance characteristics, due to Fowler-Nordheim (FN) stress [2]. Therefore, several techniques have been proposed to prevent endurance reduction. Error correction code (ECC) is a primary way to reduce bit errors for existing applications [3], [4]. However, memory capacity is decreased when ECC is used because the number of additional spare bits is increased in proportion to the number of errors requiring parity checking. Data randomization is another solution for suppressing errors in data storage systems, especially solid state drive controllers [5], [6]. The basic idea of this scheme is to operate the data transformation from original user data to minimize the probability of error, such as by using address/data scrambling schemes. Unfortunately, data randomization has an insufficient consideration for the typical character of flash memory, such as the interference. NAND flash reliability has received a great deal of attention since sub-40-nm processes were first introduced, as NAND flash lacks the Vth margin caused by floating gate (FG) coupling between cells [7]. The incremental step pulse program (ISPP) [8] and the most significant bit (MSB) page program with the temporary least significant bit data storing scheme [7] can reduce interference caused by bit-line neighbor cells. However, for 30-nm processes, it is necessary to explore additional schemes because FG coupling becomes stronger [9]. Interference cancellation (IC)-read [10] and MSB reprogram (re-PGM) schemes [9] are other attempts to minimize error. These schemes focus on cell-to-cell interference related to endurance errors. Therefore, to mitigate interference between cells, the IC-read algorithm is required to read each page several times, and the MSB re-PGM algorithm is required to write the MSB page twice. These two schemes have serious drawbacks, including performance drop and internal algorithm complexity. To develop an endurance enhancement scheme without disadvantages, we present a new data randomization scheme with a pseudorandom generator composed of the address-based seed location decoder for interference mitigation of all directions.

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II. Correlation of Endurance and Interference

Figure 1 shows three kinds of data patterns related to the endurance. Case 1 is a program verification third (PV3) solid pattern, which represents the worst E/W cycling in the past because many electrons move from the substrate to the FG to be positioned in the distribution of the PV3 state in 100% of the memory cells. Thus, tunnel oxide is the most severe in this case due to FN stress [2]. Case 2 is a PV1_PV3 pattern, in which PV1 cells are placed around PV3 cells. Therefore, the PV1 cell distribution is deeply shifted toward the PV3 state during PV3 write operations using the ISPP [6]. In addition, this pattern is the most vulnerable to the interference in even-odd bit-line architecture and used as the standard for quality specifications during reliability tests since it causes more read errors due to the interference effect. Case 3 is the data random pattern. All cells are uniformly distributed, and each distribution includes 25% of the cells. After the data randomization, every user pattern is present, such as in Case 3. Figure 2 shows the measured raw bit error rate (RBER), which is the fraction of bits that contains incorrect data for the cycling of each data pattern in 4x-nm commercial NAND flash memory. This figure is deeply related to the cell interference and the RBER of the patterns because a PV1_PV3 pattern has the highest error rate.

In addition, one important thing is that a solid PV3 pattern has the lowest error. There are two reasons. One is a solid pattern has a smaller interference influence than others [7]. The other is a solid PV3 has a considerable Vth margin due to over program disturbance [11]. According to the results mentioned above, we must pay attention to the relationship between the endurance and the interference especially.

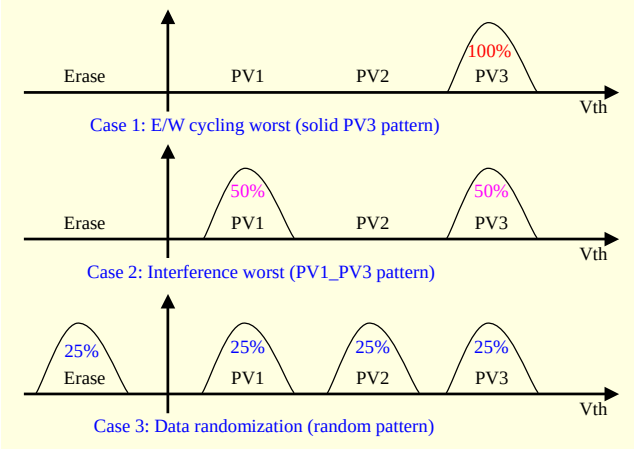

Fig. 1. Representative data patterns related to endurance.

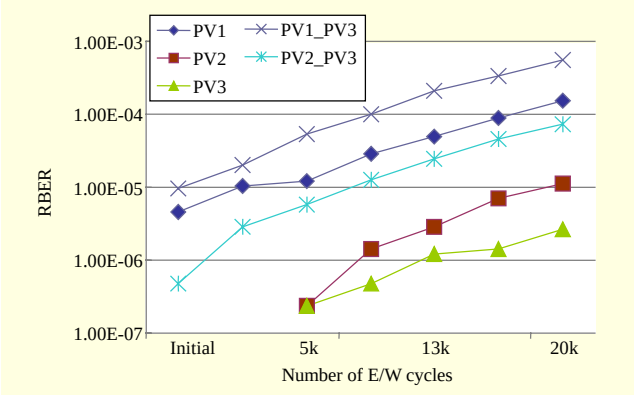

Fig. 2. Data pattern dependency by cycling in 4x-nm flash (repeating cycles erase and PV3 write, measured RBER by each pattern.)

III. Data Randomization Using 8-bit LFSR

The data randomization is defined as an operation that randomly distributes and records data patterns to decrease the occurrence of the same data in succession. This is an essential function for the maintenance of data reliability that uses error preventive write and read operations for the data. This scheme is one of the most effective methods to remove the probability of worst-case data pattern errors that have occurred in flash memory. Figure 3 shows the 8-bit linear feedback shift register (LFSR) [3] with the address-based seed location decoder, which generates the random values (RVs) in the horizontal direction and vertical direction simultaneously. In addition, Fig. 4 shows RV permutation generated by the address-based

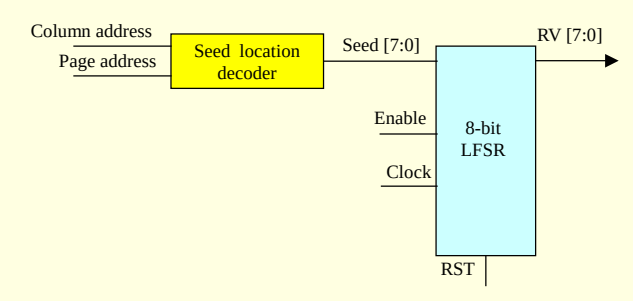

Fig. 3. 8-bit LFSR with address-based seed location decoder.

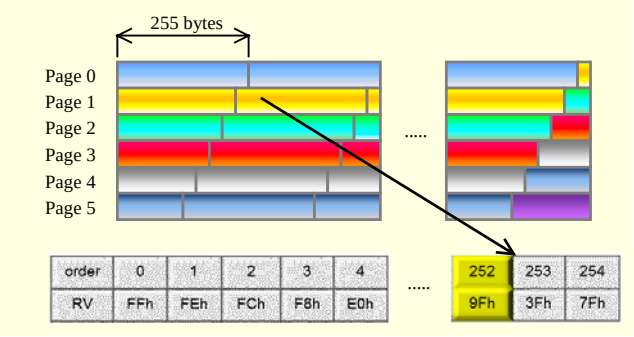

Fig. 4. RV permutation for interference mitigation.

seed location decoder. The RVs are mixed vertically, such as the diagonal pattern, due to considering the interference effect of a row. Therefore, this scheme can make bidirectional interference mitigation located in the row and the column together. If the column address is 248 decimal (d) and the page address is 4 d, the remainder is 252 d divided by 255 d, and the corresponding value of the RV is 9Fh, as in Fig. 4. The LFSR is configured as a shift register.

IV. Simulation and Test Results

Ideally, the data randomization should be divided into precisely 25% of the number of cells, as in Case 3 of Fig. 1. However, there is a mismatch because the actual period of the proposed LFSR is 255. Table 1 shows the score of the uniformity after applying the 8-bit LFSR based on the standard deviation and variance, depending on the user input pattern. In probability theory, the variance is a measure of how far the numbers lie from the expected value. However, the standard deviation, which is obtained as the square of the variance, is used more frequently than the variance. The formula for a score of uniformity is as follows:

$$\text{Score of uniformity} = [(43.3 - \text{standard deviation})/43.3] \times 100. \quad (1)$$

The usefulness of data randomization highly depends on the patterns of user data. However, we perform simulation using other patterns, shown in Table 1. We select these patterns because of the standard patterns for functional testing of flash memory. Generally, these patterns can be generated by the device itself to save data input time for test cost, but user data cannot. Therefore, the regular test patterns shown in Table 1 are more effective than user data and actually used in the industry.

From this perspective, the test with data randomization using the patterns in Table 1 is more effective than using user data. We can test E/W cycling using patterns in Table 1. This test is quite efficient for the device because the cells of memory need to take the stress equally. The test mentioned above can prevent the stress of certain cells continuously during the cycling. The most patterns have scores of uniformity over 99 in Table 1. This means that there is 1% variation compared to the ideal pattern. As a result, the probabilities of errors do not differ between the ideal pattern and the others.

Increasing the probability of large errors leads to weak endurance due to a wider Vth. Figure 5 shows the endurance errors for the patterns in the 4x-nm NAND flash memory device. The RBER is reduced using the pseudorandom pattern. Error reduction factors in 4x-nm flash are summarized in Fig. 5 and Table 2. The cycling factor of the reduction rate is 36%, and the interference factor of the reduction rate is 97%. Consequently, the interference factor affects the correlation between the endurance and the RBER more than the cycling factor does. Figure 6 shows the endurance errors according to patterns in the 2x-nm NAND flash memory devices, such as the devices shown in Fig. 5. We measure only 3-K E/W cycles (20-K E/W in 4x-nm flash) due to the rapid increase of the RBER caused by cell size reduction. Table 3 shows the error reduction factor, which refers to Fig. 6. As shown, the cycling factor of the reduction rate is 48%, and the interference factor of the reduction rate is 86%. Compared to the results obtained

Table 1. Scores of uniformity when applying 8-bit LFSR.

User Pattern	Erase (%)	PV1 (%)	PV2 (%)	PV3 (%)	Variance	Standard deviation	Score of uniformity
“IDEAL”	25.0	25.0	25.0	25.0	0	0	100
“The Worst”	0	0	100	0	1865	43.3	0
All “00”	25.1	25.1	24.7	25.1	0.028	0.169	99.6
All “FF”	24.7	25.1	25.1	25.1	0.028	0.169	99.6
All “AA”	24.9	25.1	24.9	25.1	0.009	0.098	99.8
All “55”	24.9	25.1	24.9	25.1	0.009	0.098	99.8
Logical CKBD	25.0	25.1	24.8	25.1	0.014	0.120	99.7
Random*	24.5	25.3	25.6	24.7	0.196	0.443	99.0

* Real RV generated by C-language.

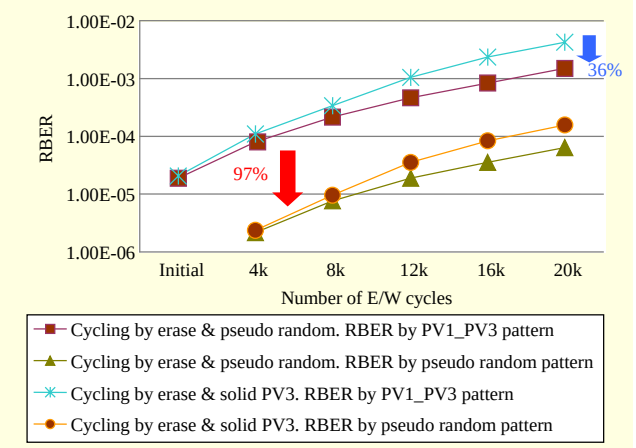

Fig. 5. Endurance error according to patterns in 4x-nm flash.

Table 2. Error reduction factor in 4x-nm flash.

Factor	Reduction rate of RBER
Cycling between random and solid PV3	36%
Interference between random and PV1_PV3	97%

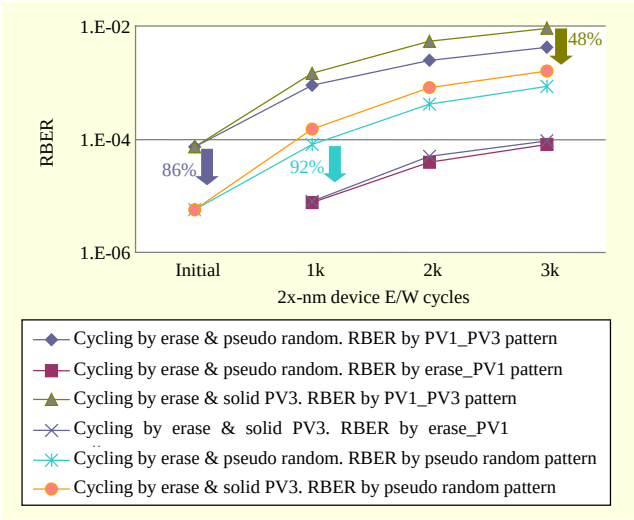

Fig. 6. Endurance errors according to patterns in 2x-nm flash.

Table 3. Error reduction factors in 2x-nm flash.

Factor	Reduction rate of RBER
Cycling between solid PV3 and random	48%
Interference between PV1_PV3 and random	86%
Interference between random and E_PV1	92%

using the 4x-nm flash, the cycling factor is increased and the interference factor is decreased, which is seen as a tech-shrinkage phenomenon. E_PV1 is a test pattern with no interference between the cells because there is a PV1 cell around the erase cells, similar to the shielding effect. The reduction rate of the RBER between the pseudorandom and the E_PV1 pattern is 92%, as shown in Table 3.

V. Conclusion

Lack of endurance for flash memory is a serious problem that causes tech shrinkage. Through experiments, we showed that the major factor underlying this problem is coupling between cells rather than oxide degradation due to FN stress. Accordingly, we focused on interference rather than cycling to achieve high endurance. We proposed a randomization scheme for user data that yields high endurance and interference mitigation. Table 4 showed comparison among endurance enhancement schemes. The proposed scheme yields significantly better results than others, achieving no performance delay, small chip size burden, and low design complexity. Most importantly, the endurance enhancement of the proposed scheme exceeds that of others because it achieves bidirectional interference cancellation. In addition, the results

Table 4. Comparison among endurance enhancement schemes.

	Re-PGM [9]	IC-Read [10]	Proposed
Performance delay rate	20% (write delay)	70% (read delay)	No
Chip size burden	Medium	Small	Small
Design complexity	High	Middle	Low
Interference cancellation	X-axis	X-axis	X-axis, Y-axis
Endurance enhancement	Medium	Medium	Very high

using 2x-nm and 4x-nm NAND flash memory devices show that the proposed scheme achieves high endurance. As a result, the endurance phenomenon can be mitigated.

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