10-Bit 200-MS/s Current-Steering DAC Using Data-Dependant Current-Cell Clock-Gating

Byung-Do Yang and Bo-Seok Seo

This letter proposes a low-power current-steering digital-to-analog converter (DAC). The proposed DAC reduces the clock power by cutting the clock signal to the current-source cells in which the data will not be changed. The 10-bit DAC is implemented using a 0.13-μm CMOS process with V_{DD}=1.2 V. Its area is 0.21 mm^2. It consumes 4.46 mW at a 1-MHz signal frequency and 200-MHz sampling rate. The clock power is reduced to 30.9% and 36.2% of a conventional DAC at 1.25-MHz and 10-MHz signal frequencies, respectively. The measured spurious free dynamic ranges are 72.8 dB and 56.1 dB at 1-MHz and 50-MHz signal frequencies, respectively.

Keywords: Clock-gating, data-dependant, digital-to-analog converter (DAC), low-power.

I. Introduction

Current-steering digital-to-analog converters (DACs) have been widely used in high-speed DACs requiring a large spurious free dynamic range (SFDR) and a wide bandwidth [1]-[9]. The current-steering DACs are based on a segmented structure using unary-encoded and binary-weighted current-source cells, as shown in Fig. 1. To achieve a high performance, a large number of current-source cells and a high sampling frequency are required. However, these requirements increase the DAC power consumption, which consists of the analog power in the current-source cells and the digital power in the decoder circuits and clock buffer. The digital power increases in proportion to the number of current-source cells and the sampling frequency. The clock power is a dominant factor in the digital power consumption. In this letter, a low-power current-steering DAC using a data-dependant current-cell clock-gating scheme is proposed. It significantly reduces the clock power by cutting the clock signal to the current-source cells in which the data will not be changed.

Manuscript received June 27, 2012; accepted Aug. 2, 2012.

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science, and Technology (2012R1A1A4A01015759). The chip fabrication was supported by the IC Design Education Center (IDEC).

Byung-Do Yang (phone: +82 43 261 3583, bdyang@cbnu.ac.kr) and Bo-Seok Seo (boseok@cbnu.ac.kr) are with the Department of Electronics Engineering, Chungbuk National University, Cheongju, Rep. of Korea.

http://dx.doi.org/10.4218/etrij.12.0212.0286

II. Architecture

Figure 1(a) shows the block diagram of a conventional 10-bit current-steering DAC, which has a 6+2+2 segmented structure consisting of six linearly decoded most significant bits (MSBs), two linearly decoded upper least significant bits (ULSBs), and two binary weighted lower least significant bits (LLSBs). The six MSBs are divided into three upper MSBs (UMSBs) used for a row decoder and three lower MSBs (LMSBs) used for a column decoder. The DAC has 255 unary current-source cells and two binary-weighted current-source cells. The cell array consists of four symmetric subcell arrays made up of 63 current-source cells and three current-source cells. The subcell array has eight rows and eight columns. Figure 1(b) shows the current-source cell. The cell data is updated by the clock signal during every clock cycle. At a high sampling rate, the clock power becomes large due to the high capacitive lines and the large number of current-source cells.

Figure 2 shows the MSB 6-bit input codes of the input signal and the changed data in a subcell array. At Input #2, the data changes only in row<4>. The clock signal is needed only for the eight current-source cells in row<4>. No clock signal is required for any of the rows except for row<4>. At Input #3, the data in row<4> and row<5> changes. The clock signal is necessary in row<4> and row<5>. Therefore, the clock power can be reduced by selectively enabling the clock signals for the

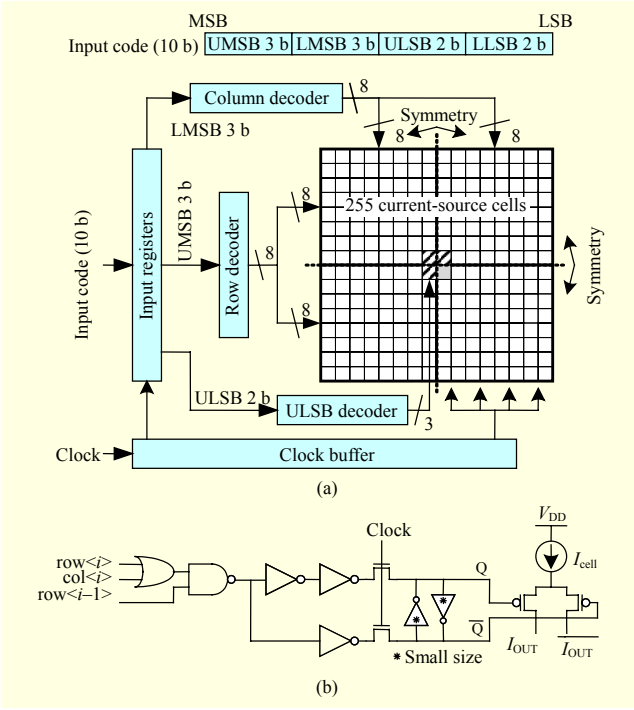

Fig. 1. (a) Block diagram of segmented structure (6+2+2) in conventional 10-bit current-steering DAC and (b) schematic of current-source cell.

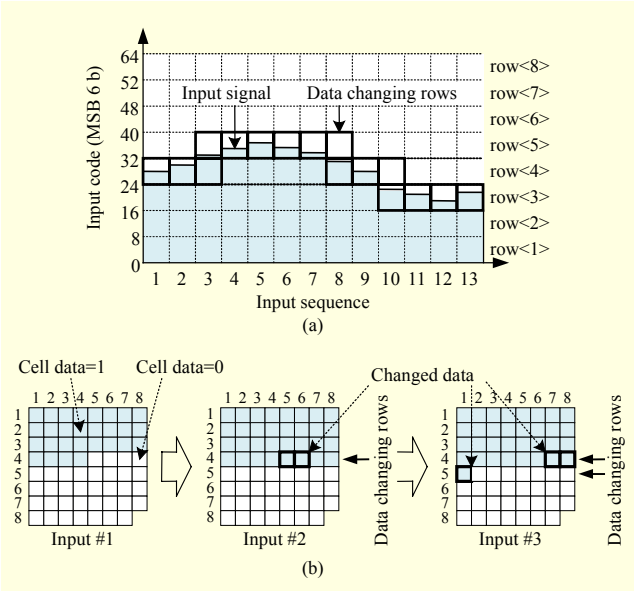

Fig. 2. (a) MSB 6-bit input codes of input signal and (b) changed data in subcell array.

rows in which data changes.

Figures 3(a) and 3(b) show the number of average clock-enabled rows among the eight rows in the DAC according to the input signal frequency and the normalized amplitude of the sine input signal, respectively. The number of average clock-enabled rows decreases as the swing voltage and the frequency

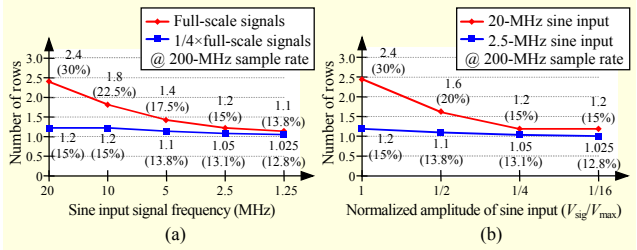

Fig. 3. Number of average clock-enabled rows among eight rows in DAC according to (a) input signal frequency and (b) normalized amplitude of sine input signal.

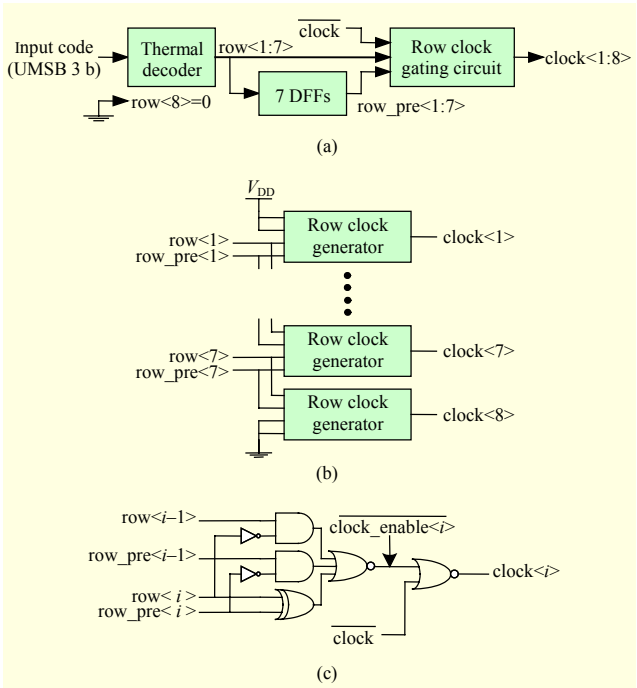

Fig. 4. (a) Proposed row decoder, (b) row clock gating circuit, and (c) row clock generator.

of the sine input signal decrease and is reduced to 2.4 to 1.1 rows (30% to 13.8%) when the frequency of the full-scale sine input signal is approximately 20 MHz to 1.25 MHz at a 200-MHz sample rate.

Figure 4 shows the proposed current-cell clock-gating row decoder. It consists of a conventional thermal decoder, 7-bit data flip-flops (DFFs), and an 8-bit row clock-gating circuit. The thermal decoder determines the row data (row<1:7>) for the current-source cells (Fig. 1(b)). The DFFs store the previous row data (row_pre<1:7>). The row clock-gating circuit enables the appropriate row clock signals (row_clock<1:8>). Figure 5 shows an example of the clock enable signals in the proposed row decoder.

Table 1 shows the power consumption of 10-bit DACs at a 200-MHz sampling rate. The conventional and proposed DACs are simulated using a 0.13-μm CMOS process with V_{DD}

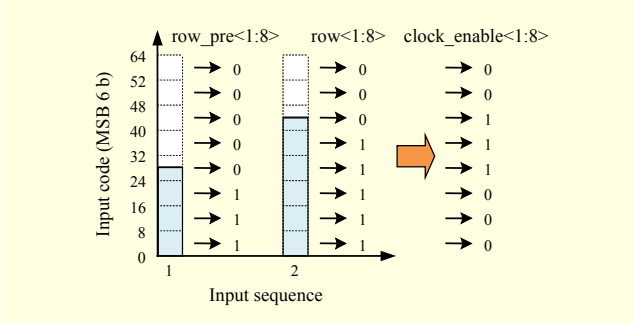

Fig. 5. Example of clock enable signals.

Table 1. Power consumption of 10-bit DACs @ 200 MS/s.

	Conventional DAC (A) (mW)		Proposed DAC (B) (mW)		Ratio (B/A) (%)	
Input signal (MHz)	10	1.25	10	1.25	10	1.25
Clock circuits	0.94	0.94	0.34	0.29	36.2%	30.9%
Decoder circuits	0.56	0.16	0.56	0.16	100%	100%
Cell current	4	4	4	4	100%	100%
Current reference	0.08	0.08	0.08	0.08	100%	100%
Total	5.58	5.18	4.98	4.53	89.2%	87.5%

= 1.2 V. The powers are measured with full-scale signals at 10-MHz and 1.25-MHz signal frequencies. The output current is 3.33 mA. The clock power is reduced to 36.2% and 30.9% of the conventional DAC at 10-MHz and 1.25-MHz signal frequencies, respectively. The proposed DAC consumes 4.98 mW and 4.53 mW at 10-MHz and 1.2-5MHz signal frequencies, respectively. It saves 10.8% and 12.5% of the DAC power compared to the conventional DAC at 10-MHz and 1.25-MHz signal frequencies, respectively. The area overhead of the proposed row decoder is 127 μm^2 (0.063%).

III. Experiment Results

The 10-bit DAC is fabricated using a 0.13-μm CMOS process with V_{DD} = 1.2 V. All measurements are made at a 200-MHz sampling rate with a 3.3-mA load current. The single output swing voltage is 0.5 V for the full-scale signals. Figure 6 shows the measured integral nonlinearity (INL) and differential nonlinearity (DNL). Figure 7 shows the measured spectrum of the DAC output. The SFDRs are 7.8 dB and 56.1 dB at 1-MHz and 50-MHz signal frequencies, respectively. Figures 8 and 9 respectively show the spectral performance of the full-scale

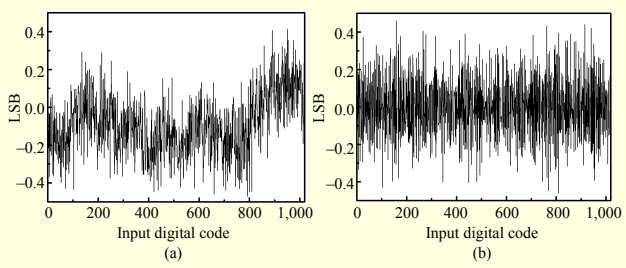

Fig. 6. (a) Measured INL and (b) measured DNL.

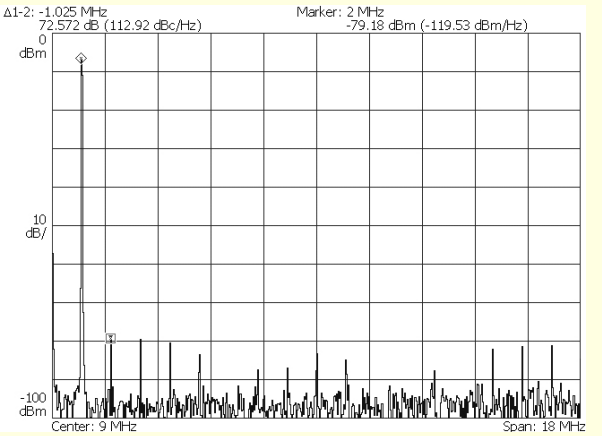

Fig. 7. Measured spectrum @ f_{sig}=1 MHz and 200 MS/s.

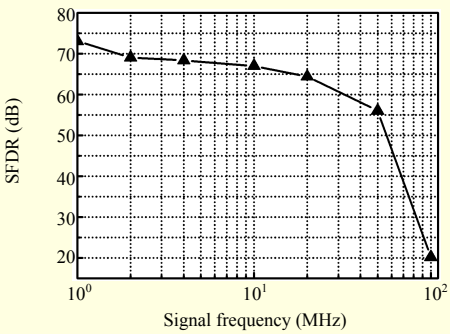

Fig. 8. Measured SFDR plot @ 200 MS/s.

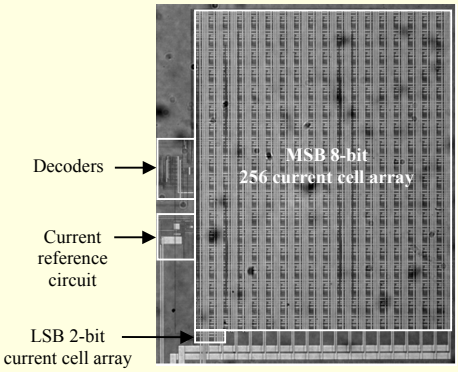

Fig. 9. Chip microphotograph.

Table 2. Summary of measured performance.

Technology	0.13-μm CMOS
Resolution	10 b
Supply voltage	1.2 V
Load current	3.3 mA
Output swing	0.5 V (single), 1 V (differential)
INL	< 0.47 LSB
DNL	< 0.46 LSB
Sampling rate (f_{CLK})	200 MHz
SFDR @ f_{CLK}=200 MHz	72.8 dB @ 1 MHz, 56.1 dB @ 50 MHz
Power @ f_{CLK}=200 MHz	4.46 mW @ f_{sig} = 1 MHz
Active area	0.21 mm^2

Table 3. Power comparison of DAC chip @ 1 MHz & 200 MS/s.

	Proposed DAC (mW)	
	Simulation	Measurement
Clock	0.28	0.38
Digital	0.14	
Cell current	4.00	4.00
Current reference	0.08	0.08
Total	4.50	4.46

Table 4. Comparisons of 10-bit current-steering DACs.

		[2]	[7]	This work
Number of bits		10	10	10
Sample rate		500 MS/s	250 MS/s	200 MS/s
SFDR		> 51 dB @ 240 MHz	> 60 dB @ 122.5 MHz	72.8 dB @ 1 MHz 56.1 dB @ 50 MHz
Technology		0.35-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
Supply voltage		3.3 V	1.8 V	1.2 V
Load current		18 mA	10 mA	3.3 mA
Power	Total	125 mW @ 100 MS/s	22 mW @ 250 MS/s	4.5 mW @ 1 MHz & 200 MS/s
	Digital	66 mW	4 mW	0.4 mW
	Analog	59 mW	18 mW	4.1 mW
Area		0.6 mm^2	0.35 mm^2	0.21 mm^2

signals and the microphotograph of the DAC chip. The core area of the DAC chip is 0.21 mm^2. Table 2 summarizes the measured performance of the DAC chip. It consumes 4.46 mW at a 1-MHz signal frequency. Table 3 compares the simulated and measured powers in the DAC chip. Table 4 shows comparisons of 10-bit current-steering DAC performances.

IV. Conclusion

A low-power current-steering DAC using a data-dependant current-cell clock-gating scheme was proposed. The 10-bit DAC was implemented using a 0.13-μm CMOS process with V_{DD} = 1.2 V. It reduced the clock power consumption to 30.9% and 36.2% of the conventional DAC at 1.25-MHz and 10-MHz signal frequencies, respectively, by enabling the clock signal only for the current-source cells in which the data will be changed. Its core area was 0.21 mm^2. It consumed 4.46 mW at a 1-MHz signal frequency and 200-MHz sampling rate. The measured SFDRs were 72.8 dB and 56.1 dB at 1-MHz and 50-MHz signal frequencies, respectively.

References

[1] J. Bastos et al., "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, Dec. 1998, pp. 1959-1969.

[2] C-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, Dec. 1998, pp. 1948-1958.

[3] A. Van den Bosch et al., "A 10-Bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, Mar. 2001, pp. 315-324.

[4] Y. Cong et al., "A 1.5-V 14-Bit 100-MSample/s Self-Calibrated DAC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, Dec. 2003, pp. 2051-2060.

[5] K. O'Sullivan et al., "A 12-bit 320-MSample/s Current-Steering CMOS D/A Converter in 0.44 mm^2," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, July 2004, pp. 1064-2060.

[6] J.A. Starzyk et al., "A Cost-Effective Approach to the Design and Layout of a 14-b Current-Steering DAC Macrocell," *IEEE Trans. Circuits Sys. I, Reg. Papers*, vol. 51, no. 1, Jan. 2004, pp. 196-300.

[7] J. Deveugele et al., "A 10-bit 250-MS/s Binary-Weighted Current-Steering DAC," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, Feb. 2006, pp. 320-329.

[8] D.A. Mercer, "Low-Power Approaches to High-Speed Current-Steering Digital-to-Analog Converters in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, Aug. 2007, pp. 1688-1698.

[9] C.-H. Lin et al., "A 12 bit 2.9 GS/s DAC with IM3 < –60 dBc Beyond 1 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, Dec. 2009, pp. 3285-3293.