Simultaneous Static Testing of A/D and D/A Converters Using a Built-in Structure

Incheol Kim, Jaewon Jang, HyeonUk Son, Jaeseok Park, and Sungho Kang

Static testing of analog-to-digital (A/D) and digital-to-analog (D/A) converters becomes more difficult when they are embedded in a system on chip. Built-in self-test (BIST) reduces the need for external support for testing. This paper proposes a new static BIST structure for testing both A/D and D/A converters. By sharing test circuitry, the proposed BIST reduces the hardware overhead. Furthermore, test time can also be reduced using the simultaneous test strategy of the proposed BIST. The proposed method can be applied in various A/D and D/A converter resolutions and analog signal swing ranges. Simulation results are presented to validate the proposed method by showing how linearity errors are detected in different situations.

Keywords: Mixed-signal testing, A/D converter, D/A converter, BIST, static testing.

I. Introduction

Monolithic integration (system on chip [SoC]) and single package integration (system in package [SiP]) are currently preferred due to their economic benefits. Digital signal processing and analog systems are often included in these packages. As semiconductor design technology has developed, some analog systems have been replaced with digital systems, but analog circuitries, which affect the performance of the overall system, are still used. In most mixed-signal circuits, analog-to-digital (A/D) and digital-to-analog (D/A) converters have played increasingly important roles [1] because they provide links between digital signal processing systems and the analog world. The accuracy of these converters may limit the performance of the digital domain; therefore, testing such data converters is very important for modern electronic devices.

However, in SoC and SiP environments, testing the analog circuitry is not easy: it is deeply embedded and difficult to access. Tests of the embedded blocks must therefore consider observability and controllability. Furthermore, the International Technology Roadmap for Semiconductors (ITRS) states that to reduce test time and cost and to increase test throughput in analog/mixed-signal testing, increased use of multisite parallel and concurrent testing is needed [2]. To support these requirements, analog/mixed-signal design for testability and built-in self-test (BIST) have been suggested as possible solutions [3].

BIST has been a good solution in digital domains, but not in the mixed-signal world. Analog stimuli and measurement of analog responses are needed for on-chip testing of A/D and D/A converters. These additional analog circuitries require high accuracy, and, as a result, more hardware overhead is inevitable. Built-in self-calibration (BISC) also can be a solution, but

Manuscript received Apr. 2, 2012; revised July 30, 2012; accepted Aug. 7, 2012.

This research was supported by the MKE (The Ministry of Knowledge Economy), Rep. of Korea, under the CITRC (Convergence Information Technology Research Center) support program (NIPA-2012-H0401-12-1006) supervised by the NIPA (National IT Industry Promotion Agency).

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http://dx.doi.org/10.4218/etrij.13.0112.0198

BISC requires more hardware overhead than BIST. Moreover, in BISC, the ideality of the built-in circuits is more important than in BIST. These can limit the application of BISC.

There are two test strategies for testing A/D and D/A converters: static method and dynamic method. However, the tests mostly consist of specification-based functional testing in production. In other words, the testing strategy is determined by the end use of the A/D and D/A converters [4]. The dynamic test has a limit on BIST implementation because a microprocessor or a processing unit is indispensable for calculating dynamic parameters. On the other hand, the static test is easier to apply to BIST, and this paper focuses on a static BIST for A/D and D/A converters.

Over the years, several methods have been developed for the static A/D and D/A converter BIST [5]-[9]. The loopback test is one of the most popular methods for testing data converters [5]-[7], but the fault masking problem has always been an issue. In [5], a BIST method using Gaussian noise for linearity characterization is proposed, but this method requires a large number of samples resulting in a long test time. The authors in [6] proposed a method for linearizing the D/A converter using a digital equalizer; yet, this method also requires many samples and a long test time. In [7], the authors scaled the D/A converter output to raise the effective A/D and D/A converters' resolutions. However, their method requires modification of the device under test (DUT) circuitry. Other methods without loopback configurations [8], [9] have also been proposed, but they either do not test entire codes [8] or require heavy area overhead.

In this paper, a new BIST structure for static testing of A/D and D/A converters is proposed. Although static testing of A/D and D/A converters generally consumes a lot of test time [5] due to the large number of samples required, the proposed method reduces both the test time and the hardware overhead. To reduce the test time, we test both the A/D and D/A converters simultaneously. The test time is greatly reduced compared to that of the loopback test. In addition, the hardware overhead is reduced compared to that of the standalone BIST by sharing additional BIST circuitry for testing the converters. Furthermore, the proposed BIST considers the various specifications of the converters. The construction of the BIST for various cases is provided. In section II, the static linearity errors for the A/D and D/A converter testing are explained, and the modified equations for the proposed BIST are introduced. Section III describes the proposed BIST structure for each converter (A/D and D/A) separately, and then the combined structures for different cases are explained. Section IV shows the Verilog HDL and HSPICE simulation results of the proposed BIST for various cases, and section V concludes the paper.

II. Preliminaries

A static test checks how the output of an A/D or D/A converter deviates from the ideal output. Generally, static errors include offset, gain, integral nonlinearity (INL), and differential nonlinearity (DNL). In the test specification, an acceptable error range is given. For example, if the acceptable range is given as ±1/2 of the least significant bit (LSB), the test for the target A/D or D/A converter indicates an unacceptable error whenever the difference between the output of the target converter and the ideal expected output is larger than 1/2 LSB. In this section, the static parameters for the A/D and D/A converters are expressed as equations. The calculation of these parameters is based on [10]. The acceptable error range is assumed to be ±1/2 LSB, the value most frequently used.

1. A/D Converter Test

The static parameters for the A/D converter test are shown in Fig. 1. The equations for testing static parameters are shown below, under the assumption that the test stimulus is a ramp with a start voltage of 0 V.

$$\text{Offset: } INL_{ADC}(0) < 1/2 \text{ LSB}, \quad (1)$$

$$\text{Gain: } -1/2 \text{ LSB} < INL_{ADC}(2^n-1) < 1/2 \text{ LSB}, \quad (2)$$

$$\text{INL: } -1/2 \text{ LSB} < INL_{ADC}(k) < 1/2 \text{ LSB}, \quad (3)$$

$$\text{DNL: } -1/2 \text{ LSB} < DNL_{ADC}(k) < 1/2 \text{ LSB}. \quad (4)$$

In (1) through (4), $INL_{ADC}(k)$ signifies the distance between the ideal and the actual k-th transition, as shown in Fig. 1. The test starts when k is "0," and the distance at the test start is "the offset." The resolution of the target A/D converter is n. Meanwhile, $DNL_{ADC}(k)$ is calculated by subtracting 1 LSB from the distance between the consecutive transitions. As

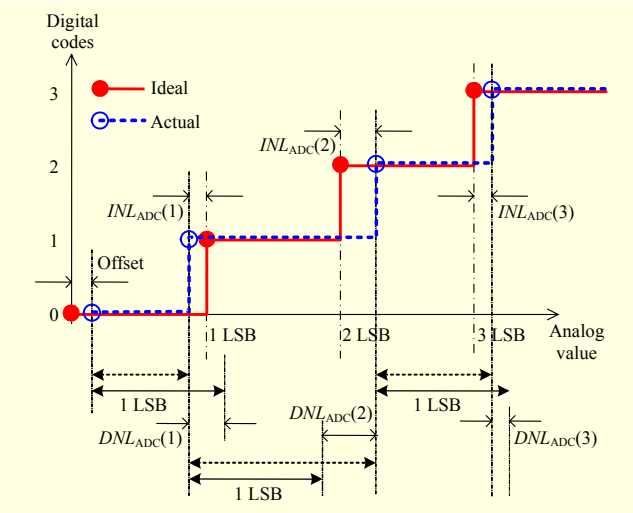

Fig. 1. Determination of INL and DNL in A/D converter test.

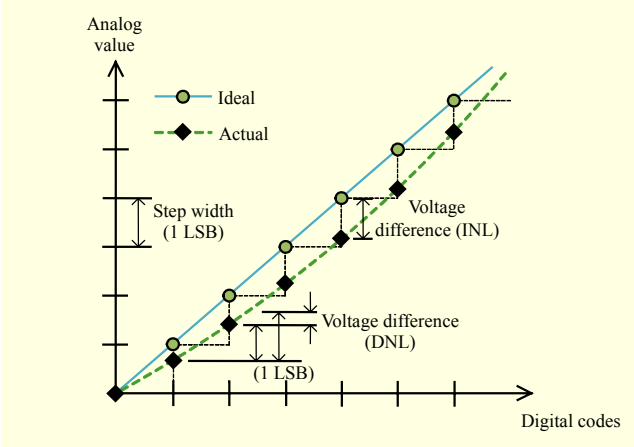

Fig. 2. Determination of INL and DNL in D/A converter test.

shown in Fig. 1 and (1) through (4), the static parameters for an A/D converter test can be derived by detecting the transitions in the test output.

2. D/A Converter Test

In the D/A converter test, we assume that the test input codes are up-count patterns. As illustrated in Fig. 2, the INL test calculates the difference between the ideal and actual outputs of the converter, and the DNL test subtracts 1 LSB from the distance between the consecutive outputs. The equations for the static D/A converter test are shown below.

$$\text{Offset: } -1/2 \text{ LSB} < INL_{DAC}(0) < 1/2 \text{ LSB}, \quad (5)$$

$$\text{Gain: } -1/2 \text{ LSB} < INL_{DAC}(2^m-1) < 1/2 \text{ LSB}, \quad (6)$$

$$\text{INL: } -1/2 \text{ LSB} < INL_{DAC}(i) < 1/2 \text{ LSB}, \quad (7)$$

$$\text{DNL: } -1/2 \text{ LSB} < DNL_{DAC}(i) < 1/2 \text{ LSB}. \quad (8)$$

In (5) through (8), $INL_{DAC}(i)$ indicates the voltage difference between the ideal and actual outputs for the test input i. The first test input is applied when i is "0" (consists of all zeros) and is used in the calculation of the offset. The resolution of the target A/D converter is m. Meanwhile, $DNL_{DAC}(i)$ is calculated by subtracting 1 LSB from the actual distance of the consecutive outputs.

III. Proposed Method

1. A/D Converter Test

In section II, the static parameters to test the A/D converter were explained. If we define the code transition levels $T(k)$, which are the A/D converter input values that cause the output to make transition k, (1) through (4) can be modified as follows.

$$\text{Offset: } T(0) < 1/2 \text{ LSB}, \quad (9)$$

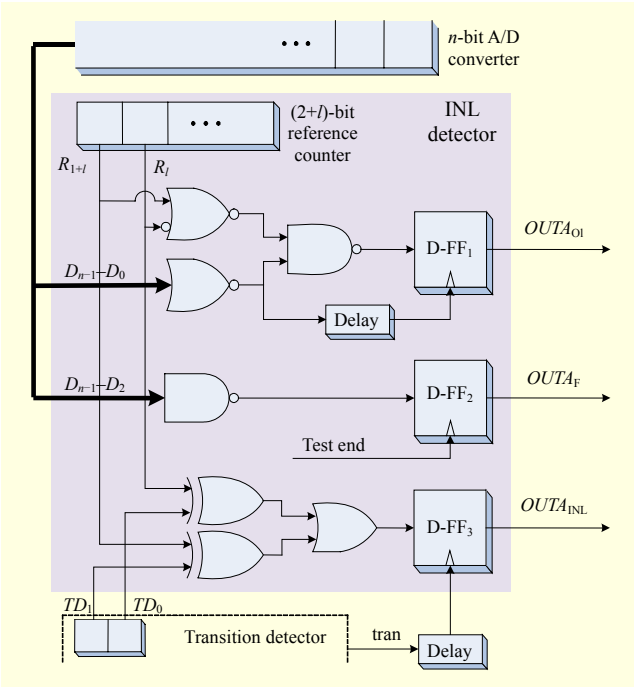

Fig. 3. Modified INL detector in A/D converter test.

$$\text{Gain: } -1/2 \text{ LSB} < T(2^n-1) - T_{IDEAL}(2^n-1) < 1/2 \text{ LSB}, \quad (10)$$

$$\text{INL: } -1/2 \text{ LSB} < T(k) - T_{IDEAL}(k) < 1/2 \text{ LSB}, \quad (11)$$

$$\text{DNL: } -1/2 \text{ LSB} < T(k) - T(k-1) - 1 < 1/2 \text{ LSB}. \quad (12)$$

Here, $T_{IDEAL}(k)$ means the input value to make the k-th transition for an ideal A/D converter. In our assumption, $T_{IDEAL}(k)=k$ LSB because the input signal is a ramp.

In our previous work [11], we proposed a static BIST method to test the A/D converter. The BIST employed four counters to detect transitions, to provide timing references for the INL test, to stabilize the A/D converter output, and to calculate the distance of the transitions. However, to reduce the hardware overhead, the BIST in [11] did not consider the higher bits of the A/D converter output. For example, if the most significant bit of the A/D converter output has a stuck-at fault, it cannot be detected. Considering this, the INL detector in [11] is expanded, as shown in Fig. 3.

As shown in Fig. 3, the offset error is not detected using a "tran" signal because no transition is detected in the transition detector at the test start. In the reference counter, $\{R_{1+l}, R_l\}$ is initialized as {01} because the comparison is made using $\{TD_1, TD_0\}$, the output of the transition detector. In this structure, $\{TD_1, TD_0\}$ and $\{R_{1+l}, R_l\}$ provide the timing of $T(k)$ and $T_{IDEAL}(k)$, respectively. In our assumption, l=1 because the acceptable range is ±1/2 LSB, and R_{l+1} is increased by 1 for each 1/2 LSB. Therefore, the subtraction in (11) is performed by this comparison. For the offset test, R_{1+l} is initialized as "1" because $T(0)$ should not exceed 1/2 LSB, as shown in (9), and

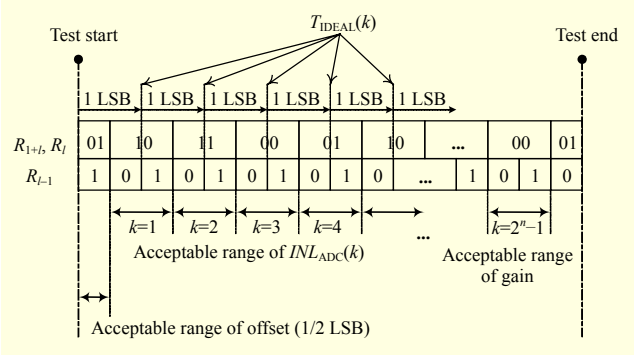

Fig. 4. Timing diagram of offset and INL tests.

(10) can be included in (11) because the test progresses from k=1 to k=2^n–1. The delay time of the input for D-FF_1 is calculated as (the time to pass the 2-input NAND gate) + (the setup time of the D-FF_1). By monitoring the $OUTA_{OI}$ signal, the offset error and the initial output value (D_{n-1}–D_0 = "000…00") can be tested.

In this way, $OUTA_{INL}$ provides the results of the INL test while $OUTA_F$ informs the final output value. The delay time of the input for D-FF_3 is calculated as (the time to pass the 2-input XOR gate) + (the time to pass the 2-input OR gate) + (the setup time of the D-FF_3). The timing diagram of the offset and INL tests are shown in Fig. 4.

The DNL test is performed using the structure in [11]. The distances between the consecutive transitions are measured to calculate (12). After the calculation, $OUTA_{DNL}$ provides the results of the DNL test.

2. D/A Converter Test

In (5) through (8), the four equations to calculate the static parameters for the D/A converter test are introduced. Using (5) through (7), $INL_{DAC}(i)$ can be acquired by subtracting the actual D/A converter output from the ideal one. Furthermore, using (8), $DNL_{DAC}(i)$ is calculated by subtracting the previous D/A converter output from the present one. Therefore, the four equations can be modified as follows:

$$\text{Offset: } -1/2 \text{ LSB} < V_{real}(0) - V_{ideal}(0) < 1/2 \text{ LSB}, \quad (13)$$

$$\text{Gain: } -1/2 \text{ LSB} < V_{real}(2^m-1) - V_{ideal}(2^m-1) < 1/2 \text{ LSB}, \quad (14)$$

$$\text{INL: } -1/2 \text{ LSB} < V_{ideal}(i) - V_{real}(i) < 1/2 \text{ LSB}, \quad (15)$$

$$\text{DNL: } -1/2 \text{ LSB} < V_{real}(i) - V_{real}(i-1) - 1 < 1/2 \text{ LSB}. \quad (16)$$

Equations (13) and (14) can be included in (15) because i ranges from 0 to 2^m–1 for a single cycle of the INL test. Then, (15) and (16) are modified as below to match each side.

$$\text{INL: } 1/2 \text{ LSB} < V_{ideal}(i+1) - V_{real}(i) < 3/2 \text{ LSB}, \quad (17)$$

$$\text{DNL: } 1/2 \text{ LSB} < V_{real}(i) - V_{real}(i-1) < 3/2 \text{ LSB}. \quad (18)$$

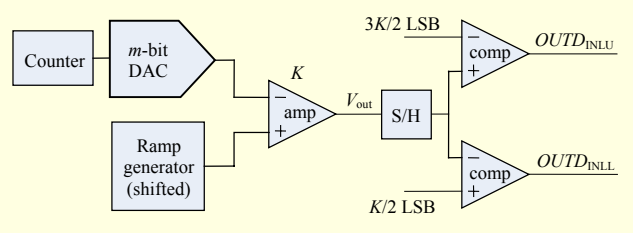

Fig. 5. Circuit for INL test.

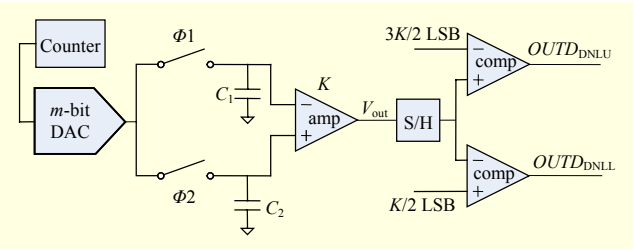

Fig. 6. Circuit for DNL test.

Table 1. Operation of DNL test.

DAC	$V(0)$	$V(1)$		$V(2)$		$V(3)$	
Φ1	Close	Open	Close	Open	Close	Open	Close
C_1	$V(0)$	$V(0)$	$V(1)$	$V(1)$	$V(2)$	$V(2)$	$V(3)$
Φ2	Open	Close	Open	Close	Open	Close	Open
C_2	-	$V(1)$	$V(1)$	$V(2)$	$V(2)$	$V(3)$	$V(3)$

To test a D/A converter with a built-in structure, voltage references are required to judge the actual output. By modifying the static parameter equations, such as (17) and (18), the required number of voltage references is greatly reduced. Now, only two (1/2 and 3/2 LSB) voltage references are required, and the circuits to perform (17) and (18) are shown in Figs. 5 and 6.

In Fig. 5, the ramp signal is shifted by 1 LSB because $V_{ideal}(i+1)$ is used in (17). The amplifier calculates the voltage difference between the shifted ramp and the D/A converter output, and this result is compared with the voltage references to determine the INL error.

In Fig. 6, the switches Φ1 and Φ2 perform cross switching. The opening and closing of the switches comprise one cycle of a test for $DNL_{DAC}(i)$. In the first half, Φ1 is opened and Φ2 is closed; therefore, C_2 holds the present D/A converter output, but C_1 still holds the previous one. In the second half, Φ1 is closed and Φ2 is opened, so that C_1 holds the present D/A converter output for use at the next cycle. The operation of switches and the voltages of the D/A converter output and capacitors are described in Table 1.

In Figs. 5 and 6, the counter and the voltage references can

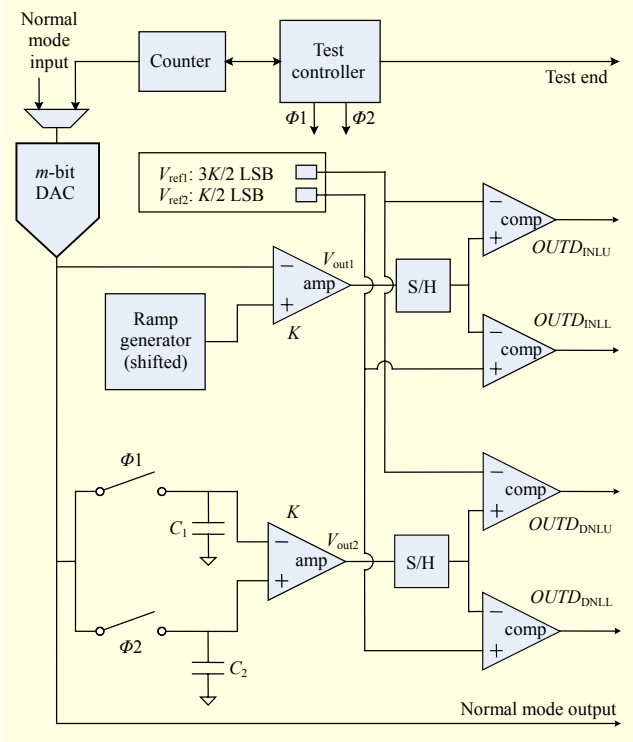

Fig. 7. BIST structure for testing D/A converter.

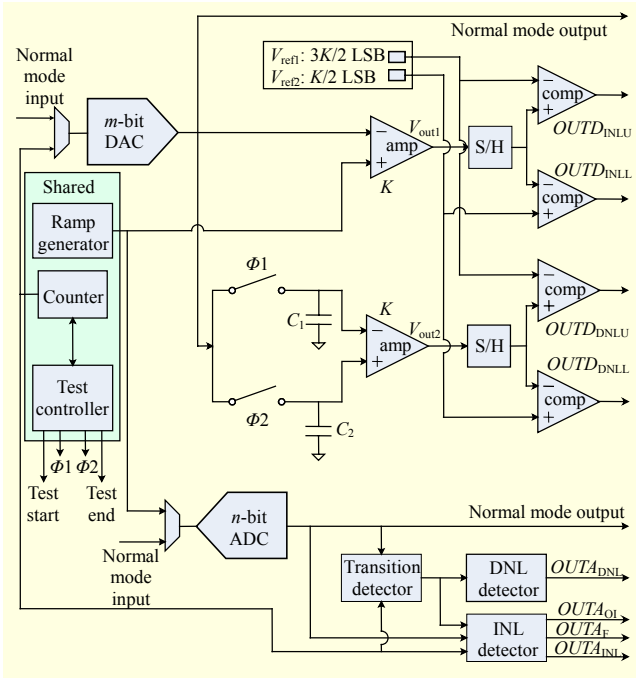

Fig. 8. Combined BIST structure.

be used in common. The amplifier, sample and hold (S/H) circuit, and comparators are also the same, but they cannot be shared due to the parallel test. Thus, the BIST structure for testing whole static parameters can be optimized by sharing the common elements. The BIST structure for testing the D/A converter is shown in Fig. 7.

In Figs. 5 through 7, the voltage differences are amplified K times because the differences are usually too small to use in comparators. After the multiplication, V_{out} is compared with two voltage references, $+K/2$ LSB and $+3K/2$ LSB. The amplifier, comparators, and voltage references can be shared in the INL and DNL tests, and the equations are optimized to reduce the number of voltage references.

3. Simultaneous Test of Converters

In the previous sections, a ramp generator and a counter (several counters in the A/D converter case) were used in common to test A/D or D/A converters. If they are shared in the combined BIST structure, the hardware overhead is reduced. The combined BIST structure for testing A/D and D/A converters is shown in Fig. 8.

In Fig. 8, the counter is used as a transition detector for testing the A/D converter and as a test pattern generator for testing the D/A converter. The size of the counter in the transition detector was 2 bits in [11], but it is extended to n-bit to detect missing codes, which were not considered in [11]. As a result, the transition detector requires the largest counter and is selected as the shared counter. Furthermore, the ramp generator is used as a test input generator for testing the A/D converter and as a voltage reference for testing the D/A converter. For simultaneous testing of both converters, the timing of each test must be arranged to share the use of the counter and the ramp generator. When the target A/D converter is n-bit and the target D/A converter is m-bit, we can consider the four cases as below. (It is assumed that 1 LSB is the same for each test.)

Case 1: $n = m$, $FSR_{ADC} = FSR_{DAC}$

Case 2: $n > m$, $FSR_{ADC} \supset FSR_{DAC}$

Case 3: $n < m$, $FSR_{ADC} \subset FSR_{DAC}$

Case 4: partially overlapped FSR

FSR means the full-scale range of the ramp that is required for each test. For each case, the start/end of the test and the adjustment of the counter are shown in Fig. 9. As shown in Fig. 9, the D/A converter test is delayed by 1 LSB to shift the ramp.

In Case 1, the difference between $\{R_{1+l}, R_l, R_{l-1}\}$ and $\{DIN_1, DIN_0, DIN_a\}$ is 2. (DIN is the test input pattern of the D/A converter, and DIN_a is not used in the test.) Therefore, the counter can be shared if the INL detector is modified. The logic gates to generate $OUTA_{INL}$ in Fig. 3 should be modified to compare $\{TD_1, TD_0\}$ with the shared counter output. After this modification, the shared counter can be used in both tests.

In Case 2, the difference is larger than that of Case 1.

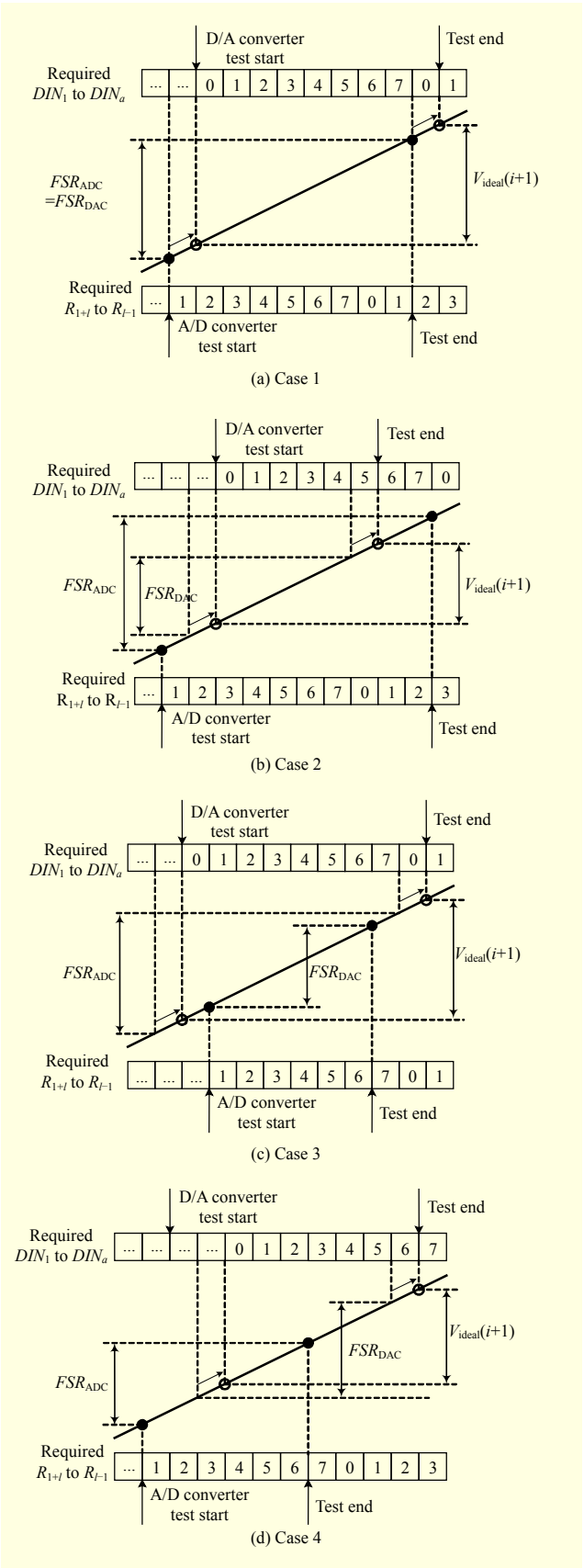

Fig. 9. Timing diagram for each case.

However, the A/D converter test uses a limited number of bits; therefore, the counter also can be shared in both tests with a simple modification of the INL detector. The D/A converter test ends earlier, but this does not affect the test results. In Cases 3 and 4, the order of the test start and end are different from the above cases, but we also can apply the proposed scheme by modifying the logic gates in the INL detector.

As explained above, the proposed BIST can test both A/D and D/A converters simultaneously by sharing the test resources. The proposed method is applicable when the converters use the same system clock and have the same 1 LSB length. In a mixed-signal SoC, the proposed BIST can be applied to reduce both test time and hardware overhead.

IV. Simulation Results

1. Test Setup

To verify the proposed method, simulations with several flash A/D converters and current-steering D/A converters are conducted. They are designed using both HSPICE and Verilog HDL. The four cases in subsection III.3 are considered, and the resolutions of the converters and the analog signal swing ranges are determined for each case. The specifications of the converters for each case are shown in Table 2.

The system clock speed is slowed down to 3.2 MHz because linearity testing must be conducted at a very low speed for some applications, such as communication [6]. The sampling rate is 200 kHz for an 8-bit converter and 100 kHz for a 7-bit converter to have the same time ticks. The acceptable ranges of the tests are ±1/2 LSB; therefore, l=1. The size of the shared counter is determined based on the resolution of the D/A converter (m).

In the D/A converter testing, the amplifier multiplies the voltage differences 128 times (K=128), and the required voltage references, 3K/2 and K/2 LSB, are 1.5 V and 0.5 V,

Table 2. Specifications of converters for each case.

	Case 1	Case 2	Case 3	Case 4
Resolution of ADC, n	8 bit	8 bit	7 bit	7 bit
Resolution of DAC, m	8 bit	7 bit	8 bit	7 bit
FSR_{ADC}	–1 V to 1 V	–1 V to 1 V	–0.5 V to 0.5 V	0 V to 1 V
FSR_{DAC}	–1 V to 1 V	–0.5 V to 0.5 V	–1 V to 1 V	–0.5 V to 0.5 V
1 LSB	$2\ V/2^8 = 1\ V/2^7 = 0.0078125$ V			

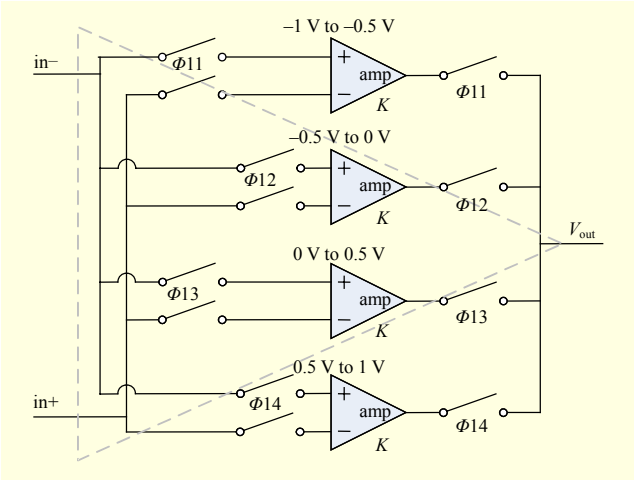

Fig. 10. Divided amplifier structure.

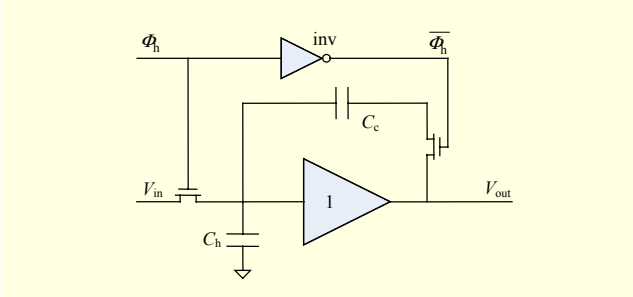

Fig. 11. A holding circuit with clock-feedthrough cancellation.

respectively. The accuracy of these voltage references is very important because the pass/fail decision is made using the references. In our simulation, a CMOS (complementary metal-oxide semiconductor) voltage divider is designed to acquire the voltage references. However, if high-accuracy voltage references can be provided from the outside of the BIST block or the chip, the accuracy of the test will be increased.

In addition, it is not easy to design an amplifier that has a unity gain over the entire FSR_{DAC}. To acquire accurate gain, we divide the amplifier, as shown in Fig. 10. According to the D/A converter output, one amplifier of appropriate voltage range is selected. The offset mismatch of the divided amplifier exists, but the impact on the test result is smaller than the deviation of the gain when using a single amplifier. The control signals $\Phi 11$ through $\Phi 14$ are generated using the test input of the D/A converter. During the test setup, the maximum gain error was set to 5%. In this case, if a voltage difference is 1 LSB+ε (linearity error of the converter), the maximum estimation error at this step is 0.05 LSB+0.05$\varepsilon \approx$ 0.05 LSB when 1 LSB >> ε. With this scheme, the gain error of the combined amplifier is reduced to less than 5%.

As seen in Fig. 6, the switches $\Phi 1$ and $\Phi 2$ perform cross switching during the DNL test for a D/A converter. During the

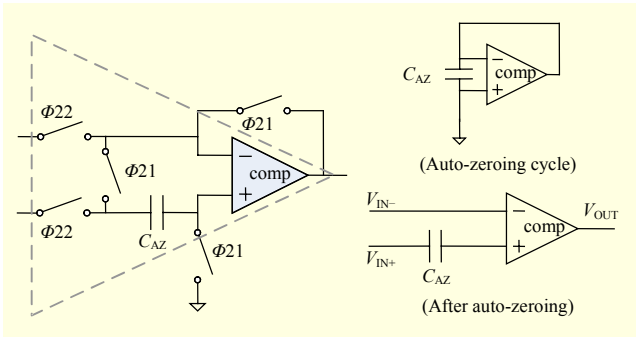

Fig. 12. Comparator offset cancellation scheme.

cross switching, the repetitive closing and opening of the switches results in clock-feedthrough errors, thus decreasing the accuracy of the holding function. To improve the accuracy, we adopt a method proposed in [12] to compensate for the clock-feedthrough error. The improved holding circuit using the method from [12] is shown in Fig. 11. In the modified holding circuit, the compensation capacitor, C_c, cancels the feedthrough charge with a small capacitance of less than 1 pF. Here, C_c is determined by the size of the switches.

In the D/A converter test, the test results are acquired using two comparators, but the offset of the comparators can degrade the accuracy of the test. By amplifying the voltage differences, the effect of the comparators' offset can be reduced. However, to acquire more accurate results, an offset cancellation scheme is employed. The comparator offset cancellation scheme, which uses the auto-zeroing capacitor, is shown in Fig. 12. During the auto-zeroing cycle, $\Phi 21$ are closed and $\Phi 22$ are opened; then, the offset voltage of the comparator is charged in C_{AZ}. After auto-zeroing, $\Phi 22$ are closed and $\Phi 21$ are opened to perform the comparison, as shown in Fig. 12. With this scheme, the inherent offset of the comparator can be canceled.

In the proposed BIST, the ramp signal is used in both the A/D and D/A converter tests. Therefore, the accuracy of the ramp signal affects the accuracy of the overall test. To generate a highly accurate ramp signal, we adopt the ramp generator proposed in [13]. The ramp generator in our BIST should generate a ramp signal of –1 V to 1 V+1 LSB, because $V_{ideal}(i+1)$ is required in the INL test of the D/A converter. The shift of the ramp signal is achieved by delaying the start of the INL test of the D/A converter. The ramp generator scheme in [13] is used in the HSPICE simulation of our BIST, and the INL error of the ramp is several tens of microvolts.

Several schemes are introduced to increase the accuracy of the proposed method, but they also increase the hardware overhead of the BIST. There is a trade-off between test accuracy and hardware overhead, and the issues that affect test accuracy must also be considered in the existing simultaneous test methods. The proposed BIST makes efforts to reduce the

hardware overhead by sharing elements and optimizing test schemes and therefore has a margin to employ the methods for increasing the test accuracy. With these methods, we make a simulation using an ideal D/A converter and ramp signal to measure the performance of the BIST circuit. The maximum error of the output of the S/H in Figs. 5 and 6 is 0.018 LSB and 0.027 LSB, respectively. In addition, the maximum error (offset) of the comparator is 0.004 LSB.

2. Static Test

The simulation of the proposed BIST is made using Verilog HDL and HSPICE. The simulation environments were introduced in subsection IV.1, and we vary the resistors in the A/D converter and the current sources in the D/A converter for the four cases. After the simulation, $OUTA_{OI}$, $OUTA_{F}$, $OUTA_{INL}$, $OUTA_{DNL}$, $OUTD_{INLU}$, $OUTD_{INLL}$, $OUTD_{DNLU}$, and $OUTD_{DNLL}$ signals of each case are observed.

The simulation results of the A/D converter test are shown in Fig. 13. The respective inserted nonlinearity for the four cases is shown at the top of each figure; it is calculated ideally using MATLAB. The simulation results are shown at the bottom of each figure, and the detected errors are counted. Fig. 13(a) is the sum of $OUTA_{OI}$ and $OUTA_{INL}$, and Fig. 13(b) shows $OUTA_{DNL}$. As shown in the figures, the number of linearity errors violating the acceptable range agrees with the ideal number.

The simulation results of the D/A converter test are shown in Fig. 14. As in Fig. 13, Fig. 14 gives the ideal and the simulation results. Fig. 14(a) shows $OUTD_{INLU}$ and $OUTD_{INLL}$, and Fig. 14(b) shows $OUTD_{DNLU}$ and $OUTD_{DNLL}$. In the D/A converter test, $OUTD_{INLU}$ and $OUTD_{DNLU}$ check the upper

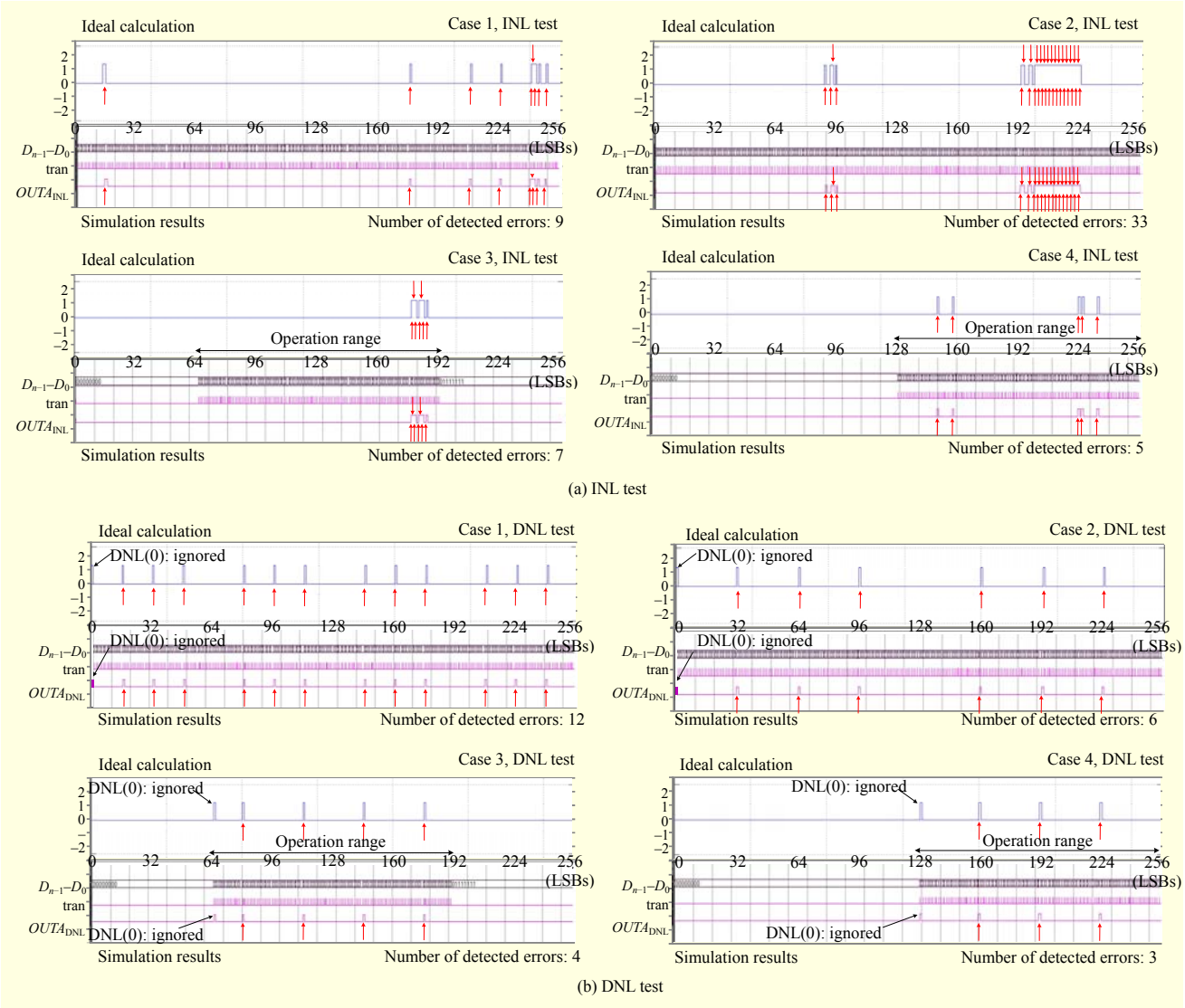

Fig. 13. Simulation results of A/D converter test.

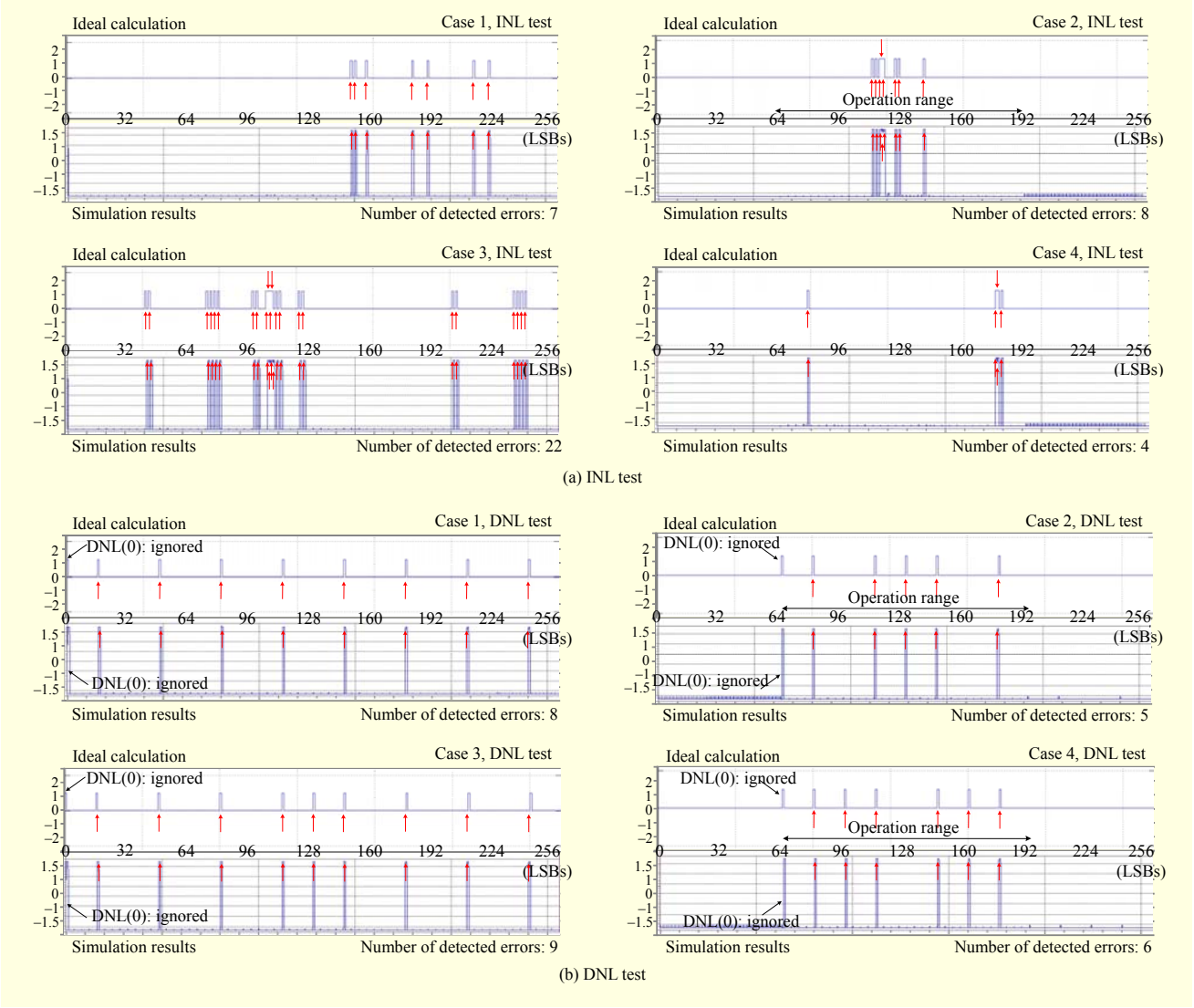

Fig. 14. Simulation results of D/A converter test.

bound of the acceptable range, while $OUTD_{INLL}$ and $OUTD_{DNLL}$ check the lower bound. Therefore, the sum of the number of detected errors in $OUTD_{INLU}$ and $OUTD_{INLL}$ indicates the detected INL errors, and the sum in $OUTD_{DNLU}$ and $OUTD_{DNLL}$ indicates the detected DNL errors. The number of detected errors also agrees with the ideal number, as shown in Fig. 13.

As shown in Figs. 13 and 14, the proposed BIST can test static parameters of A/D and D/A converters by monitoring the output signals. If all output signals are always "low" throughout the test, the A/D and D/A converters under test are fault-free and do not violate the acceptable range.

3. Discussion

The proposed BIST can detect static errors by monitoring the output signals. In a single iteration of the ramp and the shared counter, four static parameters for both A/D and D/A converters are tested. This simultaneous testing is made by sharing the common element and optimizing the test schemes.

The proposed method is verified with Verilog HDL and HSPICE simulations because the converters are regarded as black boxes performing converting functions. The BIST determines "pass" or "fail" using only the output of the converters.

The greatest strength of the proposed method is the reduced test time. The static linearity testing requires many test samples and a long test time. Therefore, if the test time of a single execution is shortened, the total test time is greatly reduced. Table 3 shows a summarized comparison of A/D and D/A converter BIST methods. The proposed BIST may require more hardware overhead than the loopback BISTs

Table 3. Comparison of A/D and D/A converter BIST methods.

	Hardware overhead	Test time	Requirements
[5]	Small	Long	High quality of noise
[6]	Small	Long	Large number of test samples
[7]	Medium	Medium	Modification of DUT
[8]	Medium	Short	Many voltage references
[9]	Large	Short	Accurate analog elements
Proposed	Medium	Shortest	Accurate analog elements

[5]-[7], but the test time of the proposed BIST is shortest and the proposed BIST does not need to address the fault masking problem. Compared to [8] and [9], the proposed BIST accomplishes the static test of A/D and D/A converters with a simple circuitry.

The proposed method performs tests by monitoring only the output of the converters. The shared counter and the analyzer for the A/D converter consist of all digital elements, and the ramp signal generator is adopted from the previous work and the performance is already proven [13]. The analyzer for the D/A converter employs several schemes; therefore, the possibility for error during the self-test is minimized.

Nevertheless, the proposed method has some limitations. The accuracy of the analog elements, including the ramp generator, should be guaranteed. The mismatch of the elements can be attenuated by calibration. The proposed method will be developed into BISC and implemented on a chip as our future work.

Consequently, the speediness and simplicity of the proposed BIST may make the method more suitable for testing embedded converters.

V. Conclusion

On-chip static linearity testing of A/D and D/A converters is a difficult task because it is one of the most time-consuming tests and additional on-chip analog circuitry is required. Nowadays, due to the expensive costs for testing A/D and D/A converters, a new cost-effective test method is needed. BIST can be a solution, especially in SoC or SiP environments.

This paper presented a new BIST method for static testing of A/D and D/A converters. The static parameters to be tested were optimized for each converter, and the BIST elements for testing each converter were reduced. Furthermore, the common BIST elements that are used in both A/D and D/A converter testing were shared to reduce hardware overhead. Compared with the conventional method, the proposed method requires simpler circuitry while achieving simultaneous testing of A/D and D/A converters. As a result, the proposed method is expected to reduce the test time significantly, with easy BIST application. The simulation results show that the proposed BIST can detect static errors of A/D and D/A converters simultaneously for various specifications of converters.

References

[1] M. Kim et al., "A 3 V 12b 100 MS/s CMOS D/A Converter for High-Speed Communication Systems," *JSTS*, vol. 3, no. 4, Dec. 2003, pp. 211-216.

[2] *The International Technology Roadmap for Semiconductors* (ITRS), 2007 ed. Available: http://www.itrs.net/Links/2007ITRS/Home2007.htm

[3] J. Ryu and S. Noh, "A New Approach for Built-in Self-Test of 4.5 to 5.5 GHz Low-Noise Amplifiers," *ETRI J.*, vol. 28, no. 3, June 2006, pp. 355-363.

[4] M. Burns and G.W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*, New York: Oxford University Press, 2001.

[5] J. Chun, H. Yu, and J. Abraham, "An Efficient Linearity Test for On-Chip High Speed ADC and DAC Using Loop-back," *Proc. ACM GLSVLSI*, Apr. 2004, pp. 328-331.

[6] H. Shin, J. Park, and J. Abraham, "A Statistical Digital Equalizer for Loopback-Based Linearity Test of Data Converters," *Proc. ATS*, Nov. 2006, pp. 245-250.

[7] X. Huang and J. Huang, "An ADC/DAC Loopback Testing Methodology by DAC Output Offsetting and Scaling," *Proc. VTS*, Apr. 2010, pp. 289-294.

[8] K. Arabi and M. Sawan, "On Chip Testing Data Converters Using Static Parameters," *IEEE T VLSI Syst.*, vol. 6, no. 3, Sept. 1998, pp. 409-419.

[9] J. Huang, C. Ong, and K. Cheng, "A BIST Scheme for On-Chip ADC and DAC Testing," *Proc. DATE*, Mar. 2000, pp. 216-220.

[10] Y. Wen, "A BIST Scheme for Testing Analog-to-Digital Converters with Digital Response Analyses," *Proc. VTS*, May 2005, pp. 383-388.

[11] I. Kim et al., "A New Analog-to-Digital Converter BIST Considering a Transient Zone," *IEICE T Electron.*, vol. E90-C, no. 11, Nov. 2007, pp. 2161-2163.

[12] K. Watanabe and S. Ogawa, "Clock-Feedthrough Compensated Sample/Hold Circuits," *Electron. Lett.*, vol. 24, no. 19, Sept. 1998, pp. 1226-1228.

[13] W. Lee et al., "A High Precision Ramp Generator for Low Cost ADC Test," *Proc. ICSICT*, Oct. 2008, pp. 2103-2106.

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