Fine-Pitch Solder on Pad Process for Microbump Interconnection

Hyun-Cheol Bae, Haksun Lee, Kwang-Seong Choi, and Yong-Sung Eom

A cost-effective and simple solder on pad (SoP) process is proposed for a fine-pitch microbump interconnection. A novel solder bump maker (SBM) material is applied to form a 60-μm pitch SoP. SBM, which is composed of ternary Sn3.0Ag0.5Cu (SAC305) solder powder and a polymer resin, is a paste material used to perform a fine-pitch SoP through a screen printing method. By optimizing the volumetric ratio of the resin, deoxidizing agent, and SAC305 solder powder, the oxide layers on the solder powder and Cu pads are successfully removed during the bumping process without additional treatment or equipment. Test vehicles with a daisy chain pattern are fabricated to develop the fine-pitch SoP process and evaluate the fine-pitch interconnection. The fabricated Si chip has 6,724 bumps with a 45-μm diameter and 60-μm pitch. The chip is flip chip bonded with a Si substrate using an underfill material with fluxing features. Using the fluxing underfill material is advantageous since it eliminates the flux cleaning process and capillary flow process of the underfill. The optimized bonding process is validated through an electrical characterization of the daisy chain pattern. This work is the first report on a successful operation of a fine-pitch SoP and microbump interconnection using a screen printing process.

Keywords: Solder on pad, SoP, fine-pitch bumping, maskless bumping, Sn3.0Ag0.5Cu, SAC305, microbump interconnection.

I. Introduction

Portable electronic devices are currently driving the growth of three-dimensional (3D) system in package (SiP) technologies. Such 3D SiP technologies offer an opportunity for more complexity, increased system performance, and multifunctional portable applications. A fine-pitch microbump interconnection was developed to increase the performance and improve the interconnection density. A Cu pillar bump with a SnAg solder cap using an electroplating process is mainly used to form a fine-pitch microbump [1], [2]. In the electroplating process for a microbump, it is very hard to obtain a Sn3.0Ag0.5Cu (SAC305) solder cap. Therefore, a cost-effective SAC305 solder on pad (SoP) process using screen printing is a very attractive option.

In addition, the flux and underfill materials are the most critical components for a reliable flip chip bonding process using microbumps. Regarding the process of applying the flux, however, there is the issue of cleaning off the flux residue after the flip chip bonding process. The flux residue is unfavorable for following an underfill dispensing process and can further create a long-term reliability issue. Therefore, the development of a flip chip bonding process without the usage of a flux for the joining of the microbumps is required.

In this letter, the first report of a fine-pitch SoP process for a microbump interconnection is presented. This fine-pitch SAC305 SoP process is developed using a maskless screen printing process.

II. Experiment

Since the microbump interconnection needs a fine-pitch and low-volume solder bump, a novel maskless solder bump maker (SBM) was developed [3]-[8]. The SBM, which is composed of solder powder and a polymer resin, is the material used to paste or bind the solder bump on a given substrate. In particular,

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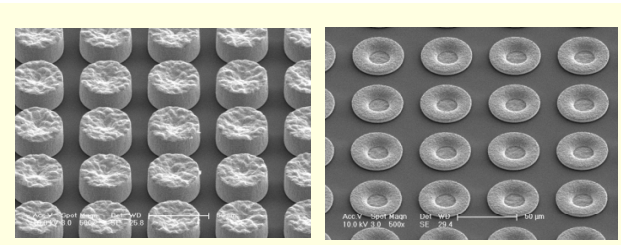


(a) (b)

Fig. 1. SEM images of daisy chain test vehicle: (a) fabricated Si chip with Cu pillars and (b) fabricated Si substrate with UBM.

the polymer resin for the SBM removes the oxide layers existing on the surface of the solder powder and Cu pad during the bumping process. In this work, SAC305 powdered solder is blended with the resin. The specifications of the distribution of the solder diameters for types 7 and 8 are according to the standard [6]: 2 μm to 11 μm and 2 μm to 8 μm with weight percentages of 90% for types 7 and 8, respectively.

The type 8 solder powder was newly adopted, as previous research established that the type 7 solder powder is usually used because the minimum bump pitch is more than 130 μm [7]-[9]. Using a numerical estimation, the number of solder particles placed on the Cu pad area is calculated. When type 7 solder powder is used, 48 solder particles can be placed on a Cu pad with a diameter of 45 μm. Similarly, for type 8, 81 solder particles can be placed on the same pad area.

The volumetric mixing ratio between the polymer resin and SAC305 solder powder is 86:14. The mixing ratio is analyzed to establish a proper interaction between the solder powder and Cu pads and optimized fully to fill the Cu pads.

Test vehicles are fabricated to develop the fine-pitch SoP process using SBM material and a screen printing process. For the demonstration, a Si chip and substrate are fabricated with a daisy chain pattern. A 7 mm × 7 mm Si chip is fabricated with 6,724 Cu pillars, each of which has a pitch of 60 μm. Each Cu pillar has a diameter of 45 μm and height of 30 μm, as shown in Fig. 1(a). Moreover, a Si substrate having the same number of Cu pads is also fabricated to form a 60-μm-pitch SoP, as shown in Fig. 1(b). The used Cu pads have a 5-μm TiW/Cu under bump metallization (UBM) layer, which has a diameter of 45 μm.

Figure 2 shows the entire bumping process for the fine-pitch SoP process. SBM material is printed on the Si substrate, and the printed area and thickness are controlled by a guide. This guide is not a patterned mask, as opposed to a photoresist mask or a metal mask, which defines the open areas or separates the microbumps. The reflow process is performed at 270ºC for 40 seconds in an IR oven. After the reflow process, the residue resin and solder particles are cleaned off in ultrasonic baths of MIF, acetone, and methanol for several minutes. While

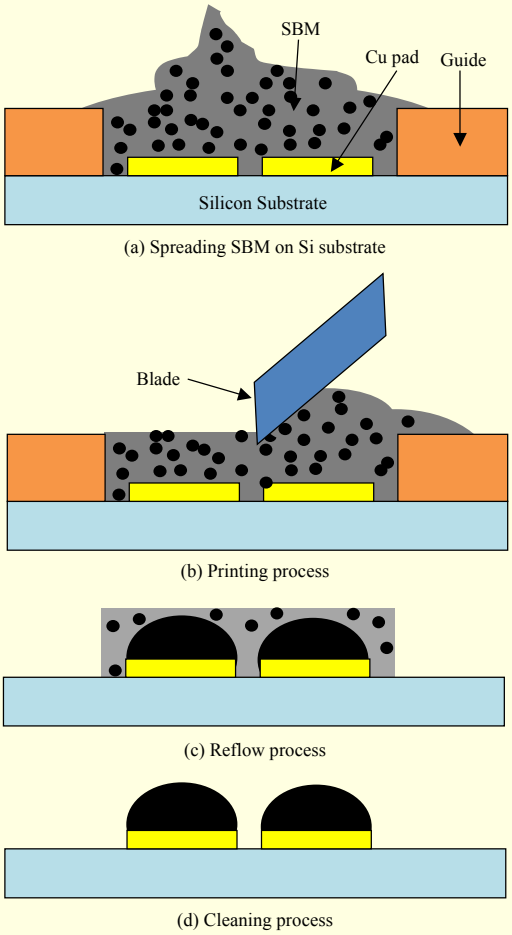


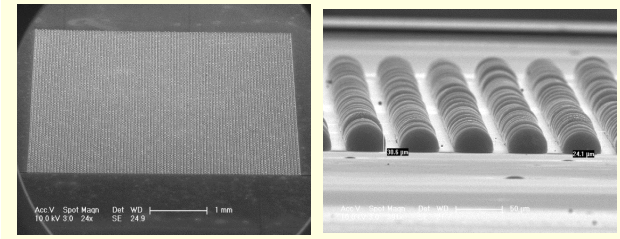
Fig. 2. Process flow of fine pitch SoP using screen printing.

previous works required such processes as a second resin printing, cleaning, and coining, the proposed SoP process does not require such processes [7], [8].

The test vehicles are flip chip bonded, and the bonding process flow is very simple. To begin with, a developed fluxing underfill, which does not require a cleaning step, is applied to the Si substrate. The fluxing underfill material is a non-flow underfill. In this material, deoxidizing agents together with a hardener are added to the underfill to form an epoxy-based thermoset. The Si chip with the Cu pillar bumps is then aligned to the Si substrate with SoP, and the solder joints are all formed simultaneously using thermocompression bonding. During the flip chip bonding, additional flux cleaning and capillary actions are not required. The optimized bumping and interconnection processes are validated by an electrical characterization of the daisy chain patterned test vehicles.

III. Results and Discussion

Figure 3 shows the scanning electron microscope (SEM)



(a) (b)

Fig. 3. SEM images: (a) fully formed SAC SoP on 6725 Cu pads and (b) magnification of (a).

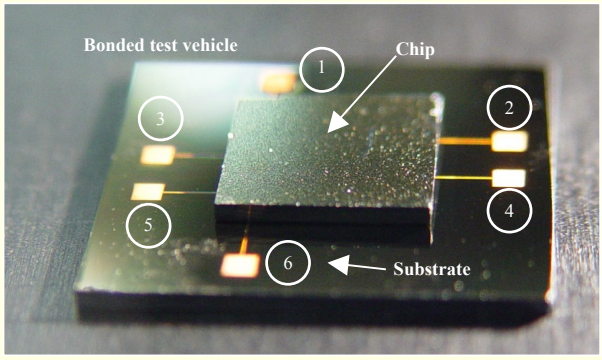
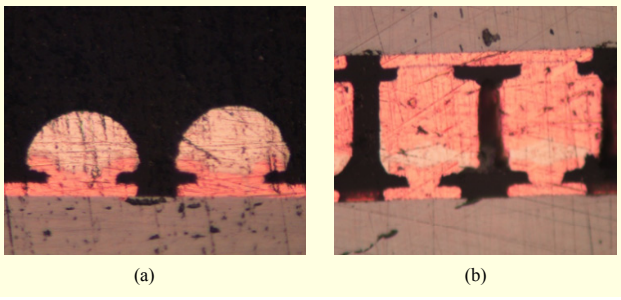


Fig. 4. Photograph of flip chip bonded test vehicle.



(a) (b)

Fig. 5. Cross-sectional images of Si substrate: (a) before and (b) after flip chip bonding process.

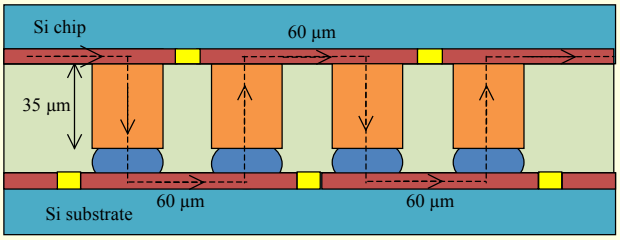


Fig. 6. Schematic of DC resistance calculation of daisy chain patterned test vehicles.

images of the formed fine-pitch SoP array on the Si substrate. As shown in Fig. 3(a), the 60-μm-pitch SoP is well formed on the UBM layers with uniform shapes. In addition, all 6,724 Cu pads are fully filled without any missing bumps. No solder bridges, which are easily formed using a maskless printing process, are found in the fabricated fine-pitch SoP array.

Figure 4 shows a photograph of the flip chip bonded test vehicle. The fabricated Si chip and substrate are well bonded with the developed fluxing underfill material [10]-[13]. First, fluxing underfill is dispensed onto the Si substrate and preheated at 120ºC for 10 seconds. Next, the pressure of 200 gf is applied onto the joint while the temperature is set to 250ºC for 20 seconds.

The fine-pitch interconnections between the Cu pillars and SoP is checked using two quick analysis methods. One is the cross-section inspection of the bonded chip and substrate, as shown in Figs. 5(a) and 5(b). Figures 5(a) and 5(b) show the cross-sectional views of the SoP and Cu pillar interconnections before and after the bonding process. From the cross-section inspection, the bump shape and height information of SoP obtained through an SEM visual inspection are verified. Cu pillars and SoP are properly interconnected without an alignment issue. Electrical defects commonly occur in fine-pitch bonding when the adjacent bumps make an electrical short effect or when an insufficient volume of solder creates an electrical opening effect. However, no such electrical defects are found in these fine-pitch Cu pillar bump interconnections.

The other method used to check the fine-pitch interconnection is to compare the calculated and measured resistance values of the test vehicles with the daisy chain patterns, as shown in Figs. 4 and 6. The bonded test vehicles are designed to connect all of the bumps and have six DC probing pads. In detail, a total of 6,724 bump interconnections are checked by probing the top and bottom pads, marked as "1" and "6," respectively. The right and left pads are designed to inspect the internal bump opening and shorting effects. If the test vehicles are well bonded, the DC resistance values will show an increasing tendency as the section goes from 1-2 to 1-6. The simple DC resistance values can be calculated with (1).

$$R_{\mathrm{TOTAL}} = \rho \times \frac{L}{A}. \quad (1)$$

Here, R_{TOTAL} is the total sum of the resistance values, ρ is the resistivity of the metal and solder, L is the length, and A is the cross-sectional area. The resistance values of the redistribution layer (RDL) of a Si chip, the interconnection bumps between the chip and substrate, and the RDL of the Si substrate are included in R_{TOTAL}. Values L and A respectively represent the length and area of all interconnection paths. The calculated and measured DC resistance values of the test vehicle, reflecting 6,724 bump interconnections, are summarized in Table 1. The comparison results clearly show that the interconnections of the

Table 1. Comparison of DC resistance values between calculated results and measured data.

Section	Measured resistance (Ω)	Total measured resistance (Ω)	Total calculated resistance (Ω)
1-2	6.0	36.8	32.3
1-3	17.3		
1-4	24.6		
1-5	31.1		
1-6	36.8		

Cu pillars and SoP are successful. These measured DC resistance values have some variations in the contact resistance.

IV. Conclusion

A fine-pitch solder on pad (SoP) process using a screen printing process was newly presented and successfully developed by optimizing the volumetric mixing ratio between a resin and Sn3.0Ag0.5Cu solder powder. Test vehicles with a daisy chain pattern were fabricated to evaluate the presented SoP technology and the simple interconnection process using a fluxing underfill material. Based on the cross-section images and DC resistance measurement data, the effectiveness of the presented bumping technology and fine-pitch microbump interconnection were verified. Because of the simplicity and cost-effectiveness of the process, SoP technology may be used instead of a solder cap process with electroplating. As a future work, the reliability test for this process will be applied.

References

[1] A. Yu et al., "Fabrication of High Aspect Ratio TSV and Assembly with Fine-Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects," *IEEE Trans. Comp. Packag. Manufact. Technol.*, vol. 1, no. 9, Sept. 2011, pp. 1336-1344.

[2] Y. Orii et al., "Ultrafine-Pitch C2 Flip Chip Interconnections with Solder-Capped Cu Pillar Bumps," *Proc. Electron. Comp. Technol. Conf.*, 2009, pp. 948-953.

[3] K.-S. Choi et al., "Novel Maskless Bumping Material for 3D Integration," *ETRI J.*, vol. 32, no. 2, Apr. 2010, pp. 342-344.

[4] K.-S. Choi et al., "Novel Bumping Material for Solder-on-Pad Technology," *ETRI J.*, vol. 33, no. 4, Aug. 2011, pp. 637-640.

[5] Y.-S. Eom et al., "Characterization of a Hybrid Cu Paste as an Isotropic Conductive Adhesive," *ETRI J.*, vol. 33, no. 6, Dec. 2011, pp. 864-870.

[6] IPC Std. J-STD-005, "Requirements for Soldering Pastes."

[7] K.-J. Sung et al., "Novel Bumping and Underfill Technologies for 3D IC Integration," *ETRI J.*, vol. 34, no. 5, Oct. 2012, pp. 706-712.

[8] K.-S. Choi et al., "Novel Bumping Process for Solder on Pad Technology," *ETRI J.*, vol. 35, no. 2, Apr. 2013, pp. 340-343.

[9] Y.-S. Eom et al., "Optimization of Material and Process for Fine Pitch LVSoP Technology," *ETRI J.*, vol. 35, no. 4, Aug. 2013, pp. 625-631.

[10] Y.-S. Eom et al. "Characterization of Polymer Matrix and Low Melting Point Solder for Anisotropic Conductive Film," *Microelectron. Eng.*, vol. 85, 2008, pp. 327-331.

[11] J.-W. Baek et al., "Chemo-rheological Characteristic of a Self-Assembling Anisotropic Conductive Adhesive System Containing a Low-Melting Point Solder," *Microelectron. Eng.*, vol. 87, 2010, pp. 1968-1972.

[12] K.-S. Jang et al., "Catalytic Behavior of Sn/Bi Metal Powder in Anhydride-Based Epoxy Curing," *J. Nanosci. Nanotechnol.*, vol. 9, no. 12, 2009, pp. 7461-7466.

[13] Y.-S. Eom et al., "Electrical Interconnection with a Smart ACA Composed of Fluxing Polymer and Solder Powder," *ETRI J.*, vol. 32, no. 3, June 2010, pp. 414-421.