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Thermal Model for Power Converters Based on Thermal Impedance

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Abstract

In this paper, the superposition principle of a heat sink temperature rise is verified based on the mathematical model of a plate-fin heat sink with two mounted heat sources. According to this, the distributed coupling thermal impedance matrix for a heat sink with multiple devices is present, and the equations for calculating the device transient junction temperatures are given. Then methods to extract the heat sink thermal impedance matrix and to measure the Epoxy Molding Compound (EMC) surface temperature of the power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) instead of the junction temperature or device case temperature are proposed. The new thermal impedance model for the power converters in Switched Reluctance Motor (SRM) drivers is implemented in MATLAB/Simulink. The obtained simulation results are validated with experimental results. Compared with the Finite Element Method (FEM) thermal model and the traditional thermal impedance model, the proposed thermal model can provide a high simulation speed with a high accuracy. Finally, the temperature rise distributions of a power converter with two control strategies, the maximum junction temperature rise, the transient temperature rise characteristics, and the thermal coupling effect are discussed.

Key words: Finite Element Method (FEM), Power converter, Temperature rise, Thermal impedance, Superposition principle, Switched Reluctance Motor (SRM)

I. INTRODUCTION

With the advantages of a firm structure, easy design, low cost, and high fault-tolerant ability, the Switched Reluctance Motor (SRM) system is used under many circumstances such as in coal mines, electric vehicles, high–speed drives and so on [1]-[7]. The power converter as the system central actuator has a number of power devices which generate a considerable amount of heat from dissipated power [8], [9]. If the device chips exceed their maximum junction temperature they can easily fail. Therefore, it is necessary to establish a thermal model to compute the power converter temperature distribution and the device junction temperatures for design and application.

Many papers can be found dealing with methods for developing a thermal model of power electronics packages. Firstly, traditional R-C networks as thermal equivalent circuits have been used to simulate stationary and transient behaviors [10]-[14]. This lumped-element model is simple and is always used for electrical equipment thermal design. The resistances and capacitances in networks can be extracted from the physical properties [10], [11] or from fitting the thermal impedance curves derived from a FEM simulation or measured curves [12], [13]. This method is wildly used to calculate the junction temperatures of power semiconductor devices and it can be easily implemented into a circuit simulator such as PSpice or Saber [14]. Secondly, the finite element methods (FEM) [8], [12] or finite difference methods (FDM) [15] have been adopted to provide high precision results in industry applications. However, they have a long calculation time, high hardware requirements and very complicated models. In addition they demand experienced engineers. The last method is the Fourier series method using the Fourier series expansion to solve the heat diffusion equation. However, this is based on package system materials and physical dimensions [16], [17].

The above methods only focus on device packages modeling, while regarding the heat sink as ideal. As a result, the entire power electronics system needs to be built including the actual cooling equipment [18]. This can be solved by using commercial FEM software, for example, ANSYS or FLUX. However, they are limited to calculating transient problems due to the long simulation times. In addition, they cannot be

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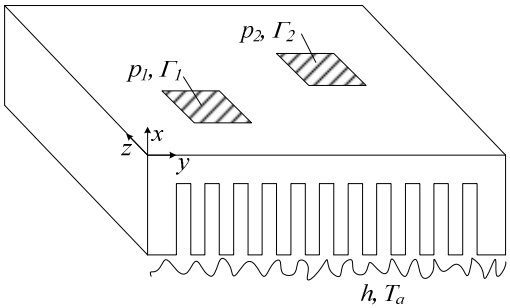


Fig. 1. Schematic of the heat sink with two heat sources under the air-cooling condition.

implemented in a circuit simulator. Moreover, it is difficult for application engineers to gain the inner dimension and material parameters of the devices. This information is important for FEM simulations and the Fourier series method. However, device datasheets always provide a transient thermal impedance curve for the device junction temperature. Therefore, it is possible to obtain the device thermal impedance model and then expand it to the heat sink. The system thermal impedance can consists of the IGBT thermal impedance and the heat sink thermal impedance [13]. With multiple-chip modules such as IGBT power modules it is necessary to consider the thermal spreading resistance [19] and the thermal coupling effect [20], [21]. The thermal impedance matrix is proposed to solve this problem [21], but it cannot be applied to multiple devices with a practical heat sink, and the application conditions are not taken into account.

In this paper, the temperature rise modeling of the power converters in SRM drives is given base on the device thermal impedance and the heat sink thermal impedance matrix. Then methods to measure the Epoxy Molding Compound (EMC) surface temperature of the power Metal Oxide Semiconductor Field Effect Transistors (MOSFET) instead of the junction temperature and the case temperature are proposed. Finally, the temperature rise distributions of power converters with two control strategies, the highest junction temperature rise, the characteristic of the temperature rise curve and the thermal coupling effect are discussed based on simulated and experimental results.

II. Mathematical Model and Temperature Rise Superposition

Fig.1 shows an air-cooling heat sink model, which has a typical plate-fin structure with two heat sources mounted on the base. The following assumptions based on experiences can simplify the problem to obtain reasonably accurate answers. With reference to Fig.1, the following are assumed.

1) All of the materials are thermally homogeneous and isotropic.

2) The thermal properties of the structure are independent of temperature.

3) The devices and the heat sink are in intimate contact. That is, the thermal contact resistance is zero.

4) The base surfaces are adiabatic except for the areas the heating devices are on.

5) The heat radiation is negligible.

6) The initial temperature of the heat sink is equal to the ambient temperature, and the ambient temperature is independent of time.

The temperature rise of the heat sink is defined as:

$$\theta = T - T_a \tag{1}$$

Where T is the heat sink temperature, T_a is the ambient temperature, and θ is the heat sink temperature rise.

The heat conduction equation of the heat sink in the Cartesian coordinate system is given bellow:

$$\nabla^2\theta - \frac{1}{\lambda / \rho c}\frac{\partial\theta}{\partial t} = 0 \tag{2}$$

Where λ [W/(m·℃)] is the heat sink thermal conductivity, ρ [kg/m3] is the heat sink density, c [J/(kg·℃)] is the specific heat capacity, and t [s] is the time.

The heat source area Γ_1 satisfies the temperature continuation:

$$\theta_d = \theta \tag{3}$$

Where θ_d is the device temperature rise.

It also meets the heat flux density continuation:

$$-\lambda\left.\frac{\partial\theta}{\partial z}\right|_{z=0} = p_1 \tag{4}$$

Where p_1 [W/m^2] is the heating power density.

In the same way, the heat source area Γ_2 also satisfies the temperature continuation and the heat flux density continuation.

The surface of the fins satisfies a convective boundary condition, given by:

$$-\lambda\left.\frac{\partial\theta}{\partial z}\right|_{z=0} = h\theta \tag{5}$$

Where h [W/(m^2·℃)] is the convection heat transfer coefficient that can be applied to the forced air-cooling condition and natural air-cooling condition.

Equations (1)-(5) are the heat transfer equations to calculate the temperature distribution of the heat sink heated by two sources. In the same way, the equations for a heat sink with individual heat sources can also be written. By comparing these three equations sets without solving them, it can be seen that the temperature rise of the heat sink with two heat sources is the sum of that with single heat sources separately. That is, the heat sink temperature rise but not the heat sink temperature satisfies the superposition principle under the proposed assumptions. Therefore, the temperature rise of the heat sink with multiple discrete heat sources can be expressed as:

$$\theta = \sum_{m=1}^{n}\theta_m \tag{6}$$

Where θ_m is the heat sink temperature rise heated by the mth heat source alone, n is the number of the sources, and θ is the heat sink temperature rise with n heat sources.

III. HEAT SINK THERMAL IMPEDANCE AND THE JUNCTION TEMPERATURE CALCULATION

The heat conduction equation without any heat sources has the same form as the transmission line equation with no inductance or leakage conductance. Therefore, the heat transfer phenomenon can be simulated by an equivalent circuit composed by resistances and capacitances, such as the Foster network or the Cauer network. The parameters of the Foster network are easy to derive while the Cauer network describes the physical properties correctly.

A heat source in different locations on the heat sink has different thermal impedance, and thermal coupling exists between all of the sources. A heat-sink lumped thermal impedance that ignores this distribution and the thermal coupling deviates from reality. Therefore, it is essential to use the distributed coupling thermal impedance for the heat sink.

If Γ_m is the heat sink base surface in contact with the mth device, then the transient temperature rise of Γ_m is:

$$\theta_{m\_sa} = \sum_{i=1}^{n} Z_{mi} p_i \tag{7}$$

Where p_i [W] is the heat flux on the heat sink surface Γ_m which is generated from the ith device; Z_{mi} refers to the impact of the ith device on the mth device; when $i=m$, Z_{mi} [℃/W] represents the self-heating thermal impedance; and when $i\neq m$, Z_{mi} [℃/W] represents the mutual-heating thermal impedance.

Therefore, the distributed coupling thermal impedance matrix for a heat sink with n devices can be defined as:

$$\boldsymbol{Z}_{n\times n} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & Z_{23} & \cdots & Z_{2n} \\ Z_{31} & Z_{32} & Z_{33} & \cdots & Z_{3n} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ Z_{n1} & Z_{n2} & Z_{n3} & \cdots & Z_{nn} \end{bmatrix}_{n\times n} \tag{8}$$

If the device location and the convective heat transfer coefficient are fixed, the distributed coupling thermal impedance matrix of the heat sink is also fixed.

The transient junction temperature of the mth device is given by:

$$\begin{aligned} T_{m\_j} &= \theta_{m\_j} + T_a \\ &= \theta_{m\_jc} + \theta_{m\_cs} + \theta_{m\_sa} + T_a \end{aligned} \tag{9}$$

Where θ_{m_j} is the junction temperature rise of the mth device, θ_{m_jc} is the temperature rise from the junction to the case, θ_{m_cs} is the temperature rise from the case to the heat sink, and θ_{m_sa} is the temperature rise from the heat sink to the ambient, which is the temperature rise of Γ_m.

The device transient temperature rise is give as:

$$\theta_{m\_jc} = Z_{m\_jc} p_{m\_j} \tag{10}$$

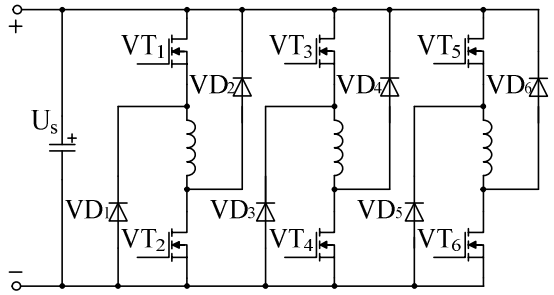


Fig. 2. Main circuit topology of the power converter.

Where Z_{m_jc} [℃/W] is the mth device thermal impedance form the junction to the case, namely the self-heating thermal impedance, which can be easily derived from the device datasheet, and p_{m_j} [W] is the heat flux on the chip area, i.e., the mth device power dissipation.

Finally, by substituting (7) and (10) into (9), the mth device transient junction temperature can be expressed as:

$$T_{m\_j} = Z_{m\_jc} p_{m\_j} + Z_{m\_cs} p_{m\_c} + \sum_{i=1}^{n} Z_{mi} p_i + T_a \tag{11}$$

Where p_{m_c} [W] is the heat flux on the mth device case, which is approximately the mth device power dissipation, and Z_{m_cs} [℃/W] is the thermal impedance form the case to the heat sink.

IV. THERMAL MODEL FOR THE POWER CONVERTER IN SRM DRIVES

A. System Introduction

In this paper, to verify the above theory, a main circuit topology of the power converter, which is called a three-phase asymmetric half-bridge, is selected as shown in Fig.2. This main circuit is widely used in SRM drives. The corresponding model structure is illustrated in Fig.3. The numbers are to identify the devices. For example, device 1 and device 2 are in parallel to constitute the VT_1.

Each power transistor is a power MOSFET (FAIRCHILD FQA160N08), and each freewheeling diode is a fast recovery diode (IXYS DSEI 2x121). Taking phase A for example, the drive signals of the upper and lower transistors, VT_1 and VT_2, are the position control signal and pulse width modulation (PWM) chopping signal during phase A, respectively. In terms of reducing the torque ripple and switching losses, as well as the iron losses, the single switch chopping strategy is always adopted. This strategy turns on the upper transistor VT_1 and keeps the lower transistor VT_2 chopping. Then both transistors are turned off in the freewheeling region.

The upper transistors are placed in the upper row of the heat sink, and the lower transistors are placed in the middle of the heat sink. The heat sink is made of aluminum alloy (AL 6063/T5), and it is assumed that the fan is stopped so that the heat sink is under the natural air-cooling condition.

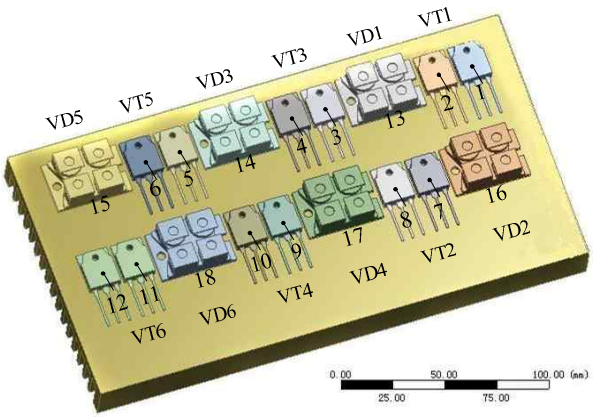


Fig. 3. Structure model of the power converter.

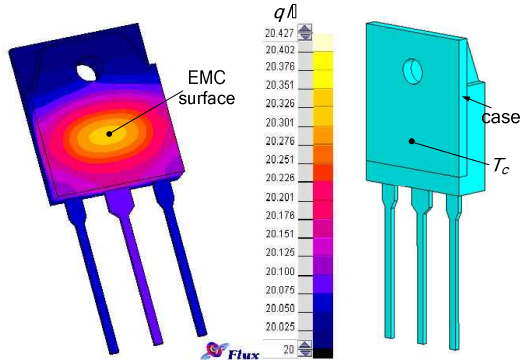


Fig. 4. FEM thermal model of the single power MOSFET.

B. EMC Surface Temperature Rise Simulation

The device case temperature T_c is always measured to predict the junction temperature according to $Z_{\theta jc}$ given by the transient thermal response curve (TTRC) in the datasheet, because the junction temperature is difficult to measure directly especially for a packaged device. T_c is the temperature on the case as shown in Fig.4. However, the device case is generally fixed on a heat sink, so to measure it the heat sink should be punched, and this penetrates the base and often penetrates the fins which destroys the cooling performance. There are a number of power MOSFETs in this system, and the traditional method [9] leads to expensive test costs as well as a large amount of destruction to the heat sink. Therefore, measuring T_c in this paper is not suitable. It is easy to measure the EMC surface temperature of the power MOSFETs in Fig.4 and Fig.8, but the thermal impedance curves from the EMC to the junction and from the EMC to the case are not given in the datasheet. Thus, a transient thermal FEM model for a single power MOSFET is built under the TTRC test condition in Fig.4. The obtained transient temperature curves for the junction, the case, and the EMC surface are shown in Fig.5, and the EMC surface temperature test point is located where the chip center faces. It is the hottest temperature on the surface.

By comparing the three curves in Fig.5, it can be seen that

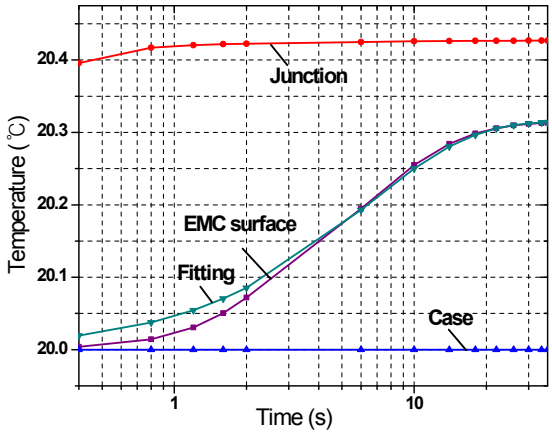


Fig. 5. Transient temperature curves for the junction, case, and EMC surface of the power MOSFET.

the temperature rise from the EMC to the junction is complex, while the temperature rise from the EMC to the case is simple. Assuming that in the latter condition the heat flux from the EMC to the case is a constant, the value is the device power dissipation. Thus, the temperature rise can be simulated by the thermal impedance model. In this paper, a third-order Cauer network is used to fit the EMC surface temperature by the least square method, and the result is shown in Fig.5.

The above method uses the easily measured EMC surface temperature instead of the junction temperature or the case temperature which are hard test. Then the case temperature can be predicted from the EMC temperature. The precondition of this simulation is that the heat transfer ability of the case is stronger than that of the EMC surface, and the convective heat transfer condition of the EMC surface is close to natural air-cooling, which is suitable for most conditions.

C. Extraction of the Heat Sink Thermal Impedance Matrix

According to (7), when the *i*th device works alone, the thermal impedance Z_{mi} is:

$$Z_{mi} = \frac{\theta_{m\_sa}}{p_i} \tag{12}$$

This means that the heat sink distributed coupling thermal impedance matrix can be extracted from (12). These thermal impedances are independent of the device power dissipation. Therefore, if the heat flux is 1W, then the transient temperature rise is the thermal impedance according to (12).

The heat sink transient 3-D thermal model in Fig.6 is established by FEM software FLUX, which also shows 18 areas and points. Firstly, the heat flux 1W is loaded upon heating area 1 contracted with device 1. The transient thermal impedance curves of 18 test points are derived, and third-order Foster networks are used to fit these curves by the least squares function in MATLAB. Then the thermal resistances *R*th and thermal capacitances *C*th are obtained, which belong to the impedances Z_{ln} (n=1,2,3…18). Secondly, the other devices are loaded separately and the other thermal impedances are

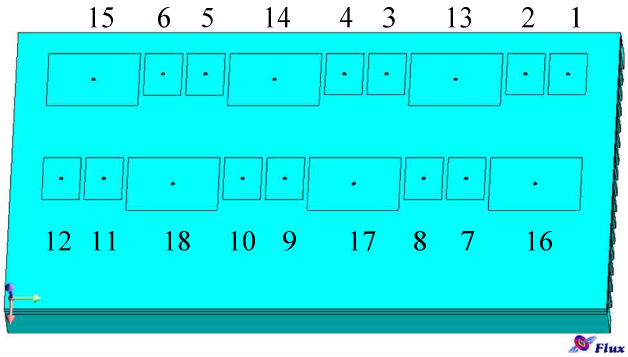


Fig. 6. Extraction model for the heat sink thermal impedance matrix.

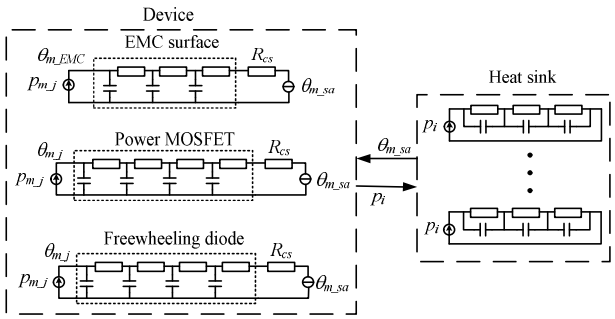


Fig. 7. Schematics of thermal impedance model for the power converter.

extracted. Finally, the heat sink distributed coupling thermal impedance matrix is derived. This extraction process is carried out automatically by M files and calling the FLUX program.

D. Temperature Rise Model of the Power Converter

Based on the above theory, the transient thermal impedance models of the EMC temperature rise, the power MOSFET junction temperature rise, and the freewheeling diode junction temperature rise are built by MATLAB/Simulink. The schematic of the model structure is illustrated in Fig.7. The device junction temperature rise models use the fourth-order Cauer network, and the EMC surface temperature rise model uses the third-order Cauer network. The contract thermal resistances between the devices and the heat sink use the lumped thermal resistances, and assuming that they are equal to simplify the problem, and naming them R_{cs}; every distributed coupling impedance, for example Z_{12}, uses a third-order Foster network; the heat flux p_i that flows through R_{cs}, and the Γ_m temperature rise θ_{m_sa} are used to connect the devices and the heat sink to satisfies (3) and (4), and to connect the Cauer network and the Foster network.

V. EXPERIMENTAL VALIDATION

In order to validate the proposed thermal model of the power converter, experiments are carried out to test the device transient temperature rises from the time of the motor startup to the time that the temperature rises become stable. During the experiments, a power converter is used to control a 500W SRM working at a stable speed of 416.7r/min without any loads. The transient EMC surface temperature rise curves of the power MOSFETs are measured by a JK-16. 12 thermocouples are placed on the surface in Fig.8. The sampling time of the JK-16 is 1 s. This temperature detection method is convenient and suitable for the power converter, as can be seen from Fig.8.

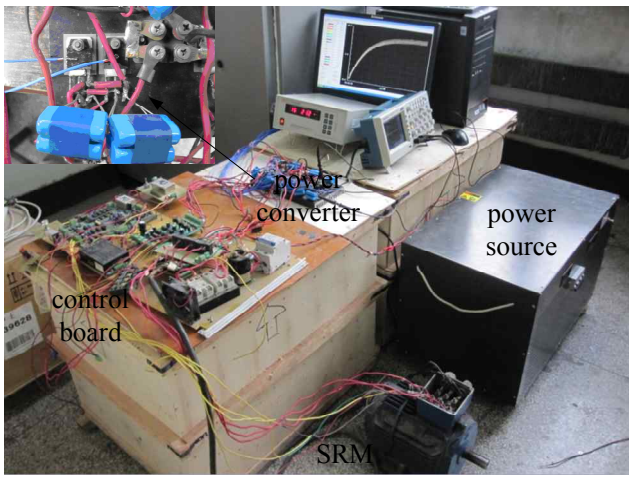


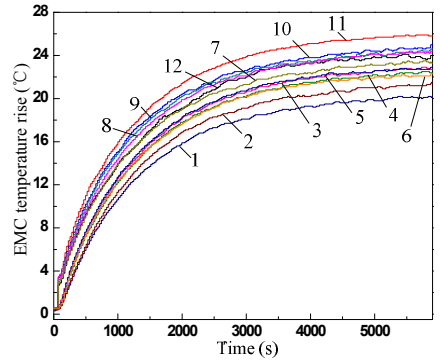
Fig. 8. Experiment photograph.

TABLE I
DISSIPATED POWER OF THE DEVICES

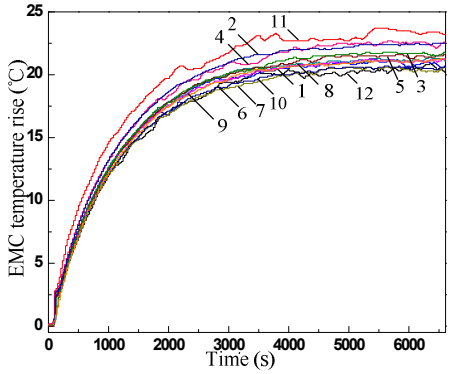
Control strategy	Dissipated power of the devices /W						
No.	1	2	3	4	5	6	7
Fixed	0.336	0.462	0.462	0.336	0.462	0.336	2.763
Alternate	1.571	1.919	1.919	1.571	1.919	1.571	1.571
No.	8	9	10	11	12	13	16
Fixed	3.377	2.763	3.377	3.684	2.456	0.200	0.010
Alternate	1.919	1.571	1.919	2.094	1.396	0.105	0.105

To determine the effect of the control strategy on the temperature distribution of the power converter, an alternate single switch chopping control strategy is designed based on the traditional fixed single switch chopping control strategy. This is done for the purpose of comparison. The alternate single switch chopping control strategy is chopping the upper transistors during one cycle of the transistor working region, then chopping the lower transistors of the same phase during the next cycle of the transistor working region, and then repeating the above process.

The experimental temperature rise curves of the test points under the two control strategies are recorded, as shown in Fig.9, to validate the simulated results. The ambient temperature is 14.6 ℃, and the estimated power dissipation of the devices is given in Table I.

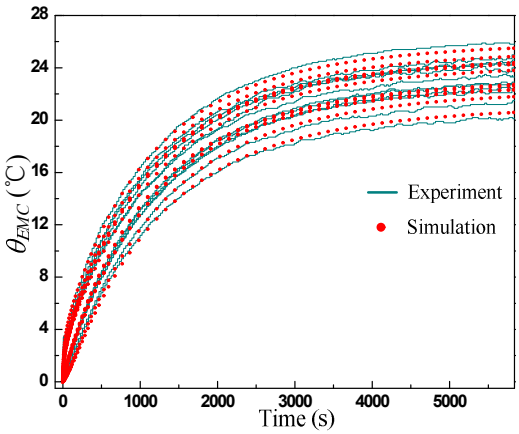


(a) Fixed single switch chopping control strategy.

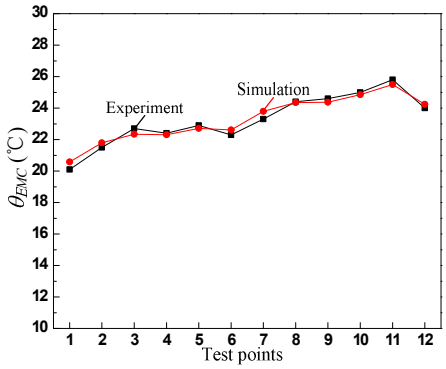


(b) Alternate single switch chopping control strategy.

Fig. 9. Experimental temperature rise curves of 12 test points under two control strategies.



(a) Transient temperature rise.

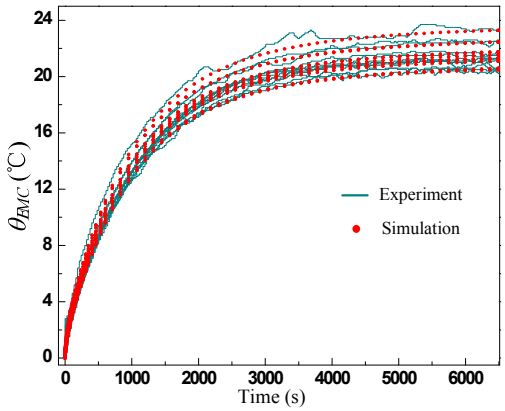


(b) Steady-state temperature rise.

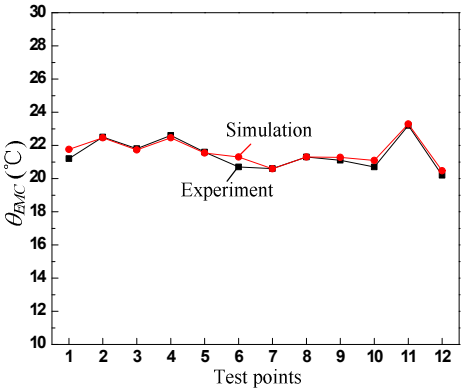
Fig. 10. Comparison of experimental results and simulated results under the fixed single switch chopping control strategy.

TABLE II
STEADY-STATE SIMULATION ACCURACY

Control strategy	Fixed	Alternate
Maximum absolute error(℃)	0.50	0.60



(a) Transient temperature rise.



(b) Steady-state temperature rise.

Fig. 11. Comparison of experimental results and simulated results under the alternate single switch chopping control strategy.

The experimental results in Fig. 9 show that all of the temperature rise curves become stable from 5000 s. This is because the device location, the control strategy, and the power losses have little effect on the time constant of the system. The curves of 7-12 in Fig. 9(a) and all of the curves in Fig. 9(b) display nearly linear rises in the beginning. This is due to the fact that the startup winding current is so large that the chopping transistors produce a large number of power dissipations in a short time such as the turn-off losses and the conduction losses.

Fig. 10 and Fig. 11 show comparisons of the simulated results and the experimental results of the 12 test points in the transient and stationary behaviors under the two control strategies.

The simulated results match well with the experimental results in both Fig. 10 and Fig. 11 with acceptable accuracy, as shown in Table II. The simulation curves in Fig. 10(a) bifurcate into two groups owing to the temperature rises of the lower transistors which are much higher than those of the upper

TABLE III

AVERAGE DISSIPATED POWER OF THE DEVICES

Control strategy	Average dissipated power /W			
	device1	device7	device13	device16
Fixed	0.420	3.070	0.200	0.010
Alternate	1.745	1.745	0.105	0.105

transistors, as can be clearly seen from Fig. 10(b). The two parallel transistors have different temperature rises, as can be seen in in Fig. 10(b) and Fig. 11(b), because the differences in the electrical behaviors between the two parallel transistors result in an uneven current distribution. This makes one transistor's temperature increase while the other's temperature decreases, as in device 11 and device 12.

The differences between the experiment and simulation are mainly due to four reasons. First, the measurement accuracy is ±(0.5%+0.5)℃ when the temperature is between 0~300℃. Second, the dissipated power varies with time in the experiment, while in the simulation it is a constant. Third, the contract resistances between the devices and the heat sink are the same constants in the simulation, but actually they are affected by many factors such as the pressure upon the device, the smooth of the interface between the device and the heat sink, the thickness of the thermal gasket between the device and the heat sink, and so on. Fourth, the convective capacity of the system fluctuates slightly all the time. Overall, absolute errors within 1℃ is very high accuracy.

In summary, the simulation results match well with the experimental results, which verifies the correctness of the proposed thermal model.

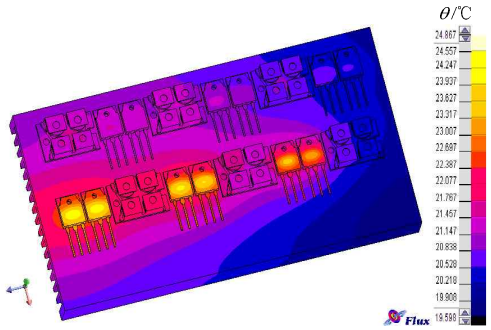
VI. RESULTS AND DISCUSSION

A. Comparisons with other thermal models

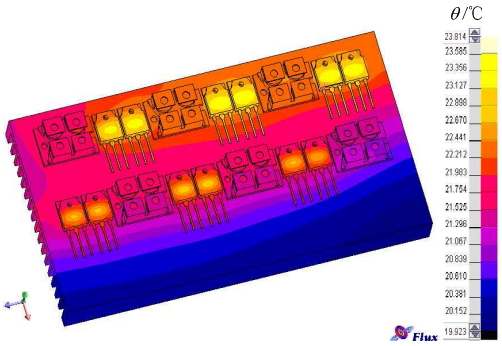
The proposed thermal model is compared with the FEM 3-D thermal model given in Fig. 12 and the traditional thermal impedance model in [13]. The power losses in Table III ignore the uneven current, which is more valuable.

Fig. 13 shows a comparison of the three steady-state junction temperature rises under the two control strategies. The simulation results from the proposed model closely match those from the FEM model. The results form the traditional thermal impedance model are much higher than the results from the other two models, so that the obtained heat sink thermal resistance is smaller than the actual value, which validates the feasibility of the traditional thermal impedance model for engineering thermal design. However, the devices at different locations have the same junction temperature rise in the traditional model, which deviates from practice.

Table IV shows a comparison between the three models in terms of solution time and calculation accuracy. It shows that the proposed model, which has the accuracy of the FEM model and the fast solution time of the traditional thermal impedance model, achieves a good compromise between speed and accuracy.



(a) Fixed single switch chopping control strategy.



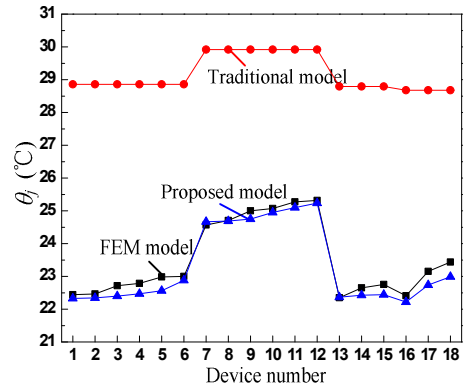
(b) Alternate single switch chopping control strategy.

Fig. 12. Stationary temperature rise distributions of the power converter under two control strategies.

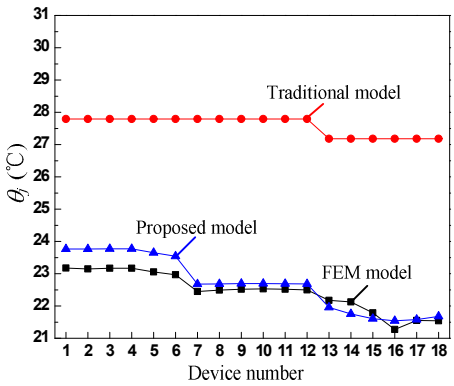
B. Stationary Temperature Rise Distributions

Fig. 12(a) shows that the temperature rises of the lower transistors are higher than those of the upper transistors in the fixed single switch chopping control strategy, because the power dissipation of the chopping transistors is much lager than that of the conducting ones. Therefore, the chopping transistors have to endure a lot of thermal stress, and are easy to overload and destroy when the load increases. Device 12 has the highest junction temperature rise, 24.867 ℃, among the power converters, owing to it is location at the edge of the heat sink resulting in its poor cooling condition.

Fig. 12(b) demonstrates that the temperature rise distribution of the power converter becomes remarkably uniform with the alternate single switch chopping control strategy. The temperature rises of the upper transistors are higher than those of the lower transistors, because the thermal resistance of the central part of the heat sink is the lowest. Device 1 has a maximum junction temperature rise of 23.814 ℃, which declines about 1 ℃ from the former maximum junction



(a) Fixed single switch chopping control strategy.



(b) Alternate single switch chopping control strategy.

Fig. 13. Comparison of the three models results under two control strategies.

TABLE IV

CONTRAST BETWEEN THE THREE MODELS IN SIMULATION

Model	Stationary time	Transient time	Accuracy
Traditional	< 1 minute	< 1 minute	low
FEM	> 2 hours	>> 2 hours	higher
Proposed	< 1 minute	< 10 minute	high

temperature rise. Therefore, the highest temperature rise of the power converter descends and the temperature distribution becomes uniform. The reduced temperature rise differences among the devices make the device electrical characteristics become consistent. In addition, each device endures similar thermal stress, and the thermal reliability of the power converter is significantly enhanced when compared to the former control strategy.

C. Transient Temperature Rise Curve

The temperature rise curves of the transistors have the same stabilization time, about 1 hour 23 minutes. The rise time is determined by the product of the thermal resistance and the thermal capacity in the system, and it is independent of the power dissipation.

The curves present a rapid rise in the beginning, and this

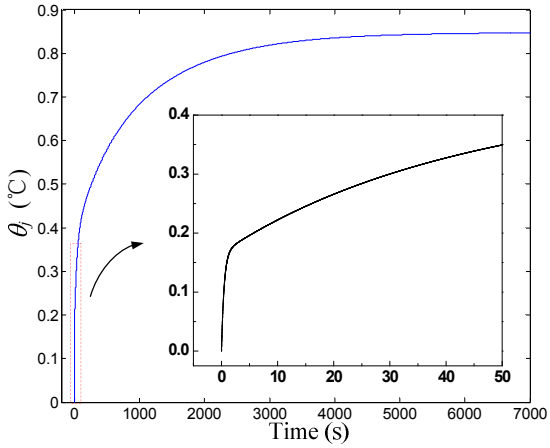


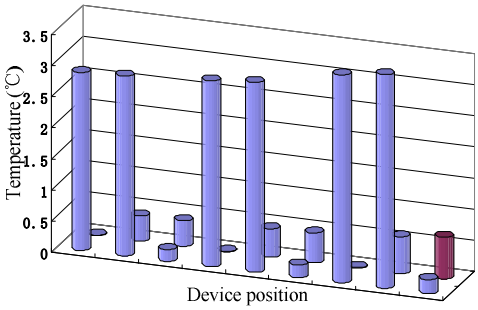
Fig. 14. Temperature rise curve with device 1 working alone.

phenomenon remains when the power dissipation is constant. For example, Fig.14 shows the junction temperature rise curve of device 13 when it is heated separately and constantly. The devices have a short thermal time constant in comparison with the heat sink. When the devices is heated, the temperature increases rapidly. However, due to the material heat capacity, the heat sink is not heated and the characteristics of the heat sink do not affect the device temperature rise. Therefore, the current temperature rise is determined by the thermal time constant of the device. With the further development of the heat conduction, the curve is mainly determined by the thermal time constant of the heat sink.

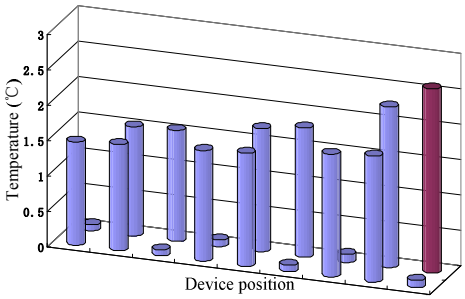
D. Thermal Coupling Effect

The influence of the thermal coupling upon the steady-state junction temperature rises of device 1 under the two control strategies is shown in Fig.15. The bottom surface (xy plane) represents the heat-sink surface where the devices are mounted. There are 18 cylinders in the figure representing the 18 devices in the power converter as in Fig.3. The cylinder's height stands for the device 1 (red cylinder) temperature rise caused by the heating of the device in this cylinder. For example, the height of the second cylinder of the lower row from the right means that the temperature rise of device 1 is caused by the heading of device 7. The temperature rise of device 1 can be derived by adding all heights of all the cylinders.

The figures illustrate that the influence of the self-heating upon the device steady-state junction temperature rise is not the largest. However, the effect of the mutual-heating is so large that it cannot be ignored. A large heating power like a power MOSFET has a tremendous impact on the device temperature rises while a small heating power such as a freewheeling diode has little effect, therefore it can be ignored. When the heating power is equal, the thermal coupling effect is increased when the distance is decreased.



(a) Fixed single switch chopping control strategy.



(b) Alternate single switch chopping control strategy.

Fig. 15. Thermal coupling effect on the stationary junction temperature rises of device 1 under two control strategies.

VII. CONCLUSIONS

Considering the temperature rise of a heat sink with multiple heat sources meets the superposition principle under the air-cooling condition. A new thermal model for power converters is proposed based on the heat sink distributed coupling thermal impedance matrix and the device thermal impedance. Take SRM drives for example, the transient temperature rise model of the power converter in a SRM drive is implemented in MATLAB/Simulink, which can calculate the device junction temperature rises, the EMC surface temperature rises, and the heat sink temperature rises of the heating area.

Then, the proposed model is validated by experiments, and the method of measuring the EMC surface temperature rise of the power MOSFET is adopted instead of the junction temperature and case temperature. The thermal model provides high accuracy with a fast calculation speed by comparing the FEM thermal model and the traditional thermal impedance model. This can be easily implemented in a circuit simulator to compute the device instantaneous temperature under different load conditions of the SRM.

Finally, according to simulation and experimental results, device 11 and device 12 are likely to have the highest temperature rise in the fixed single switch chopping control strategy. Device 1 and device 2 are also the most likely to have the maximum temperature rise in the alternate single switch chopping control strategy. The alternate single switch chopping control strategy is better than the fixed single switch chopping control strategy in terms of system thermal reliability. There is a rapid increase in the temperature rise curve during motor startup, and then the curve becomes stable from 5000 s. The rise time is determined by the product of the thermal resistance and heat capacitance of the system, and it is independent of the control strategy, the device location and the device power dissipation.

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