# An Enhanced Harmonic Voltage Compensator for General Loads in Stand-alone Distributed Generation Systems

Quoc-Nam Trinh[*], Hong-Hee Lee[†], and Tae-Won Chun[*]

[*†]School of Electrical Engineering, University of Ulsan, Ulsan, Korea

## Abstract

This paper develops an enhanced harmonic voltage compensator which is implemented with the aid of two repetitive controllers (RCs) in order to improve the output voltage performance of stand-alone distributed generation (DG) systems. The proposed harmonic voltage compensator is able to maintain the DG output voltage sinusoidal regardless of the use of nonlinear and/or unbalanced loads in the load side. In addition, it can offer good steady-state performance under various types of loads and a very fast dynamic response under load variations to overcome the slow dynamic response issue of the traditional RC. The feasibility of the proposed control strategy is verified through simulations and experiments.

**Key words:** Distributed generation, nonlinear load, unbalanced load, repetitive controller, harmonic compensation

## I. INTRODUCTION

In recent decades, concerns about global warming, gas emissions and the depletion of fossil fuels have resulted in increasing utilization of renewable energy sources (such as wind turbines, photovoltaic, fuel cells, etc.) to produce electricity. Nowadays, a large number of renewable energy sources have been integrated into power distribution systems through power electronic converters in the form of distributed generation (DG) [1]. The DG systems are mainly developed for grid-connected operation with various operational functions such as power control, harmonic current mitigation, and reactive power compensation [2]-[4]. However, due to the demand for supplying electricity to rural villages and remote islands, the use of DG in stand-alone operation is also important. In stand-alone mode, DGs must deliver a sinusoidal voltage to loads at the point of common coupling (PCC) with a constant magnitude and frequency. Due to the absence of a stiff grid in the stand-alone operation of a DG system, the quality of the DG output voltage strongly depends on the performance of the voltage control strategy. The quality of the DG output voltage is mainly evaluated by the
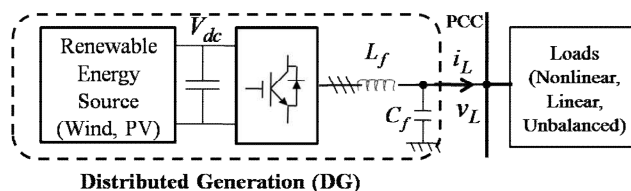
Fig. 1. Configuration of a stand-alone DG system connected with loads at the PCC.

steady-state error and dynamic performance under load changes. In addition, with the wide use of nonlinear and unbalanced loads, the total harmonic distortion (THD) should also be considered to evaluate the DG output voltage performance.

The configuration of a stand-alone DG system connected with loads at the PCC is shown in Fig. 1. In order to supply a high quality output voltage ($v_L$) at the PCC, many control efforts have been developed [5]-[15]. For the case of balanced linear loads, a proportional-integral (PI) controller in the synchronous reference frame is sufficient to produce a sinusoidal output voltage at the PCC [5]-[7]. However, the PI controller is unable to maintain a sinusoidal DG output voltage when unbalanced and/or nonlinear loads are connected to the PCC due to its limitation of the control bandwidth. In order to overcome this issue, several advanced control methods have been proposed such as PI controllers in

multiple reference frames [8], [9], predictive control [10], [11], adaptive control [12], multiple resonant controllers [13], [14], and repetitive control [15].

In [8], [9], to supply a pure sinusoidal output voltage at the PCC under a nonlinear load, a bank of PI controllers was used where each PI controller regulated the magnitude of a single harmonic voltage. In these control methods, many PI controllers and coordinate transformations are required to compensate all of the voltage harmonics, which makes this type of control strategy too complex. Meanwhile, a predictive control strategy was proposed in [10] which can provide a good control performance and a fast dynamic response. However, it is well-known that the performance of a predictive controller depends heavily on knowledge of the system parameters. Hence, system uncertainties would be a vital issue affecting the control accuracy. An adaptive control strategy is introduced in [12] where a load current observer is developed to estimate the load current variations, which helps improving the dynamic performance of the voltage controller. However, even though the load current measurement is omitted, the inverter current measurement is required. Moreover, regardless of the control effort, the output voltage is disturbed under load step changes. A control method which uses multiple resonant controllers for handling unbalanced and non-linear loads has been developed for DG systems [13], [14]. By implementing the control scheme in the stationary reference frame, coordinate transformations are eliminated. However, since each resonant controller is capable of compensating only one specific harmonic voltage, a large number of resonant controllers must be used if all of the harmonic voltages need to be compensated. In addition, these control strategies have a current control loop and require load current measurements, resulting in a complex control scheme.

To overcome the complexity of multiple resonant controllers, an advanced control strategy with a repetitive controller (RC) was introduced in [15]. In [15], one RC is able to replace a bank of resonant controllers. As a result, the control strategy is simplified. The RC in [15] can offer good steady-state performance as well as a very fast dynamic response to overcome the slow dynamic response issue of traditional RCs [16], [17]. However, the RC in [15] is only suitable for application to three-phase nonlinear loads because it takes into account only the dominant harmonic components in three-phase systems, i.e., $(6n\pm1)$th ($n$=1, 2, 3…). Hence, if single-phase nonlinear loads or unbalanced loads are used in the system, the performance of the control strategy is deteriorated due to the presence of other harmonic components such as third, ninth, fifteenth, etc.

In this paper, in order to overcome the drawback of previous RCs, an enhanced voltage control strategy is proposed which is composed of two repetitive controllers. In the proposed harmonic voltage compensator, one RC is designed in the rotating reference ($d$-$q$) frame to compensate
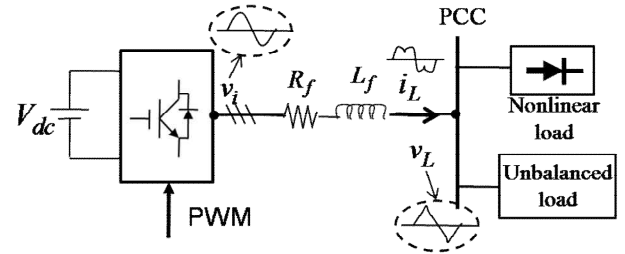


Fig. 2. Connection interface of a DG with various loads.

the $(6n\pm1)$th ($n$=1, 2, 3…) harmonics and the other RC is designed in the stationary reference ($\alpha$-$\beta$) frame to compensate triplen harmonics such as the third, ninth, fifteenth, etc. As a result, the DG output voltage is regulated to be a sinusoidal waveform irrespective of the presence of single-phase and three-phase nonlinear and/or unbalanced loads. The proposed control strategy can offer excellent steady-state performance of the DG output voltage under various load conditions as well as a fast dynamic response under load variations thanks to the short delay time of both RCs, which is only one-sixth of fundamental period. The feasibility of the proposed control strategy is verified through simulations and experiments.

## II. HARMONIC VOLTAGE COMPENSATION SCHEME

### A. Effects of nonlinear and unbalanced loads on the DG output voltage

The connection interface of a DG with various types of loads, including single-phase and three-phase nonlinear loads and/or unbalanced loads, is shown in Fig. 2. In Fig. 2, $R_f$ and $L_f$ are the resistance and inductance of the line impedance, respectively. Based on Fig. 2, the DG output voltage ($v_L$) can be calculated as:

$$v_L = v_i - R_f i_L - L_f \frac{di_L}{dt}, \qquad (1)$$

where $v_i = v_{i1}$ is the output voltage of the inverter, which is assumed to have only the fundamental component ($v_{i1}$), and $i_L$ is the load current.

If nonlinear and unbalanced loads are connected in the load side, the load current draws harmonic currents into the system. Thus, the DG output voltage is determined by:

$$v_L = \left( v_{i1} - R_f i_{L1} - L_f \frac{di_{L1}}{dt} \right) - \left( R_f \sum_{h\neq1} i_{Lh} + L_f \sum_{h\neq1} \frac{di_{Lh}}{dt} \right), \qquad (2)$$

where $i_{L1}$ and $i_{Lh}$ are the fundamental and harmonic components of the load current, respectively.

As can be seen in (2), even though the inverter can generate a pure sinusoidal output voltage, the DG output voltage becomes distorted due to a harmonic voltage drop on
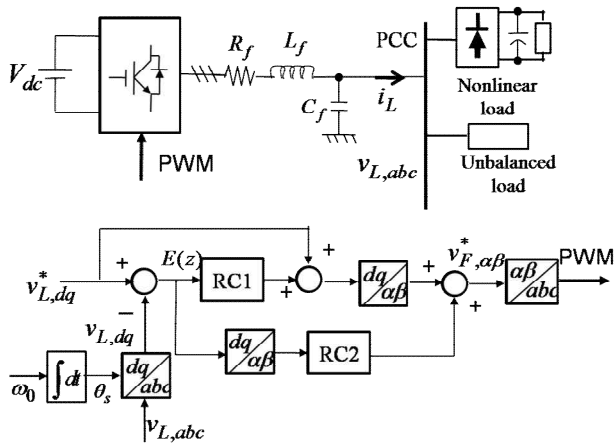
Fig. 3. Block diagram of the proposed harmonic voltage compensator.



Fig. 4. General structure of a repetitive controller.

## III. PROPOSED REPETITIVE CONTROLLER

### A. Structure of the Repetitive Controller

Fig. 4 shows the general structure of a RC in the discrete-time domain. Based on Fig. 4, the transfer function of the RC can be described as:

$$C(z) = \frac{U(z)}{E(z)} = \frac{K_r z^{-N+k}}{1 - Q(z) z^{-N}}, \qquad (4)$$

where $z^{-N}$ is the time delay unit, $z^k$ is the phase lead term, $Q(z)$ is a filter transfer function, $K_r$ is the RC gain, $R(z)$ is the reference value, $E(z)$ is the tracking error, and $U(z)$ is the output of the RC.

In (4), $N$ is the number of samples in one fundamental period which is defined as the ratio of the sampling frequency and the fundamental output frequency. As a result, the RC has three main components that need to be determined, i.e., the filter $Q(z)$, the phase lead term $z^k$, and the RC controller gain $K_r$.

In [15], the RC considers only the $(6n \pm 1)$th ($n$=1, 2, 3…) harmonic components, which are the dominant components in three-phase systems. To compensate the $(6n \pm 1)$th harmonics, the RC in [15] is designed in the $d$-$q$ frame because in this frame the $(6n \pm 1)$th harmonics behave as $6n$th ($n$=1, 2, 3…) harmonics. The transfer function of the RC in [15] is shown as:

$$C_1(z) = \frac{U(z)}{E(z)} = \frac{K_{r1} z^{-N/6+k}}{1 - Q(z) z^{-N/6}}. \qquad (5)$$

As presented in [15], the RC offers good steady-state performance and a fast dynamic response under three-phase nonlinear load conditions. However, if single-phase nonlinear loads or unbalanced loads are used in the system, the control performance will be deteriorated due to the presence of triplen harmonic components such as the third, ninth, fifteenth, etc. In order to compensate the odd harmonic components, the traditional RC or the odd-harmonic RC is an effective solution [16], [17]. Unfortunately, these RCs have a long delay time, which normally results in a poor dynamic response under load variations.

### B. Proposed Repetitive Controller

In order to compensate the odd harmonic components with a fast dynamic response, this paper introduces an enhanced harmonic voltage compensator composed of two different

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the line impedance. Hence, in order to achieve a sinusoidal output voltage at the PCC, the inverter must generate a distorted voltage to compensate for the harmonic voltage drop on the line impedance as follows:

$$v_i = v_{i1} + \sum_{h \neq 1} v_{ih}, \qquad (3)$$

where $v_{ih}$ is the harmonic component of the inverter output voltage.

Theoretically, the inverter voltage $v_i$ in (3) produces all of the harmonic components (odds and evens). However, in a practical system, the harmonic components are mainly composed of odd orders such as the third, fifth, seventh, ninth, etc. Hence, to produce a sinusoidal voltage at the PCC, the voltage compensator only needs to regulate these odd harmonics. The proposed harmonic voltage compensator composed of two repetitive controllers can fulfill the demand to supply a sinusoidal DG output voltage regardless of the use of single-phase nonlinear, three-phase nonlinear and unbalanced loads.

### B. Harmonic Voltage Compensation Scheme

A block diagram of the proposed harmonic voltage compensator is shown in Fig. 3. This compensator consists of two repetitive controllers: RC1 and RC2. In Fig. 3, RC1 is implemented in the synchronous reference ($d$-$q$) frame rotating at the fundamental frequency $\omega_0$ to compensate the $(6n \pm 1)$th ($n$=1, 2, 3…) harmonics whereas RC2 is designed in the stationary reference ($\alpha$-$\beta$) frame to mitigate triplen (such as the third, ninth, fifteenth, etc.) harmonics. Thereby, the use of two repetitive controllers, RC1 and RC2, is sufficient to compensate all of the odd harmonic voltage drops caused by many kinds of loads to ensure that the DG output voltage is maintained sinusoidal.
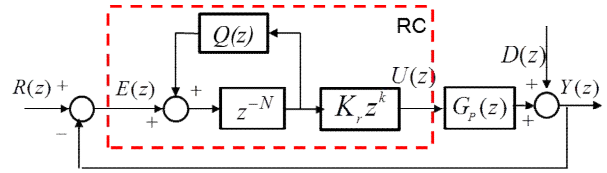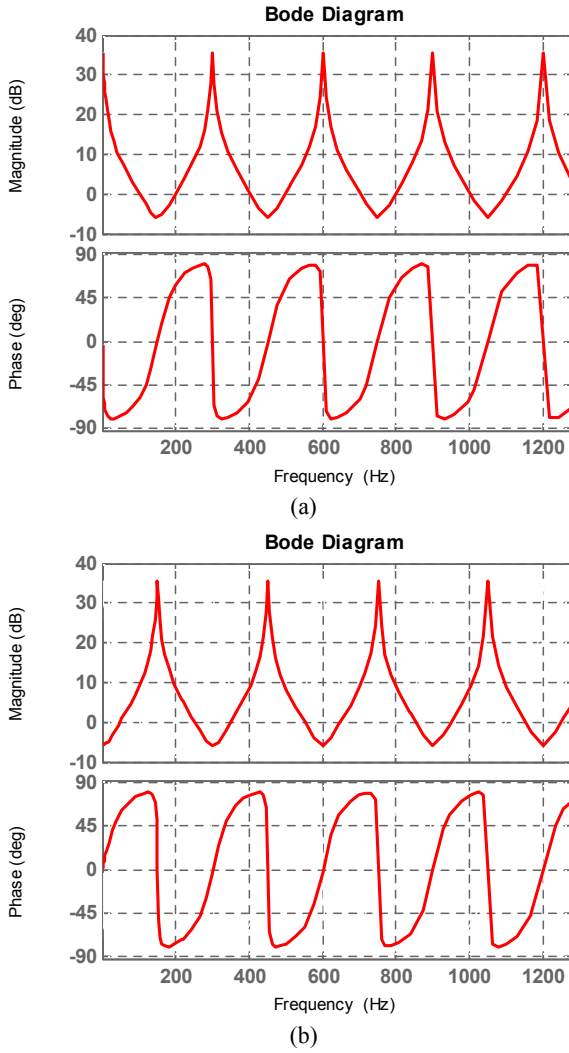
Fig. 5. Bode diagram of the RC1 and RC2.

RCs where one RC is designed to compensate the (6n±1)th (n=1, 2, 3…) harmonic components and the other RC is used to compensate triplen harmonics such as the third, ninth, fifteenth, etc.

To compensate the (6n±1)th (n=1, 2, 3…) harmonics, RC1 is designed in the *d-q* frame and has the same transfer function as given in (5). On the other hand, the ohter repetitive controller, i.e., RC2, is designed in the *α-β* frame to mitigate triplen harmonics. The transfer function of RC2 is given as:

$$C_2(z) = \frac{U(z)}{E(z)} = \frac{-K_{r2}z^{-N/6+k}}{1+Q(z)z^{-N/6}} . \qquad (6)$$

As a result, with the combination of two repetitive controllers, RC1 and RC2, designed in different reference frames, all of the odd harmonics can be compensated to supply a sinusoidal DG output voltage. As given in (5) and (6), the number of the sampling delay of the two RCs is

limited at one-sixth when compared to that of the traditional RC given in (4). Therefore, with the proposed controller, a fast dynamic response of can be achieved, which is similar to the RC in [15], without degrading the control performance under single-phase nonlinear load or unbalanced load conditions.

Bode diagrams of RC1 and RC2 are shown in Fig. 5(a) and Fig. 5(b), respectively. In Fig. 5, the fundamental frequency is selected at 50 Hz. As shown in Fig. 5, RC1 in the *d-q* frame provides a high controller gain at the 6*n*th (n=1, 2, 3…) harmonics, meanwhile RC2 in the *α-β* frame has a high gain at triplen harmonics. Therefore, a combination of these two repetitive controllers ensures that the odd harmonics can be effectively compensated.

In (5) and (6), *Q(z)* is used to improve the system stability margin by reducing the peak gains of the RC at the high-frequency range. *Q(z)* is regularly employed with a zero phase-shift low-pass filter (LPF) as given in (7) because this can improve the stability margin without degrading the steady-state performance of the RC.

$$Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1}, \qquad (7)$$

where $\alpha_0 + 2\alpha_1 = 1$ and $\alpha_0, \alpha_1 > 0$.

In order to investigate the stability condition of the proposed RC, the relationship between the tracking error *E(z)*, the reference *R(z)*, and the disturbance *D(z)* is derived as (8) according to Fig. 4.

$$E(z) = \frac{[1-Q(z)z^{-N/6}][1-G_P(z)]}{1-z^{-N/6}[Q(z)-K_r z^k G_P(z)]} R(z)$$
$$- \frac{1-Q(z)z^{-N/6}}{1-z^{-N/6}[Q(z)-K_r z^k G_P(z)]} D(z) \qquad (8)$$

Let $H(z) = Q(z) - K_r z^k G_P(z)$. Then, the repetitive control system becomes stable if the condition given in (9) is satisfied [16].

$$\left| H(e^{j\omega T}) \right| < 1, \qquad (9)$$

where $\omega \in [0, \pi/T]$; *T* denotes the sampling period and $\pi/T$ is the Nyquist frequency.

According to (9), the stability condition of the RC does not depend on the number of the delay sample *N*, but relies on *Q(z)*, $z^k$, and $K_r$. In order to guarantee the stability of the repetitive control system, the parameters *Q(z)*, $z^k$, and $K_r$ should be determined so that the vector $H(e^{j\omega T})$ does not exceed the unity circle. This condition should be taken into account when designing the RC.

## IV. DESIGN OF THE REPETITIVE CONTROLLER

The basic process to design a RC has been presented in previous studies [15]-[17]. In order to ensure the robust operation of an RC, three components need to be designed:
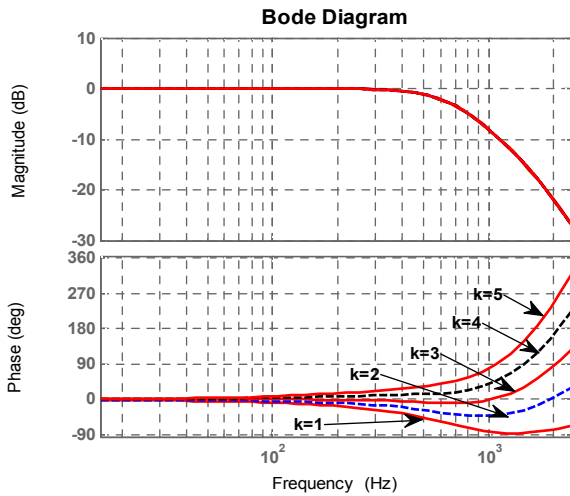
**Bode Diagram**



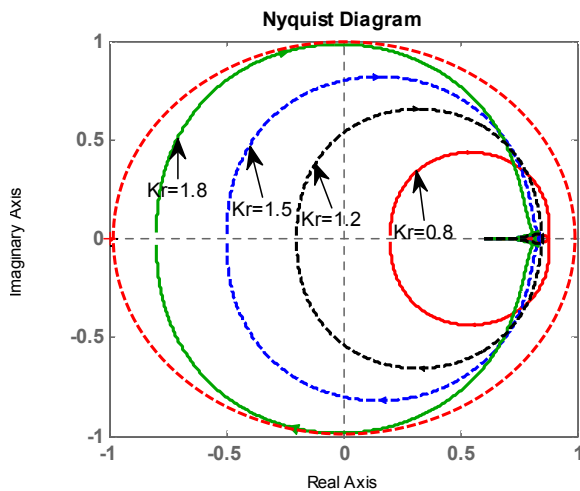Fig. 6. Bode diagram of $G_P(z)z^k$ with different values of $k$.

**Nyquist Diagram**



Fig. 7. Loci of vector $H(e^{j\omega T})$ with different values of $K_r$.

the filter $Q(z)$, the phase lead term $z^k$, and the RC controller gain $K_r$. These components are determined based on the system parameters given in Table I.

In terms of the filter $Q(z)$, a zero phase-shift LPF with the transfer function given in (10) is selected because it provides a cut-off frequency of about 2660 Hz which is sufficient to compensate the harmonic components up to the 51st order.

$$Q(z) = (z + 2 + z^{-1})/4. \tag{10}$$

The phase lead term $z^k$ is used to compensate the phase lag induced by the plant $G_P(z)$; and $k$ is selected to the minimize the phase displacement of $G_P(z)z^k$. If the output of a DG is considered to be an ideal voltage source, the plant can be simplified as a $LC$ filter with the transfer function as:

$$G_P(s) = \frac{1}{L_f C_f s^2 + R_f C_f s + 1}. \tag{11}$$

**TABLE I**
**SYSTEM PARAMETERS**

| Parameters | Values |
|---|---|
| Rated output power | 5 kW |
| DC-link voltage ($V_{dc}$) | 350 V |
| Reference output voltage | 110 V (RMS) |
| Output frequency ($f_o$) | 50 Hz |
| Sampling/Switching frequency | 9 kHz |
| Output filter inductance ($L_f$) | 2 mH |
| Output filter capacitance ($C_f$) | 27 $\mu$F |
| Load of three-phase diode rectifier | R=30 $\Omega$ <br> C=2200 $\mu$F |
| Load of single-phase diode rectifier | R=70 $\Omega$ <br> C=1000 $\mu$F |

Fig. 6 shows a Bode diagram of $G_P(z)z^k$ with different values of $k$. In Fig. 6, $k$=3 is selected because it provides a minimum phase displacement at the dominant harmonic components up to the order 31st. In addition, if one extra delay sample caused by the computation time of the control strategy is considered, $k$=4 is selected.

In the next step, the controller gain $K_r$ is determined to satisfy the stability condition given in (9) and to ensure the robust operation of the RC. To select a proper value for $K_r$, the loci of the vector $H(e^{j\omega T})$ is shown in Fig. 7 with different values of $K_r$. It can be observed that the vector $H(e^{j\omega T})$ is located inside the unity circle, which means that the system is stable if $K_r$ is less than 1.8. In fact, a large $K_r$ offers better steady-state performance as well as a faster response. However, it limits the stability margin of the system at the same time. Therefore, in order to guarantee a sufficient stability margin, $K_r$=1.5 is selected.

## V. SIMULATION RESULTS

A simulation model of a DG was built by PSIM to verify the effectiveness of the proposed compensator. The detailed system parameters are given in Table I. In the simulation, three test cases are considered:

- Case I: a three-phase diode rectifier is used in the load side.
- Case II: a single-phase diode rectifier is connected between phase A and B.
- Case III: both single-phase and three-phase diode rectifiers are used (Case I + Case II).

These three test cases are carried out by using the previous RC introduced in [15] which compensates only the $(6n\pm1)$th harmonic components and the proposed control strategy to compare their control performance.

Fig. 8 shows the steady state performance of the DG output voltage ($v_{L,abc}$) and load current ($i_{L,abc}$) under the three test cases by using the previous RC introduced in [15]. As shown in Fig. 8, the previous RC is only able to offer good
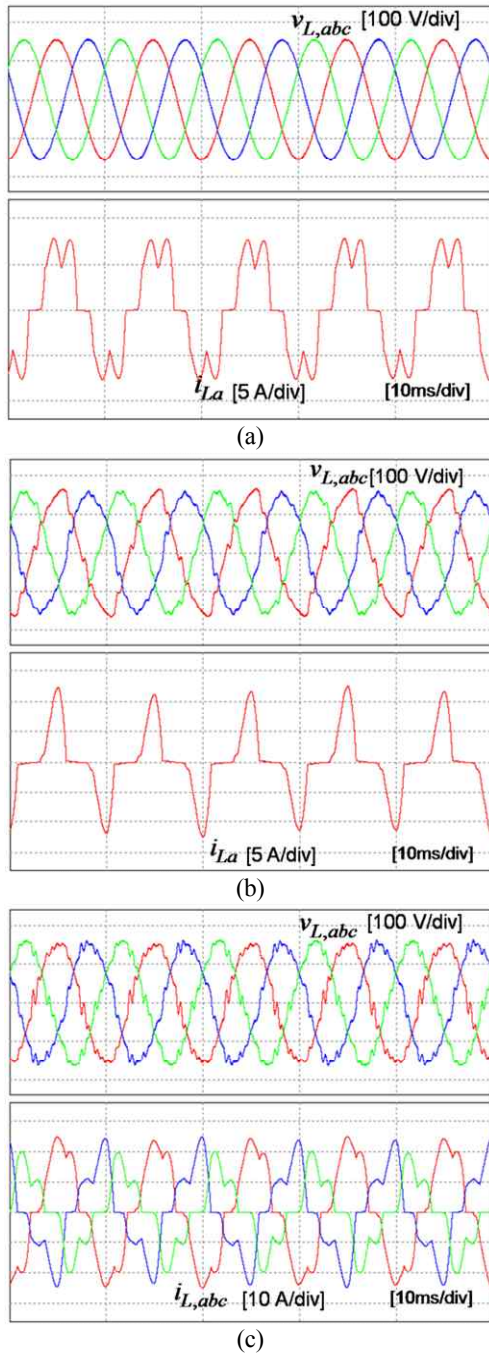
Fig. 8. Steady-state performance of the DG output voltage and load current with the previous RC under (a) case I, (b) case II, (c) case III.
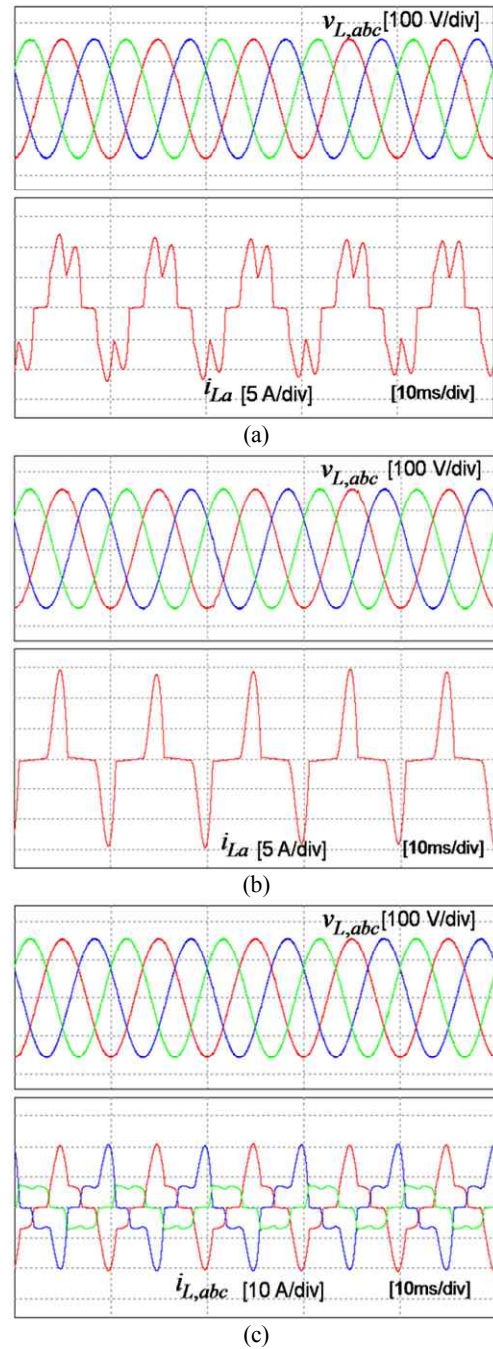


Fig. 9. Steady-state performance of the DG output voltage and load current with the proposed control strategy under (a) case I, (b) case II, (c) case III.

performance of the DG output voltage when a three-phase diode rectifier is used, case I, in Fig. 8(a). In the other test cases, it fails to maintain a sinusoidal output voltage at the PCC. This is because the previous RC takes into account only the $(6n\pm1)$th harmonics, while triplen harmonic components (such are third, ninth, fifteen, etc) caused by a single-phase nonlinear load cannot be compensated properly. As a result, the DG output voltages are distorted as shown in Fig. 8(b) and (c).

A simulation of the DG with the proposed control strategy under the same load condition as Fig. 8 was carried out and the results are shown in Fig. 9. In Fig. 9, it is obvious that the proposed control strategy can provide good performance of the DG output voltage in all three test cases. This is because the proposed controller produces a high controller gain at the $(6n\pm1)$th harmonics as well as triplen. As a result, it is able to effectively compensate all of the odd harmonic voltage drops and regulate the DG output voltage to be sinusoidal under
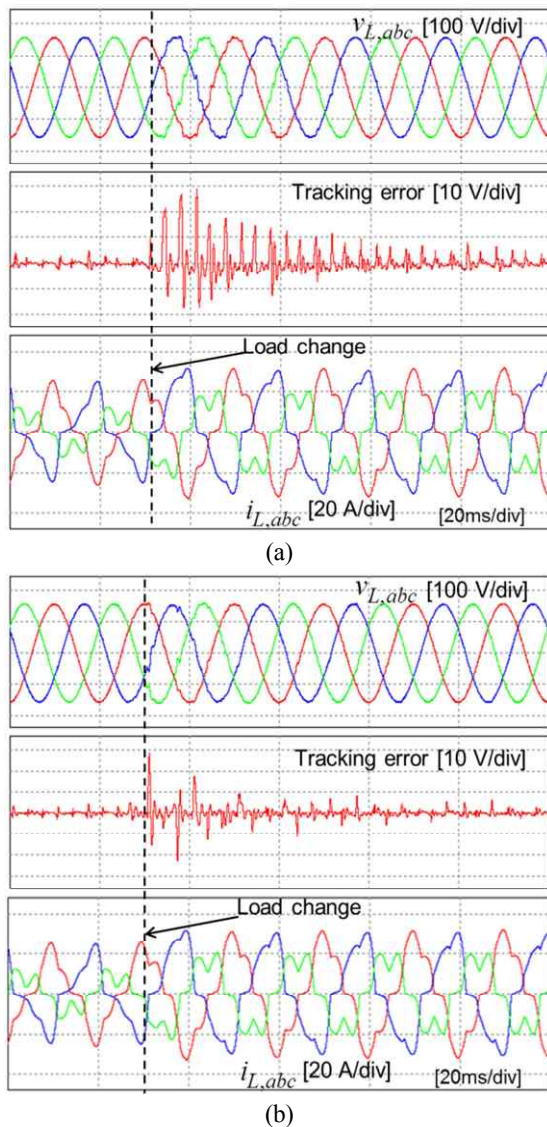
(a)



(b)

Fig. 10. Dynamic response of the DG when the load is changed with (a) the odd-harmonic RC, (b) the proposed control strategy.

various load conditions.

Along with a good steady-state performance, a fast dynamic response under load variations is also a crucial factor for a DG system. The dynamic response of the DG output voltage by using an odd-harmonic RC [17] and the proposed control strategy under a load step change is shown in Fig. 10. In Fig. 10(a), during load changes, the odd-harmonic RC needs more than 90ms to regain a sinusoidal DG output voltage. Since the odd-harmonic RC has a delay time of half a fundamental cycle, it usually needs several fundamental cycles to settle at the steady-state condition after load changes. Meanwhile, in Fig. 10(b), the proposed controller provides a much faster dynamic response. The tracking error becomes almost zero and the DG output voltage can be recovered to be a sinusoidal waveform within about 20ms (one fundamental cycle). From the simulated results, it can be concluded that the proposed

TABLE II
SUMMARRY OF THD VALUE OF DG OUTPUT VOLTAGE

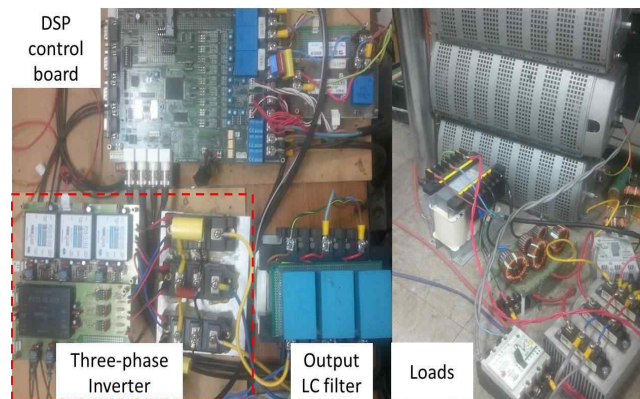| | Previous RC in [15] | | | Proposed controller | | |
|---|---|---|---|---|---|---|
| | Phase A | Phase B | Phase C | Phase A | Phase B | Phase C |
| **Case I** | 0.89% | 0.90% | 0.91% | 0.89% | 0.90% | 0.91% |
| **Case II** | 10.3% | 9.0% | 6.05% | 0.78% | 0.88% | 0.74% |
| **Case III** | 10.5% | 9.5% | 6.7% | 0.91% | 0.98% | 0.94% |



Fig. 11. Experimental system of the DG.

controller offers excellent steady-state performance under various load conditions as well as a very fast dynamic response during load variations.

A summary of the THD value of the DG output voltage with the previous RC and the proposed control strategy are shown in Table II. It can be seen that the proposed control strategy provides a much better performance when compared to the previous RC. The proposed control strategy is always able to keep the THD value of the DG output voltage lower than 1% in all test cases. In contrast, the previous RC can only provide a low THD in case I. It provides very high THD values in case II and case III. Therefore, the proposed control strategy is more general and is more effective under various load conditions.

## VI. EXPERIMENTAL RESULTS

An overview of the experimental system is shown in Fig. 11. All of the parameters in the experimental system are the same as the simulation model given in Table I. The control strategy is carried out by using a floating-point DSP (TMS320F28335 by Texas Instruments). The same three mentioned test cases are carried out experimentally to verify the effectiveness of the proposed control strategy.
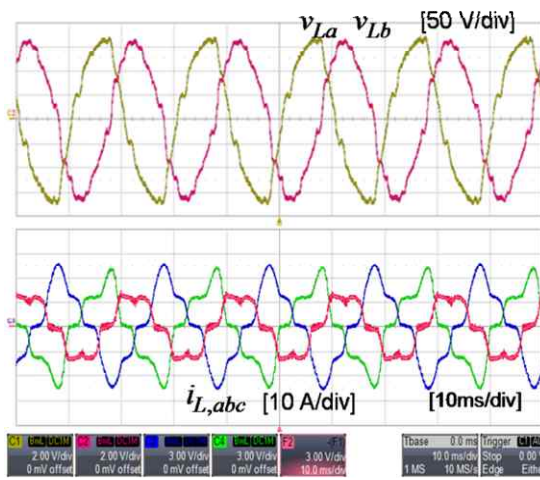
In Fig. 12, the experimental results with the previous RC [15] are shown. According to Fig. 12, which corresponds to the simulation results shown in Fig. 8, the DG output voltage is
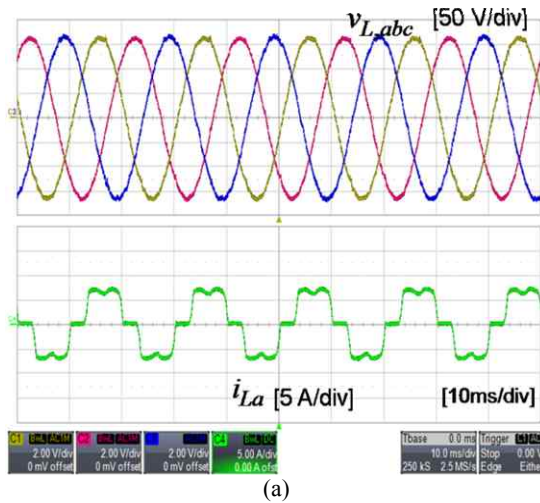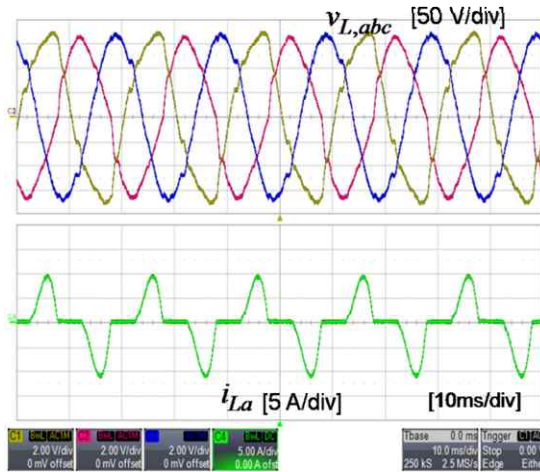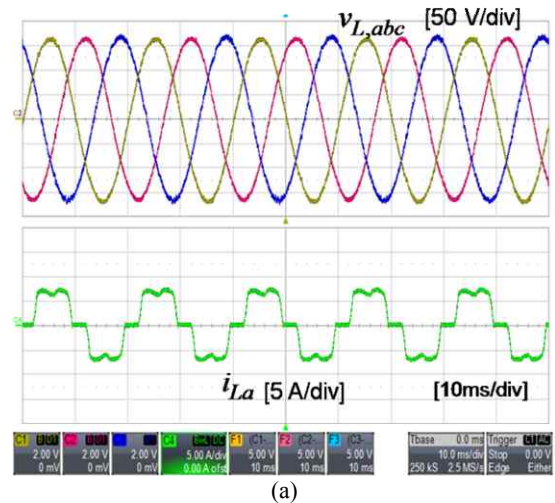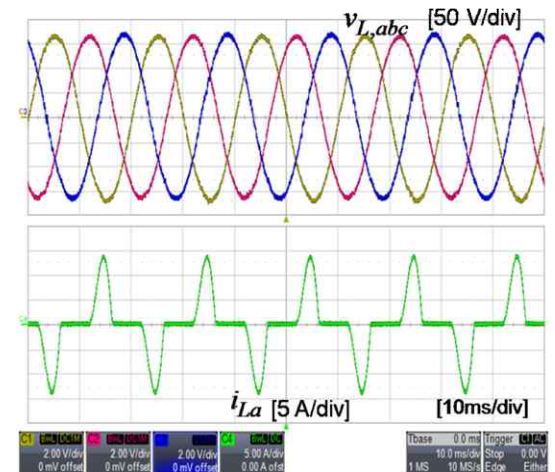
Fig. 12. Steady-state performance of the DG output voltage and load current with the previous RC under (a) case I, (b) case II, (c) case III.



Fig. 13. Steady-state performance of the DG output voltage and load current with the proposed control strategy under (a) case I, (b) case II, (c) case III..
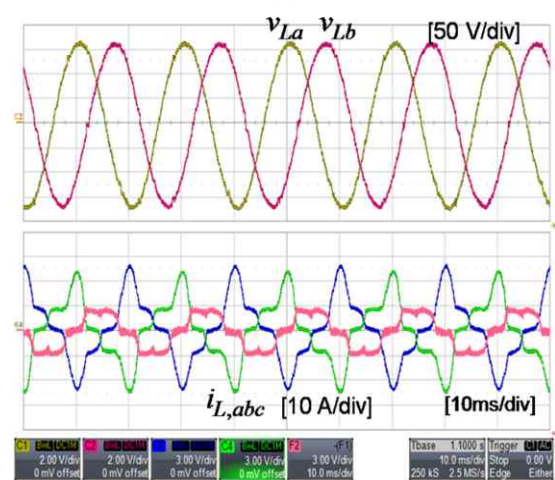
maintained balanced and sinusoidal only under case I, i.e., the three-phase nonlinear load. In the other cases, the DG output voltages become distorted and unbalanced due to the existence of the singe-phase diode rectifier. The presence of triplen

harmonics causes the voltage to become distorted and unbalanced because the previous RC can only compensate the $(6n\pm1)$th harmonics. As a result, the previous RC is unable to
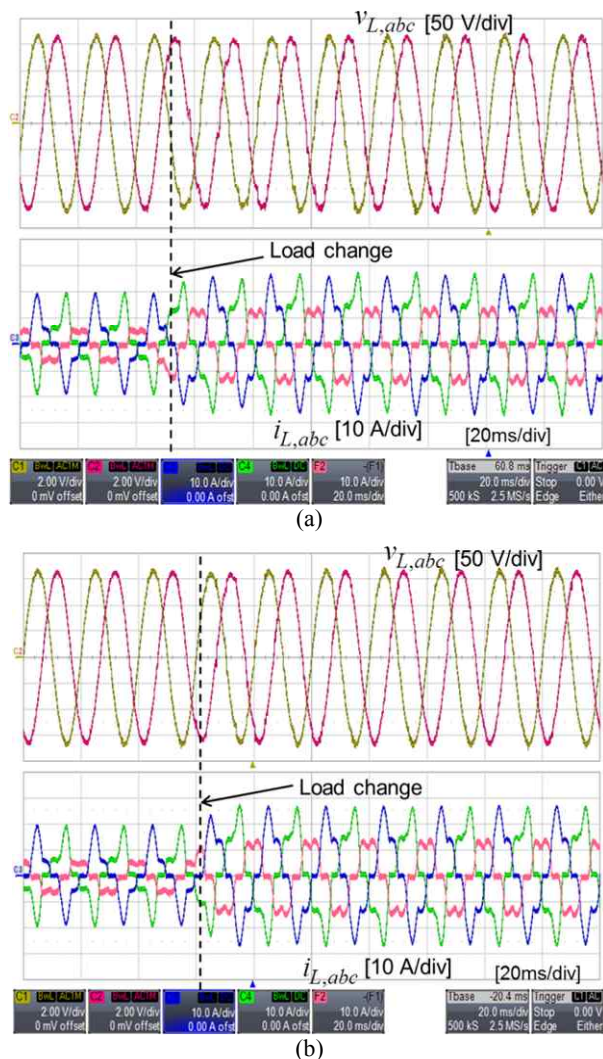
Fig. 14. Dynamic response of the DG when the load is changed with (a) the odd-harmonic RC (b) the proposed control strategy.

provide good control performance under unbalanced nonlinear load conditions.

In contrast, the proposed control strategy effectively regulates the DG output voltage to be sinusoidal in all of the test cases shown in Fig. 13. Since the proposed controller is designed to compensate all of the odd harmonics, the DG output voltage is maintained sinusoidal irrespective of the existence of single-phase or three-phase nonlinear loads. The experimental results coincide very well with those of the simulation.

Along with an improved steady-state performance, the proposed control scheme also offers a fast dynamic response under load step changes. The dynamic response of the DG output voltage using the odd-harmonic RC [17] and the proposed control strategy under load variations is shown in Fig. 14. In Fig. 14(a), when the load changes, the odd-harmonic RC needs about 100ms (five fundamental cycles) to regain a sinusoidal DG output voltage. Meanwhile, in Fig. 14(b), the

proposed controller only needs about 30 ms to make the DG output voltage settle at the steady-state performance after load changes. The fast dynamic response of the proposed harmonic voltage compensator can be seen experimentally.

## VII. CONCLUSIONS

This paper proposed an enhanced harmonic voltage compensator for stand-alone DG systems which is composed of two RCs. The analysis and design of the two RCs were presented in detail in this paper. By designing one RC to regulate the $(6n\pm1)$th harmonics and the other RC to compensate triplen harmonics, the proposed RC is capable of compensating all of the odd harmonics with a faster dynamic response when compared to the traditional RC. As a result, the proposed compensator provides excellent steady-state performance as well as a very fast dynamic response. The feasibility of the proposed control strategy is verified through simulations and experiments. The DG output voltage is regulated to be almost pure sinusoidal with an ultra-low THD under various load conditions including single-phase and three-phase nonlinear and unbalanced loads.

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**Quoc-Nam Trinh** was born in Thanh Hoa, Vietnam, in 1985. He received his B.S. in Electrical Engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2008. He is currently a combined M.S./Ph.D. student at the University of Ulsan, Ulsan, Korea. He is a member of the Korean Institute of Power Electronics (KIPE). His current research interests include distributed generation, active power filters, harmonic compensation, and power quality.

**Hong-Hee Lee** received his B.S., M.S., and Ph.D. in Electrical Engineering from Seoul National University, Seoul, Korea, in 1980, 1982, and 1990, respectively. He is a Professor in the School of Electrical Engineering, University of Ulsan, Ulsan, Korea. He is also the Director of the Network-based Research Center (NARC) at the University of Ulsan. His current research interests include power electronics, network-based motor control, and control networks. He is a Member of the Institute of Electrical and Electronics Engineers (IEEE), the Korean Institute of Power Electronics (KIPE), the Korean Institute of Electrical Engineers (KIEE), and the Institute of Control, Automation, and Systems Engineers (ICASE).

**Tae-Won Chun** was born in Korea in 1959. He received his B.S. in Electrical Engineering from Pusan National University, Pusan, Korea, in 1981, and his M.S. and Ph.D. in Electrical Engineering from Seoul National University, Seoul, Korea, in 1983 and 1987, respectively. Since 1986, he has been a Faculty Member in the Department of Electrical Engineering, University of Ulsan, Ulsan, Korea, where he is currently a Full Professor. His current research interests include the control of electrical machines, power converter circuits, and industrial applications.