# Analytical Model of Double Gate MOSFET for High Sensitivity Low Power Photosensor

Rajni Gautam, Manoj Saxena, R. S.Gupta, and Mridula Gupta

Abstract—In this paper, a high-sensitivity low power photodetector using double gate (DG) MOSFET is proposed for the first time using change in subthreshold current under illumination as the sensitivity parameter. An analytical model for optically controlled double gate (DG) MOSFET under illumination is developed to demonstrate that it can be used as high sensitivity photodetector and simulation results are used to validate the analytical results. Sensitivity of the device is compared with conventional bulk MOSFET and results show that DG MOSFET has higher sensitivity over bulk MOSFET due to much lower dark current obtained in DG MOSFET because of its effective gate control. Impact of the silicon film thickness and gate stack engineering is also studied on sensitivity.

*Index Terms*—Dark current, device simulation, DG MOSFET, high- $\kappa$ , gate stack, photodetector

#### **I. INTRODUCTION**

Due to ever increasing demand of low cost and highly sensitive photodetectors for a variety of applications, ranging from biomedicine [1], optical interconnects [2], optical storage [3] and integrated circuit compatibility of Field- Effect Transistors (FETs) have extended the potential of these devices for their use as photodetectors. High sensitivity, miniaturization, mass-production and reduction of the power consumption are primary interest in the field of MOSFET based photodetectors. MOSFET has been studied theoretically as well as experimentally by several researchers for various optically- controlled applications [4-8]. The possibility of SOI MOSFET as an optically sensitive device was presented by Bosch et al. [4]. A lot of work on analytical model for optically controlled MESFET is available in literature [9, 10]. Up to now all the research work has been focused on improving the photoresponse by implementing methods of enhancing the photocurrent such as use of transparent gate electrode [8], channel material engineering [7], back illumination [9] etc. In the present work, improvement in sensitivity is achieved by lowering the dark current (using device engineering). In this paper, double gate (DG) MOSFET structure has been studied which leads to very low dark currents [11-15] along with ZnO gate for enhanced absorption. Recently Lee et.al. [8] reported bulk MOSFET photodetector using zinc oxide gate. Use of transparent ZnO as gate material has the advantage of less reflection at the upper gate surface so that most of the light incident on the gate reach to the semiconductor.

MESFET and MOSFET based sensors have various advantages over conventional photodetectors i.e. p-n junction photodiode, pin photodiode, avalanche photodiode and BJT (HBT). Various advantages of FET based photodetectors are: low power dissipation, low noise, high input impedance and better temp stability. The conventional p-n junction photodiode suffers from low quantum efficiency [16]. Pin diode gives high sensitivity and fast response time as compared to pn

Manuscript received Dec. 14, 2012; accepted Aug. 1, 2013

R. Gautam and M. Gupta are with the Semiconductor Device Research Laboratory,Department of Electronic Science, University of Delhi, South Campus, New Delhi 110021, India

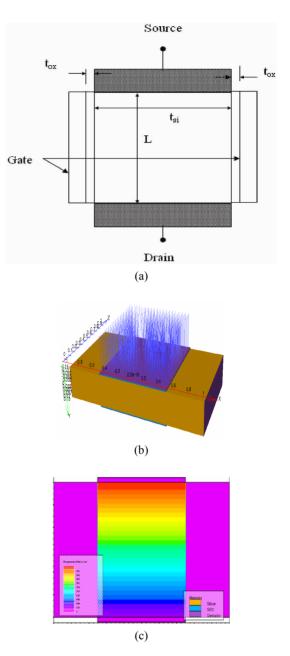
M. Saxena is with the Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, New Delhi 110015, India R. S. Gupta is with the Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, New Delhi 110086, India

E-mail : mridula@south.du.ac.in

junction photodiode [17]. The speed of pin diodes is limited by the transit time of photogenerated carriers across the intrinsic layer. If the width of the intrinsic Si layer is reduced, the quantity of absorbed photons and thus the responsivity will also be reduced. Avalanche photodiode gives high sensitivity but at the cost of increased noise [18]. Thus CMOS image sensors have attracted much attention due to their advantages of low power consumption, random sensor access, and design flexibility [19-21]. MOSFET is better than MESFET in terms of integration techniques. Another advantage of MOSFET is low dark current (i.e. off state current or subthreshold current in our case) and low power consumption. The dark current further reduces in case of DG MOSFET as compared to bulk single gate MOSFET due to better gate controllability. In the present work, the photosensor is baised in subthreshold region thus helps in realizing a low power highly sensitive photodetector. In the present work, an analytical model has been developed for optically controlled DG MOSFET with ZnO gate under illumination and close proximity with simulation results validates the analytical model. Sensitivity of the device is compared with conventional bulk MOSFET with ZnO gate and the impact of silicon film thickness and high- $\kappa$  gate stack on photosensitivity is also studied.

## **II. SIMULATION APPROACH**

DG MOSFET using ZnO gate has been simulated using ATLAS -3D device simulator [22]. Silvaco ATLAS advanced luminous 3D optical device simulator has been used to extract the device characteristics under illumination. Fig. 1(a) shows the schematic structure of DG MOSFET, Fig. 1(b) shows simulated structure of DG MOSFET under illumination and Fig. 1(c) shows the contour plot of photogeneration rate which is decaying exponentially with maximum at top (red colour). Gate metal and gate dielectric are taken to be thin so that most of the incident radiation on the gate region is transmitted to the underlying semiconductor region. Location, intensity and wavelength of the radiation has been set using BEAM statement of the luminous module. Real and imaginary values of refractive index for calculation of reflection coefficient at the gate surface for ZnO gate are taken from SOPRA database [23]. Ray trace method has been used in simulator to solve for photogeneration



**Fig. 1.** (a) Schematic structure of DG MOSFET with ZnO gate, (b) Simulated structure of DG MOSFET under illumination, (c) contour plot of photogenearation Rate. Device parameters are: channel length L=1  $\mu$ m, channel width W=1  $\mu$ m, oxide thickness t<sub>ox</sub>=10 nm, thickness of silicon t<sub>si</sub>=0.3  $\mu$ m, source/ drain doping N<sub>D</sub>=1×10<sup>20</sup> cm<sup>-3</sup>, substrate doping N<sub>A</sub>=1×10<sup>16</sup> cm<sup>-3</sup>.

rate at each grid point. Various models used in simulation are: field dependent mobility model to incorporate parallel field dependence of mobility, SRH recombination model to include minority recombination effect. Quantum effects are not taken into account.

#### **III. MODEL FORMULATION**

To detect the light, an optical radiation (of energy greater than bandgap energy of the semiconductor) is incident on the upper gate of the DG MOSFET resulting in the generation of EHP due to the absorption of incident photons. The generation rate is given by:

$$G_{op} = \alpha \phi_{op} \tag{1}$$

where  $\alpha$  is the optical absorption coefficient per unit length and  $\phi_{OP}$  is the photon flux density given by [10]:

$$\phi_{op} = P_{op} \frac{h}{c\lambda} (1 - R_1) (1 - R_2) (1 - R_3)$$
(2)

Here,  $P_{op}$  is the optical power intensity, *h* is the Planck's constant, *c* is the velocity of light,  $\lambda$  is the wavelength of the incident radiation and  $R_1$ ,  $R_2$  and  $R_3$  are the reflection coefficients at the air-gate interface, gate to oxide interface and oxide to semiconductor interface respectively. Reflection coefficients are calculated as [10]:

$$R_{i} = \frac{\left(n_{j} - n_{j+1}\right)^{2} + k_{j+1}^{2}}{\left(n_{j} + n_{j+1}\right)^{2} + k_{j+1}^{2}}$$
(3)

Here j=1,2,3 for air to gate, gate to oxide and oxide to semiconductor interface respectively.  $n_1$ ,  $n_2$ ,  $n_3$  and  $n_4$  are the refractive index of air, gate material (ZnO), oxide and semiconductor respectively and  $k_i$ 's are the corresponding absorption constants. The holes diffuse toward the source electrode and the electrons toward the drain electrode. This results in the development of a photovoltage  $V_{op}$  across the source film junction which increases the effective gate to source bias  $V_{GS}$ . The photovoltage developed is given as [4, 10]:

$$V_{op} = \frac{kT}{q} \left( \frac{\ln(1 + \alpha \phi_{op} \tau (1 - \exp(-\alpha t_{si}))))}{J_s} \right)$$
(4)

where  $J_s$  is the saturation current of the reversed biased source-film junction [4] and  $\tau$  is the carrier lifetime. Potential distribution in silicon film is obtained by solving:

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = \frac{q \left( N_A - \phi_{op} \alpha \tau e^{-\alpha y} \right)}{\varepsilon_{si}} \quad (5)$$

where  $\varphi(x, y)$  is the potential distribution in the silicon film,  $N_A$  is the doping in the silicon film, q is the electron charge,  $\tau$  is the electron lifetime, and  $\varepsilon_{si}$  is the dielectric permittivity of silicon. The potential distribution in the silicon film is assumed to be parabolic in the vertical direction and is given as:

$$\varphi(x, y) = A_o(x) + A_1(x)y + A_2(x)y^2$$
(6)

The boundary conditions required for the solution of potential  $\varphi(r, z)$  are as follows.

1. The electric field at the center of silicon film is zero:

$$\left. \frac{d\varphi(x,y)}{dy} \right|_{y=\frac{t_{si}}{2}} = 0 \tag{7}$$

2. The electric field at the silicon oxide interface is given by:

$$\frac{d\varphi(x,y)}{dy}\Big|_{y=0} = \frac{C_{ox}}{\varepsilon_{si}} (V_{gs} + V_{op} - V_{fb} - \varphi_s(x))$$
(8)

where  $V_{fb}$  is the flat band voltage,  $V_{GS}$  is the gate to source voltage,  $C_{ox}$  is the gate oxide capacitance given by  $\frac{\varepsilon_{ox}}{t_{ox}}$ ,  $\varepsilon_{ox}$  is the dielectric permittivity of oxide,  $t_{si}$  is the silicon film thickness, and  $t_{ox}$  is the oxide layer thickness.

Applying boundary conditions and substituting  $A_o(x)$ ,  $A_1(x)$  and  $A_2(x)$  in Eq. (6), we get:

$$\varphi(x,y) = \varphi_s(x) + \frac{C_{ox}}{\varepsilon_{si}} (\varphi_s(x) - V_{gs} - V_{op} + V_{fb}) y + \frac{C_{ox}}{\varepsilon_{si} t_{si}} (\varphi_s(x) - V_{gs} - V_{op} + V_{fb}) y^2$$
(9)

Now substituting (9) in (5), we obtain

$$\frac{\partial^2 \varphi_s(x)}{\partial x^2} - \frac{\varphi_s(x)}{\omega^2} = P$$
(10)

where

$$\omega = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}}} \tag{11}$$

$$P = \frac{q\left(N_A - \phi_{op}\alpha\tau\right)}{\varepsilon_{si}} - \frac{V_{gs} + V_{op} - V_{fb}}{\omega^2}$$
(12)

Solution of (10) is given by:

$$\varphi_{S}\left(x\right) = \frac{A \sinh\left(\frac{x}{\omega}\right) - B \sinh\left(\frac{x-L}{\omega}\right)}{\sinh\left(\frac{L}{\omega}\right)} - \omega^{2}P \qquad (13)$$

Applying boundary conditions at source and drain, *A* and *B* are calculated as:

$$A = \omega^2 P + V_{ds} \tag{14}$$

$$B = \omega^2 P + V_{bi} \tag{15}$$

Subthreshold current for DG MOSFET which serves as the dark current for the photodetector is given by:

$$I_{sub} = Z \mu K T n_i \frac{e^{-q \frac{V_{ds}}{KT}}}{\int \frac{1}{\int \frac$$

Here  $\mu$  is the electron mobility,  $n_i$  is the intrinsic carrier concentration, K is the boltzman constant, T is the temperature. Under illumination an additional current  $I_{ph}$  is added to the drain current  $I_{sub}$  so that total current under illumination is:

$$I_{DS} = I_{sub} + I_{ph} \tag{17}$$

 $I_{ph}$  is calculated by integrating photogenerated charge as follows [10]:

$$I_{ph} = \mu \frac{Z}{L} \int_{0}^{V_{ds} t_{si}} \int_{0}^{t_{si}} \phi_{op} \alpha \tau \exp(-\alpha y) dy dV \qquad (18)$$

In case of gate stack, two dielectric layers (Al<sub>2</sub>O<sub>3</sub> having dielectric constant  $\mathcal{E}_{r2}=9$  and thickness  $t_{ox2}=8$  nm above SiO<sub>2</sub> layer having dielectric constant  $\mathcal{E}_{r1}=3.9$  and thickness  $t_{ox1}=2$  nm) are used. In case of DG MOSFET with gate stack, effective oxide thickness  $t_{ox}$  used for calculation of electric potential is given by:

$$t_{ox} = t_{ox1} + \frac{\varepsilon_{r1}}{\varepsilon_{r2}} t_{ox2}$$
(19)

For gate stack device under illumination, one more reflection coefficient is added to account for reflection of light taking place at high- $\kappa$  (Al<sub>2</sub>O<sub>3</sub>) to SiO<sub>2</sub> interface, therefore (2) is replaced by:

$$\phi_{op} = P_{op} \frac{h}{c\lambda} (1 - R_1) (1 - R_2) (1 - R_3) (1 - R_4) \quad (20)$$

where  $R_3$  and  $R_4$  are the reflection coefficients at the interfaces Al<sub>2</sub>O<sub>3</sub> to SiO<sub>2</sub> and SiO<sub>2</sub> to Si respectively.

## **IV. RESULT AND DISCUSSION**

Table 1 shows the optical properties of ZnO [17], SiO<sub>2</sub> and Si as a function of wavelength which are used in modeling and simulation. Amount of light reaching to the semiconductor depends upon the reflection at the various interfaces i.e.  $R_1$ ,  $R_2$  and  $R_3$  which are calculated using (4) and are shown in Table 1. In simulation, only  $R_3$ could be extracted and is shown in Fig. 2 along with its analytically calculated value. As can be seen from Fig. 2, reflection coefficient R3 decreases as wavelength is increased thus indicating more absorption at higher wavelengths. Fig. 2 also shows the simulated and analytically calculated photogeneration rate (i.e.  $G_{on}$ calculated using Eqs. (2) and (3)).  $G_{op}$  first increases with  $\lambda$  reaching maximum and then decreases depending upon three factors i.e. 1) directly proportional to the absorption coefficient of the semiconductor which decreases with increase in wavelength, 2) indirectly proportional to wavelength of the incident radiation ( $\lambda$ ) and 3) directly proportional to  $(1-R_1)(1-R_2)(1-R_3)$  which increases with increase in wavelength. According to first two points (Last point), Gop decreases (increases) with increasing wavelength thus at lower wavelength last factor

	ZnO			SiO <sub>2</sub>		Si			
λ (μm)	n	k	$R_1$	n	$R_2$	n	k	R <sub>3</sub>	$\begin{array}{c} \alpha \\ (\text{cm}^{\text{-1}}) \\ \times 10^6 \end{array}$
0.25	1.92	0.383	0.115	1.6	0.008	1.58	3.63	0.56	1.827
0.3	1.99	0.404	0.126	1.578	0.013	5.0	4.168	0.48	1.746
0.35	2.14	0.457	0.15	1.565	0.024	5.43	2.989	0.41	1.073
0.4	2.27	4×10 <sup>-3</sup>	0.151	1.557	0.035	5.57	0.387	0.31	0.121
0.45	2.11	4×10 <sup>-18</sup>	0.127	1.552	0.023	4.67	0.139	0.25	0.03886
0.5	2.05	0	0.119	1.548	0.019	4.29	0.069	0.22	0.01746
0.55	2.02	0	0.114	1.545	0.018	4.08	0.043	0.20	0.00985

**Table 1.** Optical properties of ZnO,  $SiO_2$  and Si as a function of wavelength of the incident radiation. Imaginary refractive index for an insulator ( $SiO_2$ ) is zero

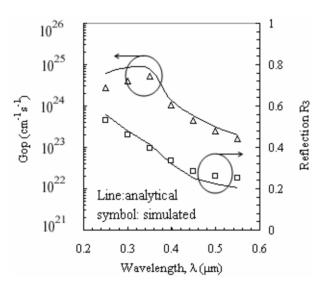
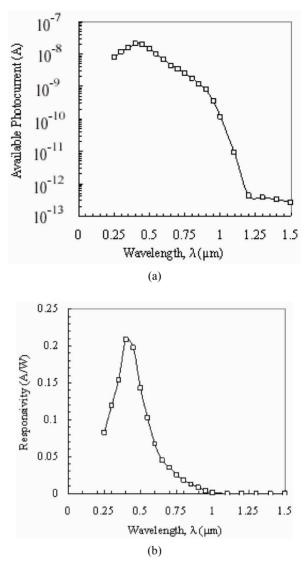


Fig. 2. Photogeneration rate and reflection coefficient  $R_3$  as a function of wavelength. Line: analytical, symbol: simulated.  $P_{op}=10\times10^{-8} \text{ W/}\mu\text{m}^2$ .

dominates whereas at larger wavelengths first two factors dominates. The sensing material used in the present work is silicon and in some cases maximum responsivity is obtained in the range of 800-1000nm for a silicon photodetector as reported in [24, 25]. However, the peak wavelength corresponding to maximum responsivity depends upon many factors such as: absorption coefficient of the silicon, reflection coefficient at the surface, surface recombination and thickness of the silicon body. In the present work, it is a MOSFET based photodetector with ZnO gate and light reaching to silicon is subjected to reflection at three interfaces i.e. air to ZnO, ZnO to SiO<sub>2</sub> and SiO<sub>2</sub> to Si thus overall spectral response will depend upon the three reflection coefficients along with the other parameters.

Fig. 3(a) shows the available photocurrent as a



**Fig. 3.** (a) Available photocurrent as a function of wavelength.  $P_{op}=10\times10^{-8} \text{ W/}\mu\text{m}^2$ ,  $V_{GS}=0.0 \text{ V}$ ,  $V_{DS}=0.05 \text{ V}$ , (b) Responsivity as a function of wavelength.  $P_{op}=10\times10^{-8} \text{ W/}\mu\text{m}^2$ ,  $V_{GS}=0.0 \text{ V}$ ,  $V_{DS}=0.05 \text{ V}$ .

function of wavelength and it clearly shows the maximum photocurrent is available at around 0.4  $\mu$ m wavelength of the incident light because at this wavelength maximum amount of light is reaching to the semiconductor. Fig. 3(b) shows the optical response for the ZnO-SiO<sub>2</sub>-Si system over a range from 0.25  $\mu$ m to 1.5  $\mu$ m. This type of behavior where maximum responsivity is obtained at lower wavelengths is also reported in [26-30]. As is clear from the Fig. 3(b), device shows a decent responsivity in the range 0.25  $\mu$ m to 0.6  $\mu$ m with peak responsivity at lamda=0.4  $\mu$ m for t<sub>si</sub>=0.3  $\mu$ m and at  $\lambda$ =0.5  $\mu$ m for t<sub>si</sub>=0.5  $\mu$ m. Thus it is capable for

detection mainly in UV, visible region. Photodetection in the visible-light zone is of great importance for various applications including environmental and biological research, sensing, detection, missile launch and imaging applications [31]. Various applications of UV detectors are UV dosimetry and imaging, solar UV measurements and astronomical studies, flame sensors (fire alarm systems, missile plume detection, combustion engine control) and biological and chemical sensors (ozone detection, determination of pollution levels in air, biological agents detection etc.) [32, 33]. The maximum responsivity wavelength lies at the edge of blue and violet light. Detection at blue/violet light is also very important for biomedical applications as reported in [34, 35]. Fig. 4 compares the impact of light on the  $I_{DS}$ - $V_{GS}$ characteristics of MOSFET and DG MOSFET when both devices are optimized for same threshold Voltage under dark condition. Comparison is performed in terms of sensitivity parameter. Sensitivity (I<sub>illumination</sub>/I<sub>dark</sub>) in subthreshold region (i.e.  $V_{GS} = 0$  V,  $V_{DS} = 0.05$  V) is  $10^3$ for bulk MOSFET and 10<sup>4</sup> for DG MOSFET. It clearly shows that DG MOSFET is a better candidate for photosensing applications because it has lower dark current and enhanced photo sensitivity due to its effective gate control and improved subthreshold characteristics. Fig. 5 illustrates the impact of light on the  $I_{DS}$ -V<sub>GS</sub> characteristics of DG MOSFET for various intensities of light. It clearly shows that higher is the light intensity, greater is the change in drain current. Also change in current due to illumination is much higher in subthreshold region than that in linear and saturation region. This is because magnitude of photogenerated current is much higher than the dark current in subthreshold region whereas it is comparable to dark current in saturation region. Thus, in the present work, subthreshold region is exploited for calculation of photosensitivity (in terms of ratio of off current under dark to the off current under illumination condition. Thus device is biased at a gate to source voltage ( $V_{GS}$ ) less than the threshold voltage and maximum sensitivity is obtained at V<sub>GS</sub>=0 V. Therefore the operating voltages are: gate to source voltage (V<sub>GS</sub>)=0 V, drain to source voltage (V<sub>DS</sub>)=0.05 V.

Fig. 6 shows  $I_{DS}$ - $V_{GS}$  characteristics at different wavelengths of light. It shows that highest  $I_{illumination}/I_{dark}$  is obtained at  $\lambda$ =0.4 $\mu$ m. Thus silicon DG MOSFET

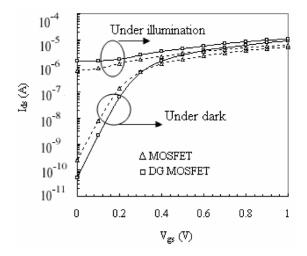


Fig. 4. Sensitivity comparison between DG MOSFET and bulk MOSFET photodetector at  $\lambda$ =0.25 µm,  $P_{op}$ =10×10<sup>-8</sup> W/µm<sup>2</sup>,  $V_{DS}$ =0.05 V.

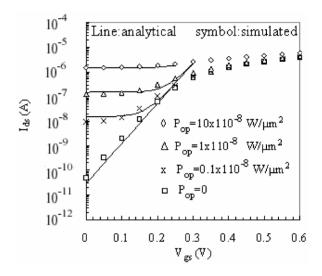
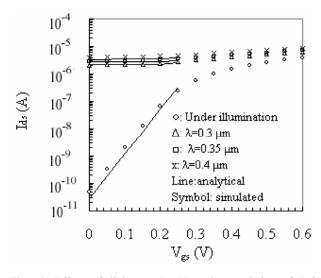


Fig. 5. Effect of light on  $I_{DS}$ -V<sub>GS</sub> characteristics of DG MOSFET at different light intensities.  $\lambda$ =0.25 µm, V<sub>DS</sub> = 0.05 V.

photodetector with ZnO gate shows maximum photo sensitivity at  $\lambda$ =0.4 µm. Close proximity of analytical results with simulation results at various intensity and wavelength of light validates the analytical model. Sensitivity of the DG MOSFET photodetector also depends on the thickness of the silicon film ( $t_{si}$ ) because subthreshold current which is also the dark current in this case is very much dependent on silicon silicon film thickness  $t_{si}$ . For effective absorption,  $t_{si}$  should be equal or greater than  $1/\alpha$  giving photoabsorption on larger area and thus higher photogenerated current. At the same time, larger  $t_{si}$  leads to higher off current giving larger dark current. At smaller wavelengths (with condition  $t_{si} > 1/\alpha$  is



**Fig. 6.** Effect of light on  $I_{DS}$ - $V_{GS}$  characteristics of DG MOSFET at different wavelengths of incident light radiation. Line: analytical, Symbols: simulated,  $\Box$ :  $\lambda$ =0.35 µm, x:  $\lambda$ =0.4 µm,  $\Delta$ :  $\lambda$ =0.3 µm,  $\circ$ : under dark.  $P_{op}$ =10×10<sup>-8</sup> W/µm<sup>2</sup>,  $V_{DS}$ =0.05 V.

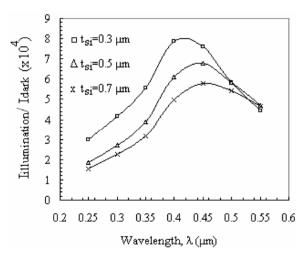


Fig. 7. Impact of silicon film thickness on sensitivity of the photodetector as a function of wavelength.  $P_{op}=10\times10^{-8}$  W/µm<sup>2</sup>.

maintained), larger  $t_{si}$ leads to reduction in photosensitivity. This is because order of decrease in dark current is much more than the order of increase in illumination current. Thus, when t<sub>si</sub> is increased from 0.3  $\mu$ m to 0.7  $\mu$ m, sensitivity is reduced by 48% at  $\lambda$ =0.4  $\mu$ m as shown in Fig. 7. But this is not the case at larger wavelengths ( $\lambda$ >0.5 µm), because at larger wavelengths, absorption coefficient is very small so it requires thick semiconductor film for absorption and photogeneration. Table 2 shows the impact of light on the electrical characteristics of the DG MOSFET. Change in threshold Voltage  $(V_{th})$ , off current  $(I_{off})$  and  $I_{on}/I_{off}$  ratio can be used

**Table 2.** Change in threshold Voltage (V<sub>th</sub>),  $I_{on}$ ,  $I_{off}$  and  $I_{on}/I_{off}$  ratio as a function of light intensity  $\lambda$ =0.25 µm

$\begin{array}{c} P_{op} \times 10^{-8} \\ W/\mu m^2 \end{array}$	V <sub>th</sub> (V)	I <sub>on</sub> (µA)	I <sub>off</sub> (nA)	$I_{\rm on}/I_{\rm off}$
0	0.35	8.82	0.05	1.75×10 <sup>5</sup>
0.1	0.34	8.85	9.58	9.25×10 <sup>2</sup>
1	0.3	9.16	128	7.16×10 <sup>1</sup>
10	0.19	10.8	1500	7.19

to extract the intensity of light falling on the gate area of DG MOSFET as illustrated in Table 2. Since  $I_{off}$  shows exponential increase upon illumination, therefore device should be biased in subthreshold region for effective detection of light. In the earlier reported work [36, 37], MOSFET is basically used to amplify the detected signal and either threshold voltage or drain to source current in on state is used as the sensitivity parameter. The photogenerated current is analogous of gate signal which changes the threshold voltage and drain current of the device. But in the present work, MOSFET itself is the sensing element and subthreshold region is exploited for calculation of photosensitivity as change in subthreshold current changes exponentially under illumination thus ratio of off current under dark to the off current under illumination condition is used as the sensitivity parameter. Since MOSFET has very low off current as compared to other conventional devices thus low off current implies small dark current thus enhanced sensitivity for photo detection. Apart from high sensitivity, operating device in subthreshold region has the advantage of low power consumption [38, 39] thus it helps in realizing the concept of low power highly sensitive sensors and also compatible with CMOS integration. In that sense DG MOSFET is even better than bulk MOSFET because of further lower off current due to effective gate control [39, 40]. Also sensitivity can be enhanced by decreasing silicon film thickness but it cannot be scaled much because for absorption  $t_{si} > 1/\alpha$  condition must be maintained. Therefore, at higher wavelengths (where  $\alpha$  is very small) and larger silicon body thickness, another method should be explored to enhance the sensitivity by reduction in dark current without affecting the photocurrent. One such method is use of high- $\kappa$  gate stack engineering. High- $\kappa$  gate stack architecture leads to further lower dark current and thus results in enhancement in sensitivity of the DG MOSFET photodetector as shown in Fig. 8.

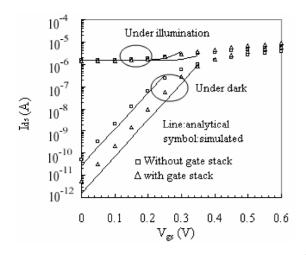


Fig. 8. Impact of gate stack on photosensitivity.  $P_{op}=10x10^{-8}$  W/µm<sup>2</sup>,  $\lambda=0.25$  µm.

Although gate stack also leads to one more reflection term at the high- $\kappa$  oxide to silicon dioxide interface but the order of reduction in dark current is much higher than the loss in power available to the semiconductor due to additional reflection at the high- $\kappa$  to SiO<sub>2</sub> interface. Using gate stack, dark current reduces from 50 pA to 5 pA whereas current under illumination remains almost unchanged thus sensitivity is improved (i.e. enhanced by 9 times) as shown in Fig. 8.

## V. CONCLUSIONS

DG MOSFET with ZnO gate shows 10 times higher sensitivity (over bulk MOSFET with ZnO gate) towards detection of light. For effective detection, device should be biased in subthreshold region as change in  $I_{off}$  (upon illumination) shows higher sensitivity and low power operation. The maximum sensitivity (i.e.  $I_{illumination}/I_{dark}$ ratio= $8 \times 10^4$ ) is obtained at wavelength of  $0.4 \mu m$ . Effective gate control, low leakage current, low power operation, ideal subthreshold characteristics of DG MOSFET combined with transparency of ZnO in visible region make DG MOSFET with ZnO gate a promising candidate for ultrasensitive, small, low-power, low cost, reliable CMOS based light sensor. Sensitivity can further be increased by decreasing silicon film thickness (maintaining  $t_{si} > 1/\alpha$ ) for smaller wavelengths. For larger wavelengths, high- $\kappa$  gate stack can be used to further enhance the sensitivity even with thick silicon body. If device is to be used for photosensing applications the

ideal operation bias point lies in the subthreshold region where the sensitivity to the optical intensity is very high. But for certain applications like electrical switching where a device is needed to have less sensitivity to optical intensity, it is required to bias the device at higher value of gate to source voltage (V<sub>GS</sub>). So the operating bias point here decides the sensitivity to the optical intensity. And in terms of design parameters, the gate material engineering is the second option to make the device less sensitive to optical intensity at a particular wavelength. For example, ZnO (i.e. gate material in the present work) is transparent to visible light thus maximum light is reached to the underlying semiconductor where absorption takes place. But ZnO absorbs UV light so the overall effect would be less sensitivity to optical intensity in UV region as compared to visible region. Similarly other gate materials can be used according to the required wavelength of interest.

#### **ACKNOWLEDGMENTS**

The authors are thankful to the DRDO and one of the authors (Rajni Gautam) is thankful to UGC, Government of India for providing the necessary financial assistance to carry out this research work.

#### REFERENCES

- H. Ouyang, C. C. Striemer, and P. M. Fauchet, "Quantitative analysis of the sensitivity of porous silicon optical biosensors", *Appl. Phys. Lett.* Vol.88, pp.163108-163108-3, 2006.
- [2] F. Gan, L. Hou, G. Wang, H. Liu, and J. Li, "Optical and recording properties of short wavelength optical storage materials", *Mater. Sci. Eng.*, Vol. B 76, pp.63-68, 2000.
- [3] H. Cho, P. Kapur, and K. C. Saraswat, "Power comparison between highspeed electrical and optical interconnects for interchip communication," *J. Lightw. Technol.*, Vol. 22, pp.2021–2033, 2004.
- [4] R. Wemer, C. Zimmermann, and A. Kalz, "Light Dependence of Partially Depleted SOI-MOSFET's Using SIMOX Substrates", *IEEE Trans. On Elec. Dev.*, Vol. 42, No. 9, pp. 1653- 1656, 1995.
- [5] T. Yamagata and K. Shimomura, "Optically Controlled Metal –Oxide Semiconductor Field

Effect Transistor Operated by Long –Wavelength Light", *Jpn. J. Appl. Phys.*, Vol.35, pp.L1589-1592, 1996.

- [6] A. K. Okyay, D. Kuzum, S. Latif, D. A. B. Miller, and K. C. Saraswat, "Silicon Germanium CMOS Optoelectronic Switching Device: Bringing Light to Latch", *IEEE Transactions On Electron Devices*, Vol. 54, 3252-3259, 2007.
- [7] Y. Liu, K. Gopalafishan, P. B. Griffin, K. Ma, M. D. Deal, J. D. Plummer, "MOSFETs and High-speed Photodetectors on Ge-on-Insulator Substrates Fabricated Using Rapid Melt Growth", *IEDM*, pp 1001-1004, 2004.
- [8] E. Lee, D. Moon, J. H. Yang, K. S. Lim, and Y. K. Choi, Transparent Zinc Oxide Gate Metal–Oxide– Semiconductor Field-Effect Transistor for High-Responsivity Photodetector", *IEEE Electron Device Letters*, Vol. 30, No. 5, pp. 493-495, 2009.
- [9] N. S. Roy, B. B. Pal, and R. U. Khan, "Analysis of GaAs OPFET with Improved Optical Absorption under Back Illumination", *IEEE Transactions On Electron Devices*, Vol.46, pp.2351-2353, 1999.
- [10] P. Chakrabarti, N. L. Shrestha, S. Srivastava, and V. Khemka, "An Improved Model of Ion-Implanted GaAs OPFET", *IEEE Trans. on Elec. Dev.*, Vol. 39, No. 9, pp. 2050-2059, 1992.
- [11] J. S. Martin, A. Bournel, P. Dollfus, Comparison of multiple-gate MOSFET architectures using Monte Carlo simulation, *Solid-State Electron*. Vol.50, pp.94-101, 2006.
- [12] A.Tsormpatzoglou, C. A. Dimitriadis, R. Clerc,Q. Rafhay, G. Pananakakis, and G. Ghibaudo, , "Semi-Analytical Modeling of Short-Channel Effects n Si and Ge Symmetrical Double-Gate MOSFETs", *IEEE Transactions On Electron Devices*, Vol.4, No.8, pp. 1943-1952, 2007.
- [13] H. Kang, J. W. Han, and Y. K. Choi, "Analytical Threshold Voltage Model for Double-Gate MOSFETs With Localized Charges", *IEEE Elec. Dev. Lett.*, Vol. 29, No. 8, pp. 927-930, 2008.
- [14] H. Liu, Z. Xiong, J. K. O. Sin, P. Xuan, J. Bokor, "A High Performance Double-Gate SO1 MOSFET Using Lateral Solid Phase Epitaxy", 2002 IEEE International SO1 Conference, pp.28-29, October 2002.
- [15] Y. Taur, X. Liang, W. Wang, and H. Lu, "A Continuous, Analytic Drain-Current Model for DG

MOSFETs", *IEEE Electron Device Letters*, Vol. 25, 107-109, 2004.

- [16] H. Zimmermann, "Integrated high speed, high sensitivity photodiodes and optoelectronic integrated circuits," *Sens. Mater.*, Vol. 13, No. 4, pp. 189–206, 2001.
- [17] R. A. Ismail, W. K. Hamoudi, "Characteristics Of Novel Silicon Pin Photodiode Made By Rapid Thermal Diffusion Technique", *Journal of Electron Devices*, Vol. 14, pp. 1104-1107, 2012.
- [18] A. Stoykov, and R. Scheuermann. "Silicon Avalanche Photodiodes." *Laboratory for Muon Spin Spectroscopy, Paul Scherrer Institut*, 2004.
- [19] M. Schanz, W. Brockherde, R. Hauschild, B. J. Hosticka, and M. Schwarz, "Smart CMOS image sensor arrays," *IEEE Trans. Electron Devices*, Vol. 44, No. 10, pp. 1699–1705, Oct. 1997.
- [20] B. Ackland and A. Dickinson, "Camera-on-a-chip," in Proc. ISSCD Tech. Papers, pp. 22–25, 1996.
- [21] E. R. Fossum, "Active pixel sensors: Are CCD's dinosaurs?," in Proc. SPIE Charge-Coupled Devices Solid-State Optical Sensors", Vol. 1900, pp. 2–14, 1993.
- [22] ATLAS User's Manual: 3-D Device Simulator, SILVACO International, Version 5.14.0.R, 2010.
- [23] SOPRA infobase, http://refractiveindex.info.
- [24] S.M.Sze, "Physics of semiconductor Devices, 2<sup>nd</sup> edition, John Wiley and Sons, pp.804.1981.
- [25] O. Bazkir, "Quantum Efficiency Determination of Unbiased Silicon Photodiode And Photodiode Based Trap Detectors", *Rev.Adv.Mater.Sci.* Vol.21, pp.90-98, 2009.
- [26] H.-D. Um, S. A. Moiz, K. T. Park, J. Y. Jung, S. W. Jee, C. H. Ahn, D. C. Kim, H. K. Cho, D. W. Kim, and J. H. Lee, "Highly selective spectral response with enhanced responsivity of *n*-ZnO/*p*-Si radial heterojunction nanowire photodiodes, *Applied Physics Letters*, Vol.98, pp.033102-3, 2011
- [27] M. L. Simpson,, M. N. Ericson, G. E. Jellison, Jr.,W. B. Dress, A. L. Wintenberg, and M. Bobrek, "Application Specific Spectral Response with CMOS Compatible Photodiodes", *IEEE Transactions on Electron Devices*, Vol. 46, no. 5, pp. 905-913, May 1999.
- [28] S.N. Chattopadhyay, C. B. Overton, S. Vetter, M. Azadeh, B. H. Olson, and N. El Naga, "Optically Controlled Silicon MESFET Fabrication and

CharacterizationsforOpticalModulator/Demodulator",JournalofSemiconductorTechnologyandScience,No.3, pp. 213-224, September, 2010.Vol.10,

- [29] A. V. Shah, H. Schade, M. Vanecek, J. Meier, E. Vallat-Sauvain, N.Wyrsch, U. Krol, C. Droz and J. Bailat, "Thin-film Silicon Solar Cell Technology", Progress In Photovoltaics: Research And Applications", *Prog. Photovolt: Res. Appl.*, Vol.12, pp.113–142, 2004.
- [30] P. R. Rao, X. Wang, A. J. P. Theuwissen, "Degradation of Spectral Response and Dark Current of CMOS Image Sensors in Deep-Submicron Technology due to γ-Irradiation", *in the proc. of Solid State Device Research Conference* (ESSDERC), 11-13 Sept. 2007, pp. 370 – 373.
- [31] Z. Zhan, L. Zheng, Y. Pan, G. Sun and L. Li, "Selfpowered, visible-light photodetector based on thermally reduced grapheme oxide–ZnO (rGO– ZnO) hybrid nanostructure" *J. Mater. Chem.*, Vol. 22, pp.2589–2595, 2012.
- [32] F. Omnès, E. Monroy, E. Muñoz, J. L. Reverchon, "Wide bandgap UV photodetectors : A short review of devices and Applications", *Proc. of SPIE*, Vol. 6473, pp. 64730E-15, 2007.
- [33] K. Liu , M. Sakurai and M. Aono, "ZnO-Based Ultraviolet Photodetectors", *Sensors*, Vol. 10, pp. 8604-8634, 2010.
- [34] M. L. F. Lerch, A. B. Rosenfeld, P. E. Simmonds, G. N. Taylor, S. R. Meikle, and V. L. Perevertailo, "Spectral Characterization of a Blue-Enhanced Silicon Photodetector", *IEEE Transactions on Nuclear Science*, Vol. 48, No. 4, pp. 1220-1224, August 2001
- [35] H. Zhitao, C. Jinkui, M. Fantao and J. Rencheng, "Design and simulation of blue/violet sensitive photodetectors in silicon-on-insulator", *Journal of Semiconductors*, Vol. 30, No. 10, pp. 104008-4, October 2009.
- [36] W. Zhang, M. Chan, R. Huang and P.K. Ko, "High Responsivity Photo-Sensor Using Gate Body Tied SOI MOSFET", *Proceedings IEEE International* SOI Conference, pp.149-150, Oct. 1998.
- [37] R. Wemer, C. Zimmermann, and A. Kalz, "Light Dependence of Partially Depleted SOI-MOSFET' s Using SIMOX Substrates", *IEEE Trans. On Elec. Dev.*, Vol. 42, No. 9, pp. 1653- 1656, 1995.

- [38] R. Vaddi, S. Dasgupta, and R. P. Agarwal, "Device and Circuit Design Challenges in the Digital Subthreshold Region for Ultralow-Power Applications", *VLSI Design*, Vol. 2009, Article ID 283702, 14 pages, 2009.
- [39] J.-J. Kim and K. Roy, "Double Gate MOSFET Subthreshold Logic for Ultra-Low Power Applications", *in the proc of IEEE SOI Conference*, pp. 97- 98, 29 Sept.-2 Oct. 2003.
- [40] K. Ramasamy and C. Crespo "Double-Gate MOSFETs." Portland State University, ECE, 2003.



**Rajni Gautam** is currently working toward the Ph.D. degree in the Department of Electronic Science, University of Delhi South Campus, New Delhi, India. She has authored/coauthored 25 technical papers in international journals and

conferences. Her current research interests are in the areas of analytical modeling, and simulation of cylindrical gate all around MOSFET, Study of localised charges reliability and analytical modelling and simulation of gate all around MOSFET for sensor applications.



**Manoj Saxena** was born in New Delhi, India, on August 14, 1977. He received the B.Sc. (with honors), M. Sc., and Ph.D. degrees from the University of Delhi, New Delhi, in 1998, 2000, and 2006, respectively, all in electronics. He joined

Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi in 2000 and presently he is Associate Professor. He has authored/coauthored 170 technical papers in international journals and conferences. His current research interests are in the areas of analytical modeling, design, and simulation of Optically controlled MESFET/MOSFET, silicon-on-nothing, insulated-shallow-extension, cylindrical gate MOSFET and Tunnel FET.



**R. S. Gupta** received the B.Sc. and M.Sc. degrees from Agra University, Agra, India, in 1963 and 1966, respectively, and the Ph.D. degree in electronic engineering from the Institute of Technology, Banaras Hindu University, Varanasi, India, in

1970. He has authored or coauthored more than 600 papers in various international and national journals and conference proceedings and supervised 46 Ph. D students. Currently he is Professor and Head in Department of ECE, Maharaja Agrasen Institute of Technology (GGIP University, Delhi). His current interests and activities include modeling and simulations of HEMTs, and advance MOSFET device designs.



**Mridula Gupta** received the B.Sc. degree in physics, the M.Sc. degree in electronics, the M.Tech. degree in microwave electronics, and the Ph.D. degree in optoelectronics from the University of Delhi, Delhi, India, in 1984, 1986, 1988, and 1998,

respectively. Since 1989, she has been with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, where she was previously a Lecturer and is currently an Professor and with the Semiconductor Devices Research Laboratory. She has authored or coauthored more than 330 publications in international and national journals and conference proceedings. Her current research interests include modeling and simulation of MOSFETs, MESFETs, and HEMTs, for microwave applications.