An 8-b 1GS/s Fractional Folding CMOS Analog-to-Digital Converter with an Arithmetic Digital Encoding Technique

Seongjoo Lee, Jangwoo Lee, Mun-Kyo Lee, Sun-Phil Nah, and Minkyu Song

Abstract—A fractional folding analog-to-digital converter (ADC) with a novel arithmetic digital encoding technique is discussed. In order to reduce the asymmetry errors of the boundary conditions for the conventional folding ADC, a structure using an odd number of folding blocks and fractional folding rate is proposed. To implement the fractional technique, a new arithmetic digital encoding technique composed of a memory and an adder is described. Further, the coding errors generated by device mismatching and other external factors are minimized, since an iterating offset self-calibration technique is adopted with a digital error correction logic. A prototype 8-bit 1GS/s ADC has been fabricated using an 1.2V 0.13 um 1-poly 6-metal CMOS process. The effective chip area is 2.1 mm^2(ADC core : 1.4 mm^2 , calibration engine : 0.7 mm^2), and the power consumption is 88 mW. The measured SNDR is 46.22 dB at the conversion rate of 1 GS/s. Both values of INL and DNL are within 1 LSB.

Index Terms—Fractional folding ADC, iterating offset self-calibration, arithmetic digital encoding

I. INTRODUCTION

With the growth of digital broadcasting market and wireless communication technology, A/D Converters satisfying high conversion rates of a few GHz are required for high-performance multimedia instruments such as HDTV, Satellite Set Top Box(S-STB), Ultra Wide Band (UWB), digital oscilloscope, and so on. In order to satisfy the high speed ADC, a few structures have been reported such as flash, pipelining, and time-interleaving [1-3]. However, the flash ADCs cause a difficulty in realizing the high resolution due to an increase in the number of preprocessing amplifiers by 2^n times with the increasing resolution. Thus it is a great constraint in realizing the ADC because of its huge power consumption and chip area. In case of pipelining architecture, it is hard to raise the operating speed due to the limitation of an operational amplifier. Further, a time interleaving ADC has huge chip area and power consumption in proportion to the channel expansion. Thus the time interleaving scheme causes a reduction of SNDR by the clock skew and long delay times.

Recently, the ADCs with a folding structure have been continuously studied to solve such problems, and many kind of folding ADCs have been published [4-12]. However, folding ADCs have an asymmetry error for boundary conditions, since there is even number of folding blocks. It reduces the performance of ADC and causes many problems [5]. Further, the folding structure has a severe linearity error due to the undesired operation of the comparators. Even though a few calibration techniques have been described to improve the linearity errors, it is not enough to satisfy the required specifications [5, 6]. Hence, in this paper, we propose a fractional folding ADC which has an 8-bit resolution, a

high conversion rate of 1 GS/s, a low power consumption, and a small chip area. Further, a new encoding algorithm for the fractional folding scheme is discussed. A new calibration technique with the iterating offset self-calibration through a feedback loop for digital errors is described.

In Section II, the circuit techniques for the proposed folding ADC are discussed. Measured results are described in Section III. Finally, the conclusions are summarized in Section IV.

II. ARCHITECTURE

Fig. 1 shows a block diagram and basic explanation for a 3-bit folding ADC. When a binary 3-bit digital code is divided into the most significant 1-bit and the other 2-bits, the other 2-bits are repeated per the most significant bit. Namely, the folding ADC is divided into coarse ADC and fine ADC. To use this process, the analog input signal is folded by a folding-amp up to the resolution of coarse ADC. That is principle of folding ADC. In the case of 8-bit folding ADC, it is designed as 2+6 or 3+5 coarse and fine blocks [7, 8]. In the case of 2+6 structure with the 6-bit fine ADC in 8-bit folding ADC, there is an advantage of obtaining broad input bandwidths. However, since the number of 6-bit ADC's comparator is 64, it has disadvantages of a large chip area and huge power consumption. Thus the 3+5 structure with a smaller chip area and a lower power has recently been a dominant scheme compared with the 2+6 structure. In the case of 3+5 structure, we normally use the cascaded folding blocks to reduce the load capacitances. Further, a resistance averaging technique is also usually adopted to minimize the offset errors for each preprocessing amplifier and folding block [9]. However, the
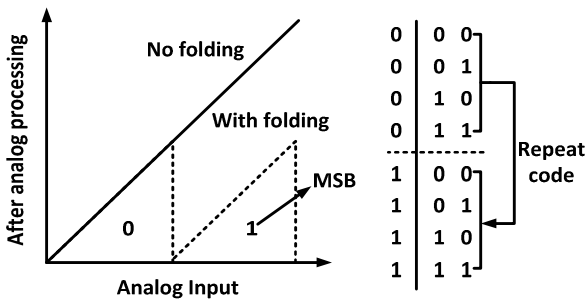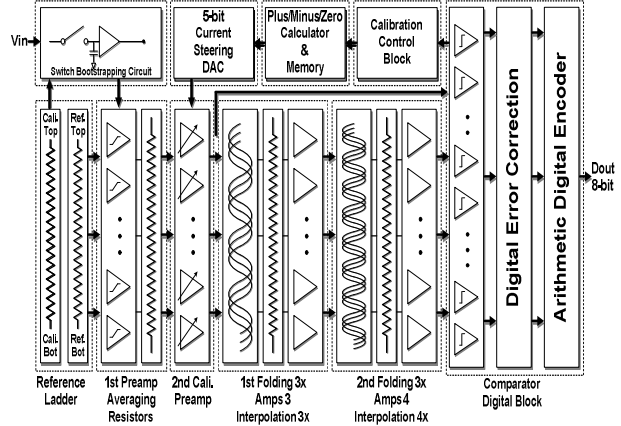

Fig. 1. Basic Explanation for a 3-bit folding ADC.

Fig. 2. Structure of the 8-bit fractional folding ADC.

conventional folding ADCs which composed of an even number of preprocessing amplifiers and folding amplifiers have asymmetric output voltages for the preprocessing amplifiers. Thus satisfactory averaging effects may not be expected [10]. In this paper, a new fractional folding structure using an odd number of preprocessing amplifiers and folding amplifiers based on the folding ADC with the conventional 3+5 structure is proposed. Further, a few kinds of techniques are described to solve various problems of the conventional folding structure.

Fig. 2 shows the overall structure of the proposed 8-bit fractional folding ADC composed of the input signal processing part to receive the signals, the amplifier to process the signal in parallel, the comparators, the self-calibrating circuit, the digital error correction circuit, the novel encoder and the clock generator.

III. CIRCUIT DESCRIPTION

### 1. Fractional Folding Technique

Fig. 3 shows the circuit diagram of a folder and conceptual output signals of folding blocks. Table 1 shows the comparison of conventional folding structures and the proposed fractional folding one. FR means Folding Rate, NFB means Number of Folding Blocks, and IR means Interpolation Rate, respectively. In the parallel processing type of ADCs, generally, the offset errors generated at the analog input processing may reduce SNDR. Therefore, the resistance averaging technique at the output of the preprocessing amplifiers is

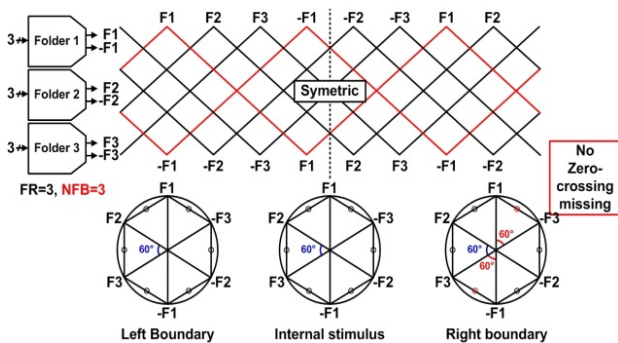**Table 1.** Comparison of conventional ones and the proposed one

Folding Structure	FR	NFB	IR	# of Preamp	# of Comp
Folding 2+6	4	16	4	80	64
	4	8	8	40	64
Folding 3+5	8	8	4	72	32
	8	4	8	36	32
Fractional Folding	7.11	9	4	27	36
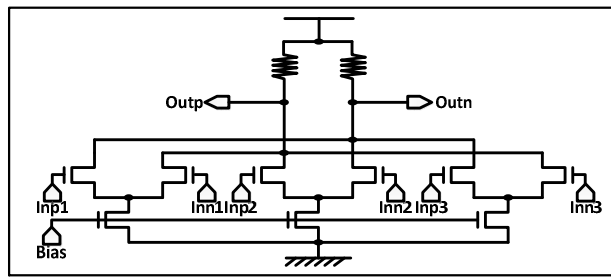
(a)
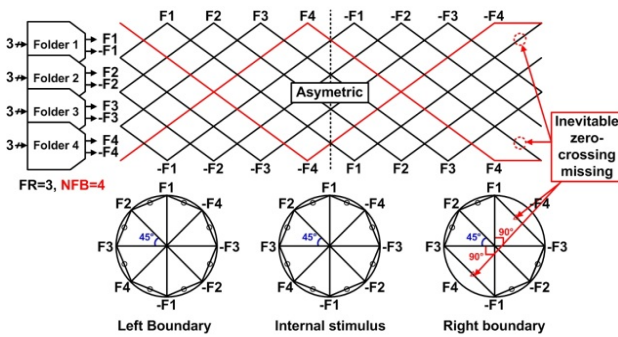
(b)

(c)

Fig. 3. Conceptual output signals of the folding blocks (a) circuit diagram of folder, (b) conventional one, (c) proposed one.

normally used to solve those problems. However, since the conventional folding ADCs are composed of even NFBs as shown Table 1 and Fig. 3(b), it is difficult to implement a symmetrical averaging technique. In order
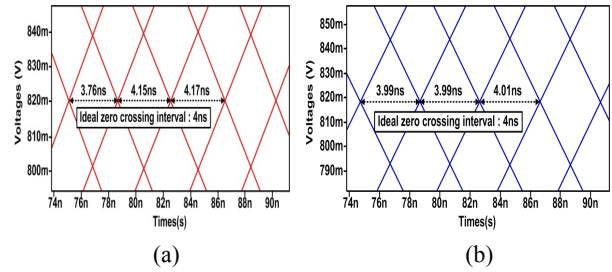

(a)   (b)

Fig. 4. SPICE simulation result for the zero-crossing errors (a) conventional one, (b) fractional one.

to solve the problem, using a dummy circuit has been published [9, 10], but it is not a fundamental solution due to the reduction of the signal linearity and an increase in the power. To adopt a symmetrical averaging technique, it is the best way to use the odd number of preprocessing amplifiers like Fig. 3(c). The nomenclature of fractional folding is that the folding rate of 7.11 has a decimal point. In the case of the conventional folding structure shown in Fig. 3(b), there exist many errors at the zero-crossing gap due to the asymmetry of boundary conditions. However, in the case of the fractional folding structure shown in Fig. 3(c), there are almost no zero-crossing errors because of odd number of folding blocks and preprocessing amplifiers. Further, since the signals of each block have symmetrical waveforms, high level IR and low power consumptions are obtained.

Fig. 4 shows the SPICE simulation results for the analog output signals of 1st folding amps in Fig. 2. In the case of the conventional even NFBs shown in Fig. 4(a), the maximum error rate is about 6% due to the asymmetric boundary conditions. In the case of the fractional folding structure of Fig. 4(b), the error is about 0.25% due to the symmetric boundary conditions. From Tab.1, further, the number of preamplifiers is drastically reduced, compared to the others.

2. An Arithmetic Digital Encoding

The final analog output signals of fractional folding ADC are not proportional to 2^n because of the odd number of folding blocks. Therefore, the most difficult problem of the fractional folding ADC can not use the conventional normal digital encoding algorithm [3]. Although an encoder based on many switches has been conventionally used to solve those problems, the circuit configurations are too complicated to have the high
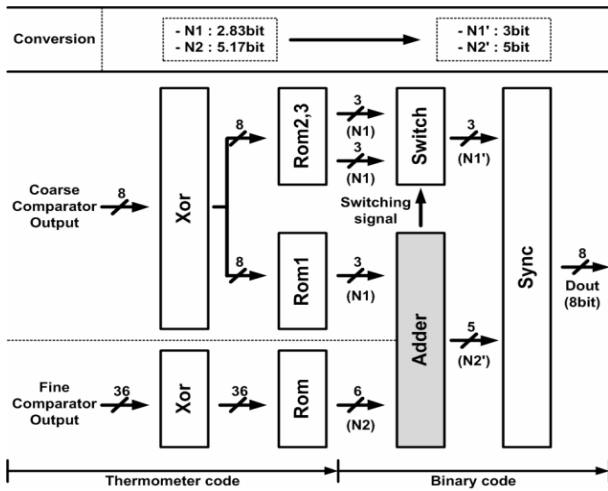
Fig. 5. Block diagram for proposed encoder.

Fig. 6. Arithmetic digital encoding procedure for the fine ADC block.

speed operation. Therefore, in this paper, a new type of digital encoder is proposed with the combination of a conventional ROM encoder and adder logic. Fig. 5 shows the block diagram for the structure of the encoder. Due to the fractional folding rate of 7.11, the fractional folding structure has a digital signal value of $\log_2(7.11)$ (N_1=2.83-bit) at the coarse ADC block, and a digital signal value of $\log_2(36)$ (N_2=5.17-bit) at the fine ADC block. In order to generate the normal coarse digital bit (N_1=3-bit) and the fine digital bit (N_2=5-bit), the fractional digital bit must be converted into normal digital bit. Fig. 6 shows the encoding procedure of the fine ADC block. The additional 0.17-bit at the fine ADC block can be eliminated by the addition of ROM1 digital output at the coarse ADC block. Namely, the 6-bit digital code of fine ADC is converted into 5-bit digital code by the addition of ROM1 digital code.

Then, the switching signal of the adder block at the fine ADC selects the ROM2 or ROM3 at the coarse ADC block shown in Fig. 5. Thus the results of coarse ADC are synchronized by the output of fine ADC, and the final 8-bit results of the fractional folding ADC are finally obtained. The proposed encoder has an advantage of independent operation between the coarse and fine block through the use of the adder circuit, while the conventional switching structure has the limitation of asynchronous delay time.

3. Digital Coding Error Correction Logic

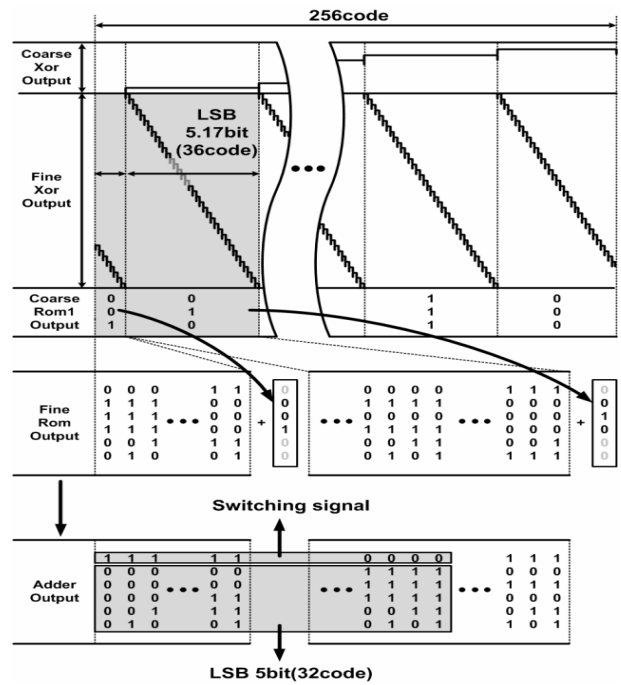Since a normal folding ADC is composed of a coarse

block and a fine block, the partitioned structure may cause serious digital errors due to the time delay between the coarse block and the fine block. Fig. 7 shows the mechanism of the coding errors. When the time delay error of Δt occurs at the output signals of the coarse and fine folding blocks as shown in Fig. 7(a), the output signals of the comparators also have the error codes as shown Fig. 7(b), an example of coding errors. Even though the desired coding is 1000 at all cases, 1001 or 1111 may be obtained. Since the errors are very fatal, we must reduce or eliminate the coding errors.

In this paper, a digital error correction technique is proposed as shown in Fig. 8. Fig. 8(a) shows the correction algorithm, and Fig. 8(b) shows the digital correction logic (DCL). First of all, DCL selects Up or Down signal in advance by the 2nd binary code of the fine ADC. It means pre-selected codes are stored. Then, the output of the XOR generated by both the 3rd binary code of the coarse ADC and the fine comparator output decides the LSB codes of the fine ADC. If the output of XOR is 1, the LSB codes are corrected into the pre-selected codes. If the output of XOR is 0, the LSB codes are not corrected. Therefore, it minimizes the coding errors due to the time delay between the coarse and fine. The additional area and power consumption of the DCL
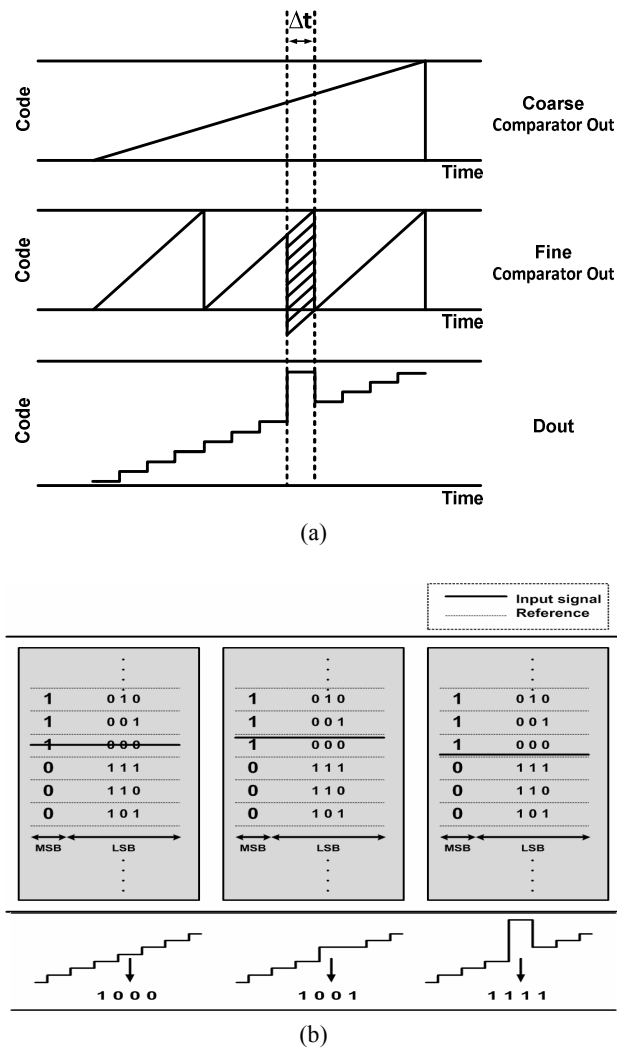
(a)

(b)

Fig. 7. Mechanism of coding errors in a folding ADC (a) Digital coding errors of comparators, (b) Example of coding error.

are very small.

4. Self-Calibration Technique

Most of the ADCs have some drawbacks of linearity error, gain errors, and a few errors due to device mismatching and other secondary effects. Hence, many ADCs recently have a self-calibration logic to reduce the errors [11-14]. Fig. 9 shows a proposed self-calibration technique. At the calibration mode, the calibration references are biased to the preamplifiers. Then, comparator output controls +1 or -1 block, and they are stored at the memory cell. According to the memory cell, the input codes of 4-bit Digital-to-Analog Converter (DAC) are decided. The role of DAC controls the current
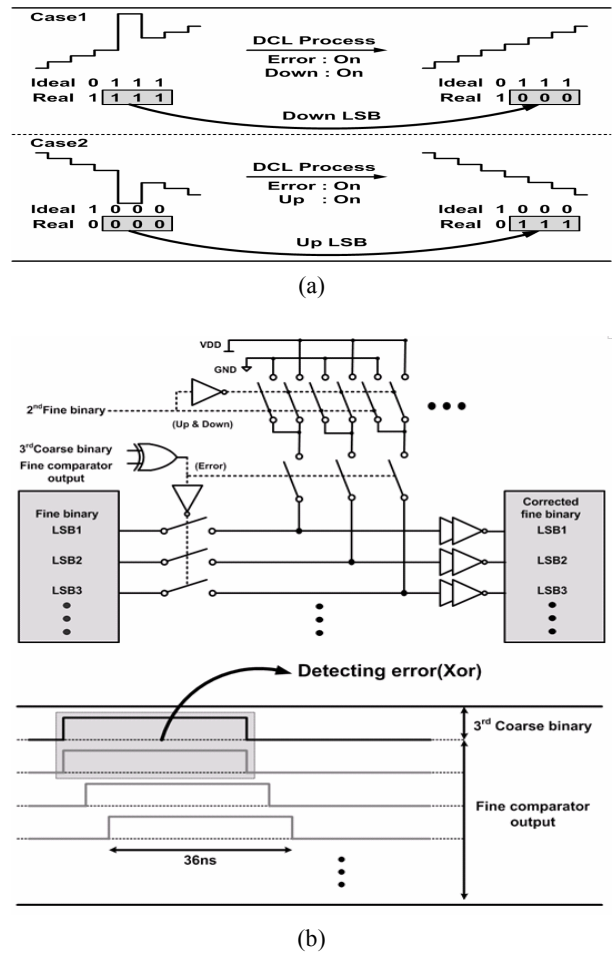

(a)

(b)

Fig. 8. Proposed digital error correction technique (a) Error correction algorithm, (b) Digital correction logic (DCL).
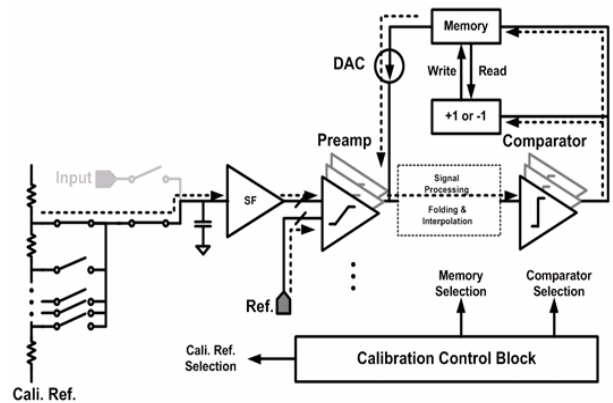

Fig. 9. Self-calibration technique.

of preamplifier. Therefore, the gain of preamplifier at the main ADC block is controlled by DAC and memory at the calibration block. While the maximum error range of ADC is about ±3LSB without the calibration logic, it is reduced to a level of ±0.5LSB with the operation of the
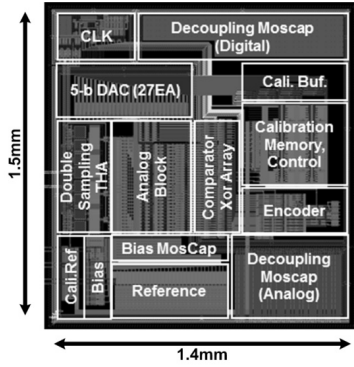
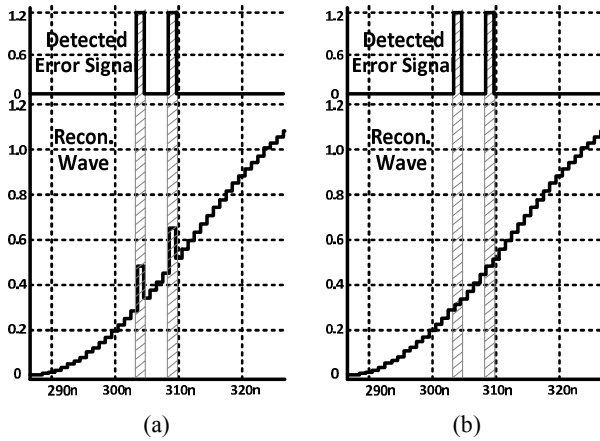**Fig. 10.** Chip photograph with calibration circuits.

Fig. 11. SPICE simulation results of the fractional folding ADC (a) without DCL, (b) with DCL.

calibration logic. Thus the performance degradation by the overall mismatch of ADC is minimized by the self-calibration logic.

IV. MEASUREMENT RESULTS

In order to verify the performance of the proposed fractional folding ADC, a prototype 8-bit 1GS/s ADC has been fabricated with Samsung 130 nm 1P6M CMOS process. Fig. 10 shows the chip photograph of the ADC. The main chip area is about 2.1 mm^2 , and the power consumption is about 88 mW at the power supply voltage of 1.2 V. A few decoupling capacitors are integrated into the chip at the spare spaces to reduce the interference among the individual blocks, EMI problems and power supply noise. Fig. 11 shows the post-layout SPICE simulation results of the reconstructed ADC waveforms at the sampling frequency of 1 GHz and the input frequency of 10 MHz to analyze the performance of the
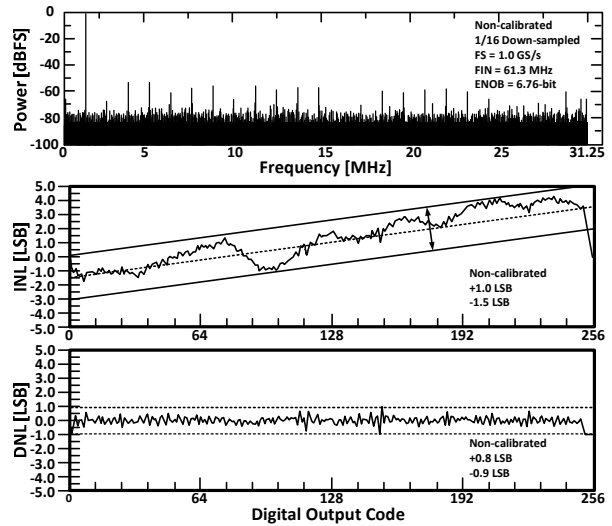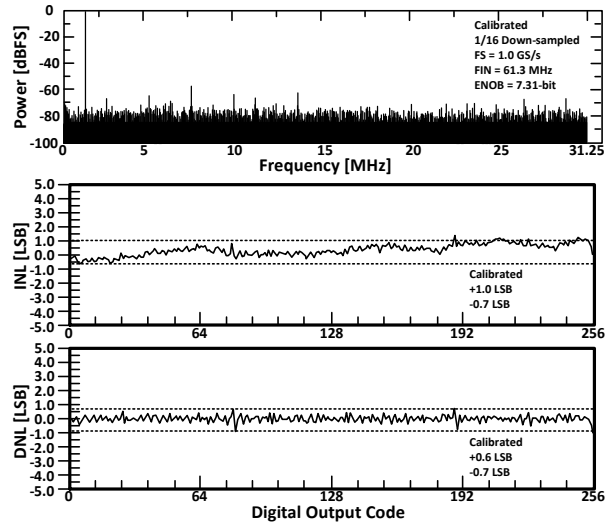
Fig. 12. Measured Results (a) Without calibration technique, (b) with calibration technique.

digital error correction logic. Without the digital correction logic, there exist many glitches and code errors as shown in Fig. 11(a). However, the code errors are drastically eliminated with the proposed error correction logic as shown in Fig. 11(b).

Fig. 12 shows the measurement results of the proposed ADC at the input frequency of 61.3 MHz and the sampling frequency (f_s) of 1 GHz. To measure the GHz sampling frequencies, decimation circuits capable of 1/16 down sampling are added into the output buffer. It is very helpful technique to verify the high-speed ADC. Fig.

12(a) shows the measurement results of non-calibrated ADC, whereas Fig. 12(b) shows the measured results of calibrated ADC. The measured result of SNDR with the calibrated technique is improved by 3.31dB, compared to that of the non-calibrated technique, INL by 0.8 LSB, and DNL by 0.4 LSB, respectively.

Fig. 13 shows the measured results of ENOB versus input frequencies at the sampling frequency (f_s) of 1 GHz. The measured ENOB of the calibrated ADC is about 7.41-bit at the lower frequency of 10 MHz, while that is about 6.80-bit at the nyquist input frequency. Table 2 shows the summary of the measurement results. With the calibration technique, the measurement results are drastically improved. Table 3 shows the performance comparison with the conventional ones. With the fractional folding technique, the performances are improved such as SNDR, INL, DNL, power consumption, and so on. FOM is about 0.52 pJ, even though 130 nm CMOS technology is used.
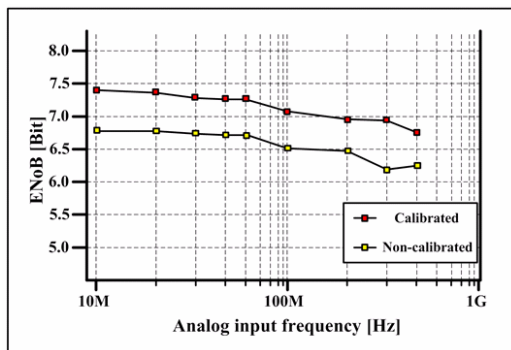

Fig. 13. Measured ENOB at f_s=1GHz.

Table 2. Summary of the measurement results

Architecture		Fractional Folding ADC	
Resolution		8-b	
Conversion Rate		1GS/s	
Power Supply		1.2V(Analog&Digital)	
Power Consumption		88mW (ADC & Calibration)	
Chip Area		2.1 mm^2 (ADC & Calibration)	
Technology		0.13μm 1P6M CMOS	
Self-calibration		ON	OFF
SNDR	fin=10MHz	46.22 dB	42.94 dB
	fin=400MHz	42.68 dB	39.71 dB
INL(LSB)		+1.0 / -0.7	+1.0 / -1.5
DNL(LSB)		+0.6 / -0.7	+0.8 / -0.9

Table 3. Performance comparison with conventional ones

	This work	[12]	[13]	[14]
Technology	130nm	180nm	65nm	90nm
Resolution	8bit	10bit	8bit	8bit
Conversion Rate	1GHz	1GHz	1GHz	1.25GHz
Power Supply	1.2V	1.8V	1.2V	1.0V
SNDR	46.22dB	56.9dB	48.1dB	46.4dB
ENOB	7.41bit	9.1bit	7.7bit	7.0bit
INL [LSB]	1	0.72	unnoted	1.3
DNL [LSB]	0.7	0.2	unnoted	1.1
Power Dissipation	88mW	2.52W	75mW	207mW
Chip Area	2.1mm^2	49mm^2	0.24mm^2	2.38mm^2
FOM [/Conv]	0.52pJ	4.592pJ	0.361pJ	1.294pJ

V. CONCLUSIONS

In this paper, a fractional folding ADC was discussed to satisfy a low power consumption, a small chip area and a high speed conversion rates. To implement the characteristics, a fractional folding technique, an arithmetic digital encoding, a new digital error correction logic and self-calibration circuits were described. To verify the proposed ideas, a prototype 8-bit 1GS/s folding ADC was fabricated. The measurement results of the ADC were remarkable, compared to those of the conventional ones. The measured FOM was about 0.52 pJ, even though 130 nm CMOS technology was used. Therefore, the proposed techniques are very useful to design a high performance folding ADC.

ACKNOWLEDGMENTS

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