A Reset-Free Anti-Harmonic Programmable MDLL-Based Frequency Multiplier

Geontae Park, Hyungtak Kim, and Jongsun Kim

Abstract—**A reset-free anti-harmonic programmable multiplying delay-locked loop (MDLL) that provides flexible integer clock multiplication for high performance clocking applications is presented. The proposed MDLL removes harmonic locking problems by utilizing a simple harmonic lock detector and control logic, which allows this MDLL to change the input clock frequency and multiplication factor during operation without the use of start-up circuitry and external reset. A programmable voltage controlled delay line (VCDL) is utilized to achieve a wide operating frequency range from 80 MHz to 1.2 GHz with a multiplication factor of 4, 5, 8, 10, 16 and 20. This MDLL achieves a measured peak-to-peak jitter of 20 ps at 1.2 GHz.**

Index Terms—**frequency multiplier, multiplying DLL, DLL, MDLL**

I. INTRODUCTION

CMOS frequency multipliers have been widely used in integrated wireless transceiver systems and inter-chip I/O interface applications to multiply the incoming reference clock frequency [1, 2]. Most frequency multipliers are based on a phase-locked loop (PLL). Since a PLL is a higher-order system, it has an inherent stability problem and is difficult to design. Also, accumulated jitter of the VCO makes PLLs more susceptible to supply and substrate noise and process, voltage, and temperature (PVT) variations [1]. On the contrary, a typical delay-

locked loop (DLL) is a single-pole system with no jitter accumulation problem.

Recently, multiplying delay-locked loop (MDLL) [3, 4] based frequency multipliers have been introduced to replace PLL-based ones due to their advantages such as ease of design, smaller area, lower power dissipation, no-stability issue, and better jitter performance. However, conventional MDLLs [3, 4] suffer from a harmonic locking problem. Harmonic locking occurs when the DLL and MDLL locks to harmonic reference edges of the input clock as shown in Fig. 1, resulting in incorrect output clock frequencies. Also, these conventional MDLLs are not able to switch the frequency from low to high. Moreover, changing of the input clock frequency and multiplication ratio during operation is not available.

Although [5] was introduced to avoid harmonic locking, it requires a complicated error detector circuit with large on-chip capacitors and area overhead.

In this paper, a new simple reset-free anti-harmonic programmable MDLL-based frequency multiplier is presented. The proposed frequency multiplier has the capability of changing the input clock frequency and multiplication factor during operation, while maintaining locking process without any external reset. To resolve harmonic locking problems and allow changing of the
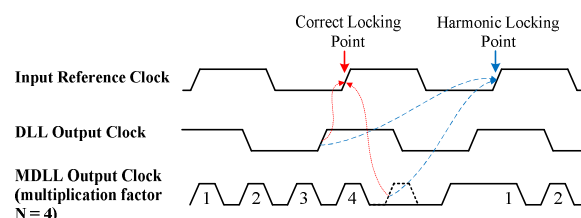
Fig. 1. Timing diagram of harmonic locking problem in DLLs and MDLLs.

input clock frequency and multiplication factor without increasing complexity and hardware overhead, a new harmonic lock detector and simple control logic are proposed. To achieve a wide operating frequency range, the number of delay elements of the VCDL is programmable.

II. PROPOSED ARCHITECTURE AND CIRCUIT DESIGN

The proposed MDLL-based frequency multiplier is shown in Fig. 2. It comprises an input multiplexer (MUX$_1$), a voltage controlled delay line (VCDL), a phase detector (PD), a charge pump (CP), a regulator, a bias circuit, a harmonic lock detector, a control logic block, and a divide-by-N divider. The VCDL consists of a total of 24 single-ended delay elements (DEs) and a 4-to-1 output multiplexer (MUX$_2$) for wide operating frequency range operation. The DE utilizes a typical shunt-capacitor inverter (SCI). The proposed MDLL provides programmable clock multiplication with a multiplication factor N=4, 5, 8, 10, 16, and 20. By adjusting the delay of the VCO-like VCDL, the output clock frequency f_{Oclk} can be varied.

Fig. 3 shows the locking process and the proposed simple harmonic lock detector (HLD) with the control logic block. Referring to Figs. 1 and 2, when the Control signal is asserted, the external input clock Iclk enters the VCDL through the MUX$_1$ and then propagates through the VCDL. At every N cycles of Oclk, the divider generates the low pulse signal Div. The Div signal is used for the control Logic block that generates the Control signal. Every N pulses of the output Oclk, the phase of Iclk and Oclk are compared by the PD when the Control signal is asserted. In response to the PD's output
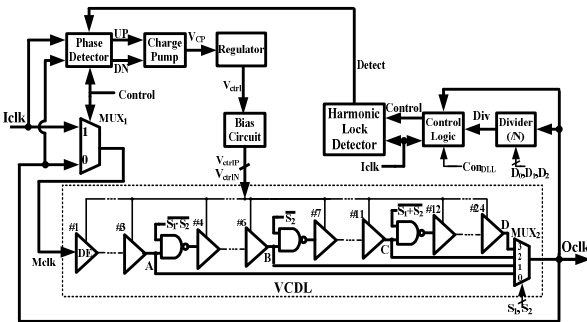

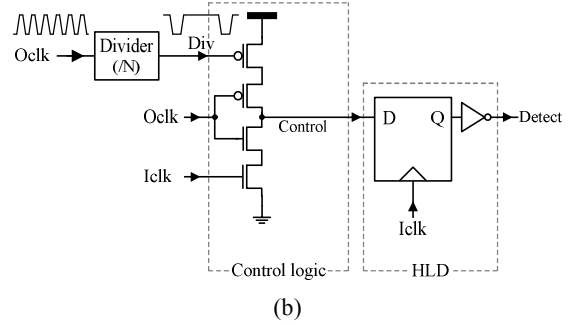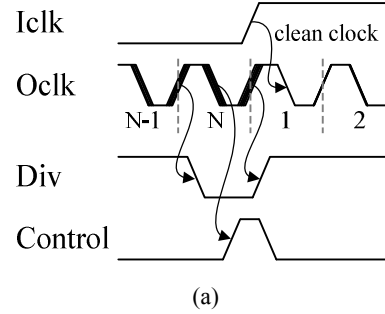Fig. 2. Proposed MDLL-based Frequency Multiplier.

Fig. 3. (a) Locking process (b) Proposed simple harmonic lock detector (HLD) and control logic block.

Table 1. Programmable MDLL frequency range

S$_1$	S$_2$	Number of DEs	Frequency Range
1	1	#1~#3	1.2 – 0.45 GHz
0	1	#1~#6	0.8 – 0.28 GHz
1	0	#1~#11	0.5 – 0.16 GHz
0	0	#1~#24	− 0.08 GHz

(UP, DN), the CP generates a control voltage V$_{cp}$. The delay of the DE is then adjusted to make f_{Oclk}=N×f_{Iclk} depending on the bias voltage, V$_{ctrlN}$ and V$_{ctrlP}$, which generated by the regulator and the bias circuit.

As shown in Fig. 3(a), when the MDLL is locked, Iclk's rising edge is aligned with the Nth rising edge of Oclk, resulting in zero phase difference between the input and output clocks. This architecture achieves better jitter performance than a PLL by periodically replacing the rotating edge with a clean edge of the input Iclk. In order to achieve a wide operating frequency range with monotonic delay increase, the number of cascaded DEs of the VCDL can be selected as four steps to produce a desired output clock delay by using the three NAND gates and the MUX$_2$ with control inputs S$_1$ and S$_2$ as shown in Table 1.

III. Harmonic Lock Detector and Anti-Harmonic Process

Unlike the conventional MDLL [3] that has a harmonic locking problem, the proposed MDLL utilizes a simple harmonic lock detector to avoid harmonic locking. As shown in Fig. 3(a), the HLD is a simple D flip-flop. The Control signal is asserted when both Div and Oclk goes low and is disabled when both Div and Oclk goes high. The PD is activated while the Control signal is high.

By comparing the relationship between the Control signal and Iclk, harmonic locking can be easily detected and corrected as shown in Fig. 4. If the Oclk frequency, f_{Oclk}, is lower than the desired frequency, $N \times f_{Iclk}$, with an example N=8, the Control signal is low at the 2'nd rising edge of Iclk. This condition is considered as a start of possible harmonic lock. Then the HLD generates the Detect signal by sampling the Control signal at the rising edge of Iclk. The Detect signal is disabled at the next rising edge of Iclk. This Detect pulse is used to avoid harmonic locking by simply switching the PD outputs when the HLD is turned on. This causes additional
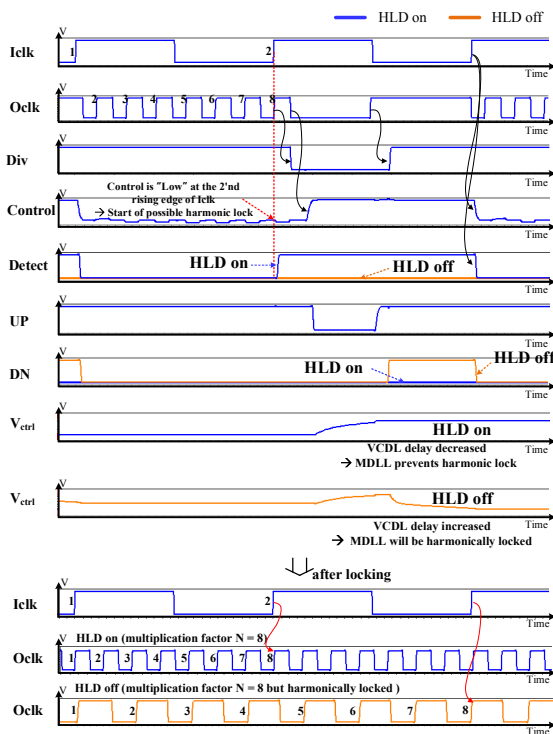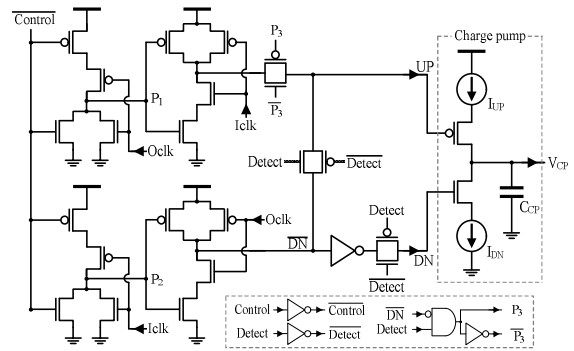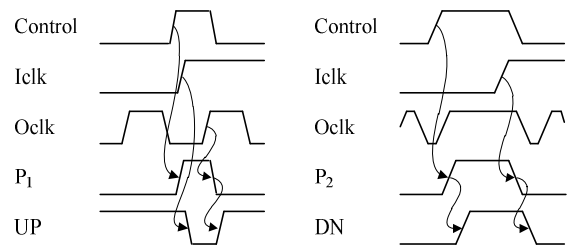

Fig. 4. Simulated timing diagram of harmonic lock detecting and correcting process

(a)

(b)

Fig. 5. (a) Proposed PD and charge pump (b) Detailed timing diagram of the PD operation to avoid harmonic locking

active-low UP pulses that increase I_{up} current and V_{ctrl} voltage, resulting in correctly locked output frequency f_{Oclk} with a multiplication factor of 8. On the other hand, the DN pulse signal is generated when the HLD is turned off, resulting in harmonically locked 1/2 frequency of f_{Oclk}.

Fig. 5 shows the proposed PD and the charge pump. As shown in Fig. 5(a), this PD compares the phase of Iclk and Oclk while the Control signal is high, and then enables the active-low UP signal when the Iclk is high and the Oclk is low. The DN signal is enabled when the Iclk is low and the Oclk is high.

IV. Experimental Results

The proposed MDLL is fabricated in a 0.18-μm CMOS process and tested in a chip-on-board (COB) assembly. Fig. 6 shows the simulated MDLL operation that shows the capability of changing the multiplication factor (=division ratio) N and the input clock frequency during operation without external reset. Fig. 7 presents the measured timing diagram of the Iclk and Oclk signals at f_{Oclk}=100 MHz ~ 1 GHz with multiplication factors of
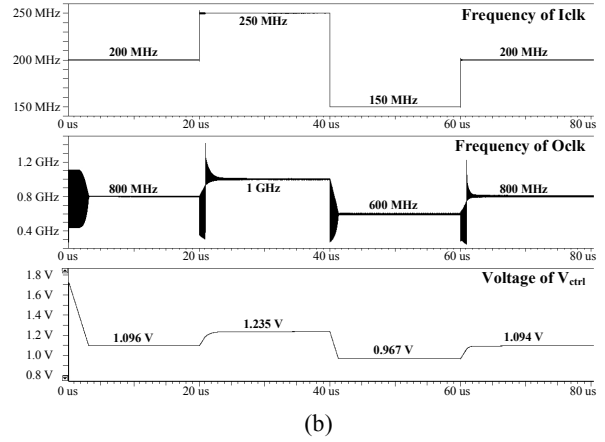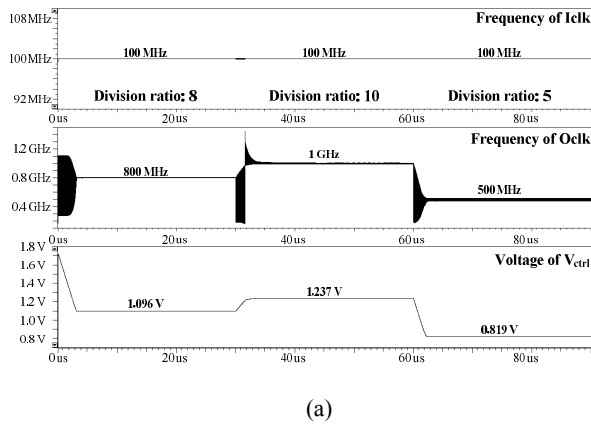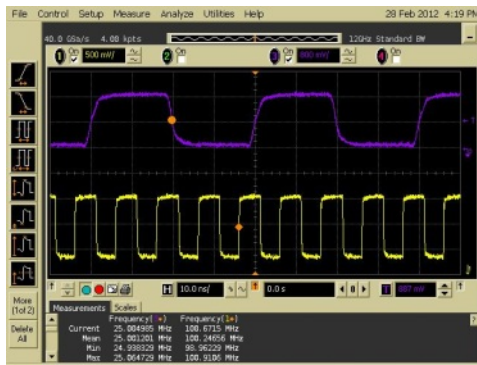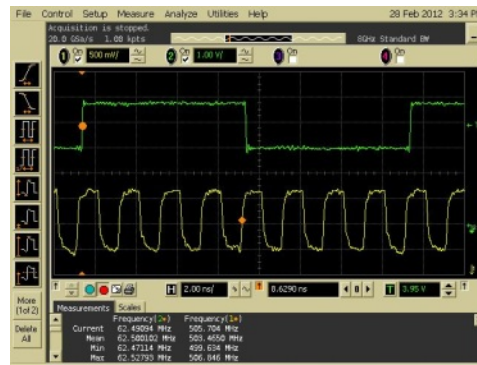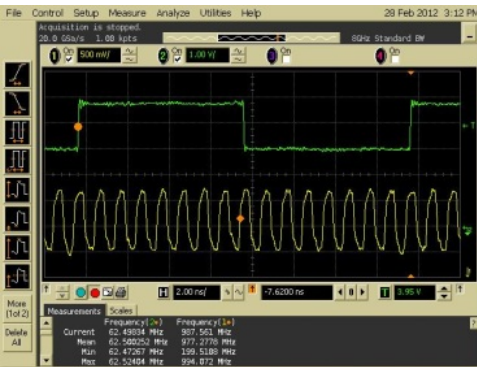
(a)

(b)

Fig. 6. Simulated MDLL operation (a) when the division ratio N is changed to 8, 10, and 5 (b) when the input clock frequency is changed.
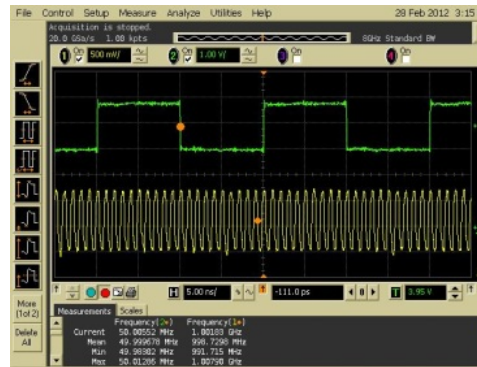

Oclk at 100 MHz (N=4)

Oclk at 500 MHz (N=8)

Oclk at 1 GHz (N=16)

Oclk at 1 GHz (N=20)

Fig. 7. Measured Iclk and Oclk signals with multiplication factors of 4, 8, 16, and 20.

N=4, 8, 16, and 20, respectively.

As shown in Fig. 8(a), proposed MDLL achieves a measured peak-to-peak jitter of 20.0 ps at 1.2 GHz. The output frequency range is from 80 MHz to 1.2 GHz. The output frequency range figure-of-merit (FOM = $f_{\text{Oclk\_max}}/f_{\text{Oclk\_min}}$) is 15, where $f_{\text{Oclk\_max}}$ is the maximum output frequency and $f_{\text{Oclk\_min}}$ is the minimum output frequency.

Fig. 8(b) shows the die microphotograph and layout of the proposed MDLL. It occupies an active area of only 0.045 mm^2 and the power dissipation is 12.8 mW at 1.2 GHz for a supply voltage of 1.8 V. A performance comparison between the proposed MDLL and other MDLLs is given in Table 2.
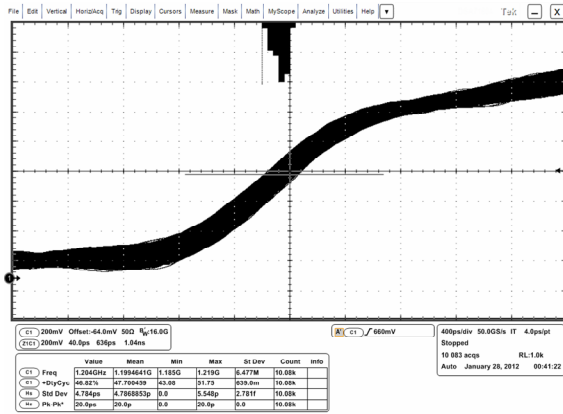
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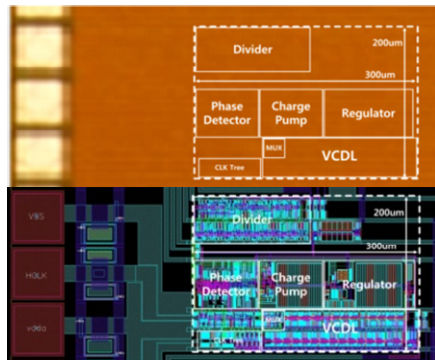
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Fig. 8. (a) Measured peak-to-peak jitter at 1.2 GHz (b) Chip microphotograph and layout.

Table 2. Performance summary and comparison

	[3]	[5]	[6]	This work
Technology	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Supply voltage (V)	1.8	1.8	3.3	1.8
Architecture	Mixed	Mixed	All digital	Mixed
Operating frequency ragne(GHz)	0.2-2	0.9-2.9	0.06-0.45	0.08-1.2
Active area	0.05 mm^2	0.07 mm^2	0.216 mm^2	0.045 mm^2
Freq. multiplication	4, 6, 8, 10	13 - 20	2 - 15	4, 5, 8, 10, 16, 20
Power dissipation	12 mW @ 2 GHz	19.8 mW @ 2 GHz	<17mW	12.8 mW@ 1.2 GHz
Jitter (pk-pk)	13.11ps @ 2 GHz	12.9 ps @2.16 GHz	37.8 ps @ 0.415 GHz	20.0 ps @1.2 GHz
Anti-harmonic lock capability	X	O	O	O
Changing of input clock freq. & division factor during operation	X	O	X	O
FOM(= f$_{max}$/f$_{min}$)	10	3.2	7.5	15

IV. CONCLUSIONS

We have developed a reset-free anti-harmonic programmable MDLL that provides flexible integer clock multiplication. By utilizing a simple harmonic lock detector and a phase detector, the proposed MDLL removes harmonic locking problems and allows reset-free changing of the input clock frequency and multiplication factor during operation without initialization. The multiplication factor is easily programmable. The proposed MDLL, implemented in a 0.18-μm 1.8-V CMOS process, occupies an active area of only 0.045 mm^2. The programmable output frequency range is from 80 MHz to 1.2 GHz with a measured peak-to-peak jitter of 20.0 ps at 1.2 GHz. Compared with prior works, this MDLL achieves the best output frequency range figure-of-merit (FOM) of 15 with smaller chip area.

ACKNOWLEDGMENTS

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Geontae Park was born in Seoul, Korea, on 1988. He received the B.S. degree in the Department of Electronic and Electrical Engineering from Hongik University, Korea, in 2011 and M.S. degree in Electronic Engineering from Hongik University, Korea, in 2013, respectively. He is currently pursuing the Ph.D. degree in the Department of Electronic and Electrical Engineering from Hongik University, Korea. His interests include low power and high-speed interface circuits.

Hyungtak Kim Hyungtak Kim received the B.S. degree from Seoul National University, Korea, in 1996 and the M.S. and Ph.D. degree from Cornell University, NY, USA in 2003, all in electrical engineering. Prior to joining Hongik University, he was a senior engineer in semiconductor R&D center, Samsung Electronics, Co. Ltd., where he developed CMOS devices and process integration for 60nm DRAM technology. He is currently an assistant professor in the school of electrical engineering at Hongik University, Korea. His research interests include the devices and circuits of wide bandgap semiconductors and novel TFTs.

Jongsun Kim received the Ph.D. degree from the Electrical Engineering Department, University of California, Los Angeles (UCLA) in 2006 in the field of Integrated Circuits and Systems. He was a Postdoctoral Fellow at UCLA from 2006 to 2007. From 1994 to 2001 and from 2007 to 2008, he was with Samsung Electronics as a senior research engineer in the DRAM Design Team, where he worked on the design and development of Synchronous DRAMs, SGDRAMs, Rambus DRAMs, DDR3 and DDR4 DRAMs. Dr. Kim joined the School of Electronic & Electrical Engineering, Hongik University in March 2008. Prof. Kim's research interests are in the area of high-performance mixed-signal circuits and systems design. Current research area includes high-speed and low-power transceiver circuits for chip-to-chip communications, clock recovery circuits (PLLs/DLLs/CDRs), frequency synthesizers, signal integrity and power integrity, ultra low-power memories, power-management ICs (PMICs), RF-interconnect circuits, and low-power memory interface circuits and systems.