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Design Optimization of Silicon-based Junctionless Fin-type Field-Effect Transistors for Low Standby Power Technology

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Abstract – Recently, the junctionless (JL) transistors realized by a single-type doping process have attracted attention instead of the conventional metal-oxide-semiconductor field-effect transistors (MOSFET). The JL transistor can overcome MOSFET's problems such as the thermal budget and short-channel effect. Thus, the JL transistor is considered as great alternative device for a next generation low standby power silicon system. In this paper, the JL FinFET was simulated with a three dimensional (3D) technology computer-aided design (TCAD) simulator and optimized for DC characteristics according to device dimension and doping concentration. The design variables were the fin width (W_{fin}), fin height (H_{fin}), and doping concentration (D_{ch}). After the optimization of DC characteristics, RF characteristics of JL FinFET were also extracted.

Keywords: Junctionless, FinFET, Radio frequency, TCAD

1. Introduction

These days, semiconductor devices based on a silicon substrate are being developed for better electrical characteristics and cost-efficiency. However, conventional silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET) technologies are faced with their scaling limit as transistor size continues to decrease [1-4]. Thus, instead of traditional n/p/n or p/n/p MOSFET, many studies for the junctionless (JL) MOSFET have been reported**.** The JL MOSFET was originally proposed and demonstrated by Colinge *et al* [5-6]. This transistor, which has no pn junctions, operates in accumulation mode (AM) and a degenerate p-type polysilicon gate is used for adjusting threshold voltage to be positive so that its operations are same as the conventional n-type MOSFET. But unlike the conventional short-channel MOSFET need to make highly precise junctions, the JL MOSFETs do not need to form junctions. Thus, the JL MOSFET can overcome many fabrication issues in view of doping techniques and thermal budget without short-channel effects (SCEs) [7-11].

In this paper, design optimization of the JL MOSFET which have a fin-type structure (JL FinFET) is performed in view of threshold voltage (V_{th}), higher gate controllability, enhanced current drivability, and better subthreshold swing (*SS*). The device was designed with a Silvaco three-dimensional (3D) technology computer-aided design (TCAD) simulation program [12] and the optimization reference of this work is the low standby power technology (LSPT) performances of international technology roadmap for semiconductors (ITRS) roadmap [13]. Also, to obtain accurate results for simulations, electron concentration model, electron-field model, gate current assignment model, and 3D-structure mobility model is considered [12]. Finally, the important parameters such as transconductance (g_m), cut-off frequency (f_T), and maximum oscillation frequency (f_{max}) are extracted after an optimization process for DC performances.

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2. Simulation Results

Fig. 1 shows the structure of JL FinFET with 20 nm channel length (L_{ch}) simulated by the 3D TCAD program. To avoid polysilicon gate depletion, a degenerately doped polysilicon gate was adopted. The gate dielectric material is hafnium oxide (HfO_2) with 2 nm thickness (t_{ox}).

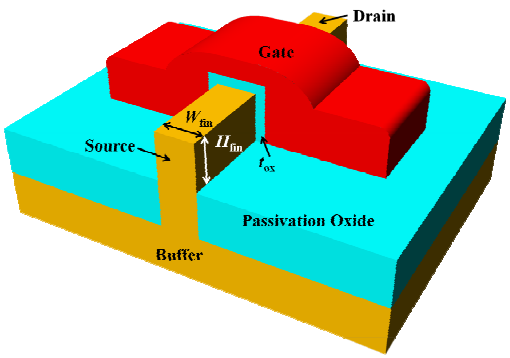


Fig. 1. The structure of JL FinFET with 20 nm channel length (L_{ch}) simulated by the 3D TCAD program.

The on-state current (I_{on}) was defined as a drain current (I_{DS}) at $V_{GS} = V_{DS} = 1$ V and the off-state current (I_{off}) was defined as an point of V_{GS} where I_{DS} begins to burst. The V_{th} was defined as V_{GS} at $I_{DS} = 10^{-7}$ A/μm.

The current of JL MOSFET is dominated by body current instead of surface current between gate oxide and inversion channel layer. Therefore, the channel doping concentration (D_{ch}), fin height (H_{fin}), and fin width (W_{fin}) which are important variables for device optimization process are designated as the simulation variables. Fig. 2 shows the I_{DS}-V_{GS} transfer curves for JL FinFET with various channel doping concentration. D_{ch} was changed n-type 1×10^{18} cm^{-3} to 4×10^{19} cm^{-3}. Both H_{fin} and W_{fin} are fixed at 10 nm. When the D_{ch} increases, V_{th} goes decrease and I_{on} as well as I_{off} is increases. The V_{th} is changed by depletion layer of channel region. The relationship between D_{ch} and depletion layer for MOS structure is presented by (1) [14].

$$W_d = \sqrt{\frac{2\varepsilon_s \Phi_{bi}}{qD_{ch}}} \tag{1}$$

where ε_s is the semiconductor permittivity, Φ_{bi} is the built in potential and q is the electric potential.

The width of depletion region (W_d) is reduced by increase of D_{ch}. JL devices are dominated not by surface current but by body current. Therefore, the high N_{ch} makes it difficult to fully deplete under the gate and V_{th} is decreased. The characteristics of V_{th} according to D_{ch} are summarized in Fig. 3.

Fig. 3 shows V_{th} as a function of D_{ch}. It is confirmed that V_{th} appears to be a negative linear function of D_{ch}. The horizontal slashed area is the section of V_{th} due to the LSPT operation reference suggested by the ITRS Roadmap, and its vicinity with ±0.1 V. The vertical slashed area represents the range of D_{ch} satisfying V_{th} reference range. The corresponding D_{ch} range to the V_{th} is 2.3×10^{19} cm^{-3} to 3×10^{19} cm^{-3}.

Fig. 4 demonstrates the detailed graph for on- and off-state current for the range of the optimized D_{ch} range of Fig. 3. The current level of JL FinFET has lower limit of I_{on} (500 μA/μm) and upper limit of I_{off} (10 pA/μm) for dependable LSPT operations. The I_{on} and I_{off} increased by changes of bulk driving current and leakage current that was caused by decrease of W_d, respectively. It turns out that the permissible D_{ch} satisfied with V_{th}, I_{on}, and I_{off} level is vicinity of 2.7×10^{19} cm^{-3}.

Fig. 5 depicts the subthreshold swing (*SS*) as a function

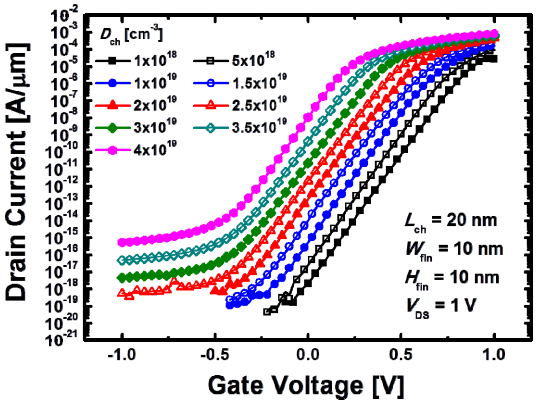


Fig. 2. I_{DS}-V_{GS} transfer curves for JL FinFET with various channel doping concentration.

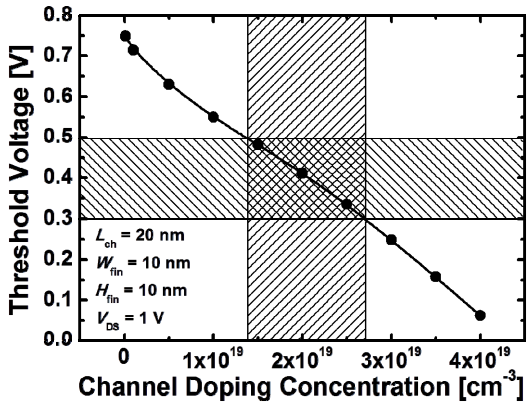


Fig. 3. V_{th} curves as a function of D_{ch}.

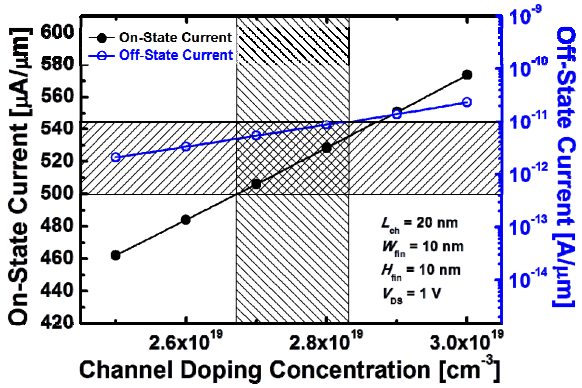


Fig. 4. On-state current and off-state current at the optimized D_{ch} range.

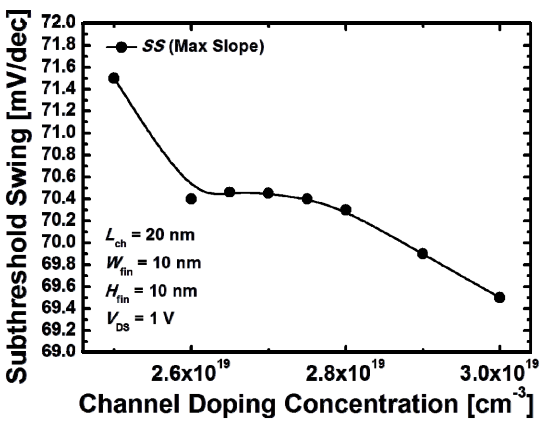


Fig. 5. Subthreshold swing (*SS*) as a function of D_{ch}.

of D_{ch}. 69 mV/dec to 71 mV/dec *SS* characteristics are observed over D_{ch} region and the vicinity of 2.7×10^{19} cm^{-3} where the point of *SS* reflection should be desirable at channel doping concentration. The values of *SS* has the minimum variation near D_{ch} = 2.7×10^{19} cm^{-3}. Fig. 6 demonstrates the I_{DS}-V_{GS} transfer curves for JL FinFET according to various W_{fin}. As W_{fin} increases, the channel region where electrons flow is distends and I_{on} increases. However, the large W_{fin} makes hard to fully deplete channel region at an off-state. Accordingly, the I_{off} increases dramatically. The difference of electron concentration under the off-state with W_{fin} of 5 nm and W_{fin} of 20 nm is depicts at Fig. 7. The maximum electron concentration of channel region was obtained 1.61 cm^{-3} and 12.9 cm^{-3}, respectively, at W_{fin} of 5 nm and W_{fin} of 20 nm. It indicates that the increase of W_{fin} makes difficult to control the I_{off}.

Fig. 8 shows the changes of *SS* and V_{th} with different W_{fin}. When W_{fin} increases, transistor needs less gate voltages to achieve turn-on condition and consequentially, V_{th} decreases. On the other hand, *SS* shows increasing results because a variation of I_{off} is much higher than variation of I_{on}. By the LSPT operation range of V_{th}, the W_{fin} of 6 nm to 10 nm is suggested as an optimized parameter.

Fig. 9 is the I_{DS}-V_{GS} transfer curves for JL FinFET

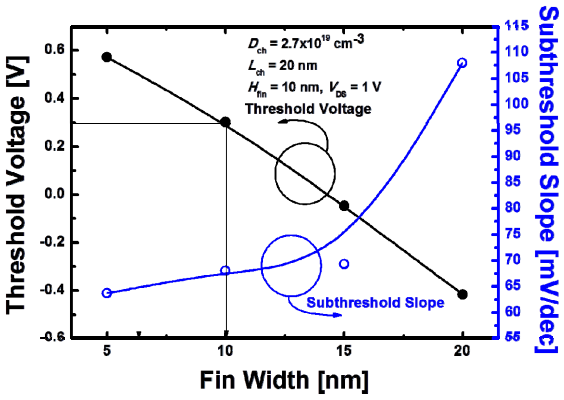


Fig. 8. *SS* and V_{th} curves with different W_{fin}.

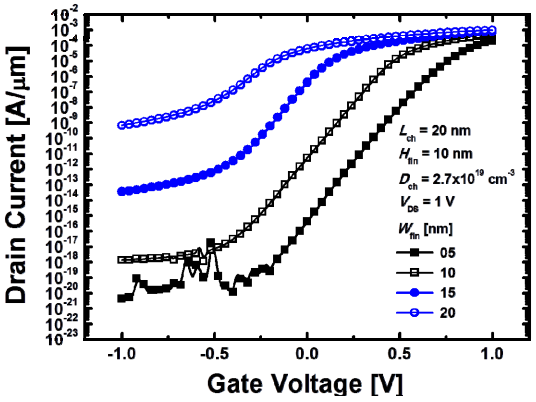


Fig. 6. I_{DS}-V_{GS} transfer curves for JL FinFET according to various W_{fin}.

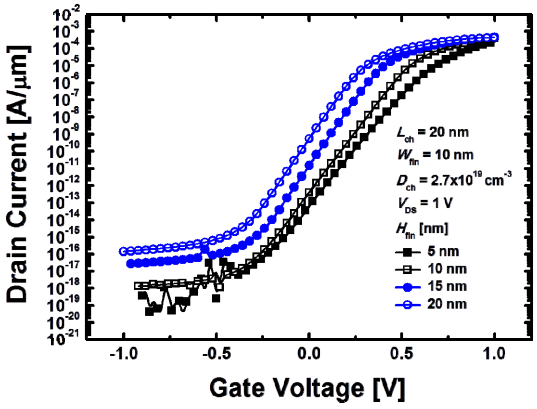
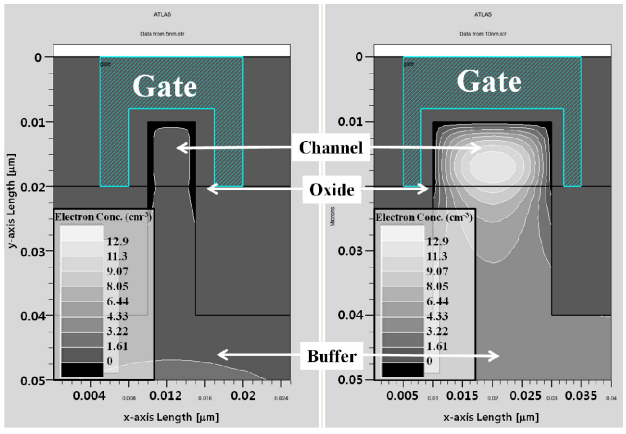
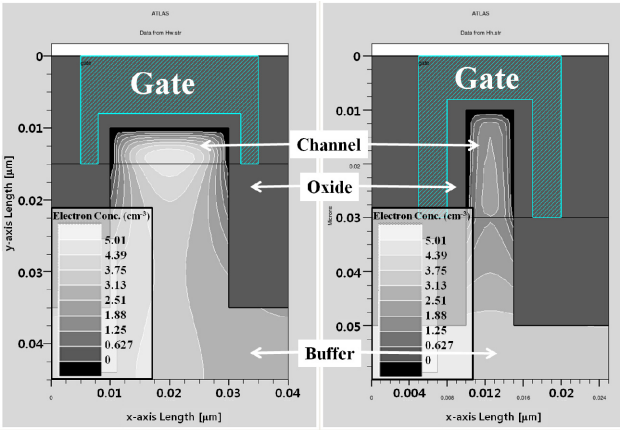


Fig. 9. I_{DS}-V_{GS} transfer curves for JL FinFET according to various H_{fin}.



(a) (b)

Fig. 7. Electron concentration under the off-state for JL FinFETs with (a) W_{fin} of 5 nm and (b) W_{fin} of 20 nm. (D_{ch} = 2.7×10^{19} cm^{-3}, V_{DS} = -1 V)



(a) (b)

Fig. 10. Electron concentration at (a) high W_{fin}=20 nm and (b) high H_{fin}=20 nm under the off-state. (D_{ch} = 2.7×10^{19} cm^{-3}, V_{DS} = -1 V)

according to various H_{fin}. The increase of H_{fin} also increases the channel region that current flows. However, the changes of H_{fin} are less vulnerable to I_{off} than that of W_{fin}. Although the increase of H_{fin} increases I_{off}, the Fin-side depletion area is fastened by fixed W_{fin}. It can be observed at Fig. 10 which shows electron concentration of high W_{fin} and high H_{fin} under the off-state. In this figure, it is confirmed that low H_{fin} of JL FinFET is easier to deplete all channel area and I_{off} should be much lower. Fig. 11 depicts the changes of *SS* and V_{th} with different H_{fin}. The V_{th} and *SS* are in inverse proportion to the H_{fin}. And by the LSPT operation range of V_{th}, the H_{fin} of under 10 nm are an optimized regions. In this region, the H_{fin} of 10 nm where has an minimum value of *SS* is the optimized result of H_{fin}.

Fig. 12 show the main conductance characteristics of optimized JL FinFET with D_{ch} of 2.7×10^{19} cm^{-3}, W_{fin} of 10 nm, and H_{fin} of 10 nm. The transconductance (g_m) and source-drain conductance (g_{ds}) determine the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) by following equations (2) and (3) [15].

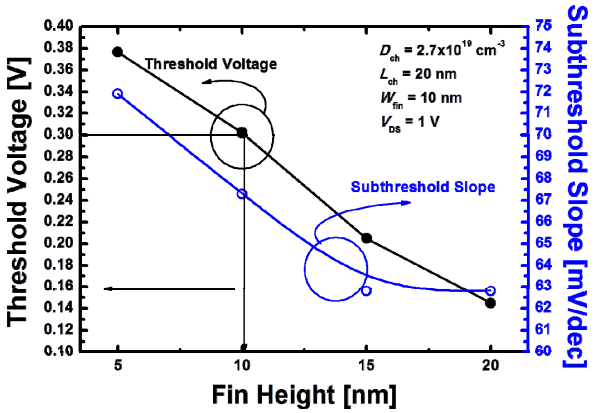


Fig. 11. *SS* and V_{th} curves with different H_{fin}.

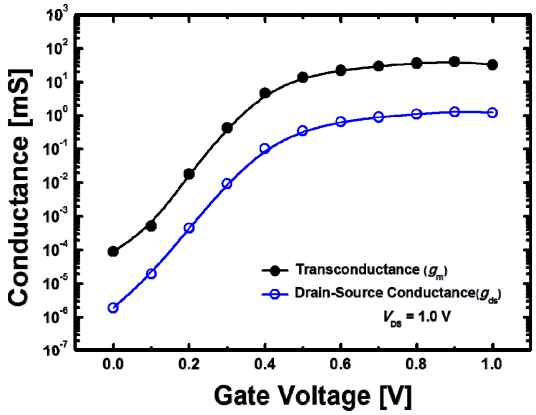
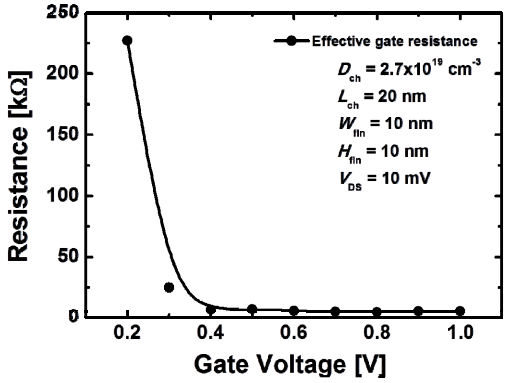


Fig. 12. The transconductance (g_m) and source-drain conductance (g_{ds}) characteristics of an optimized JL FinFET with D_{ch} of 2.7×10^{19} cm^{-3}, W_{fin} of 10 nm, and H_{fin} of 10 nm.

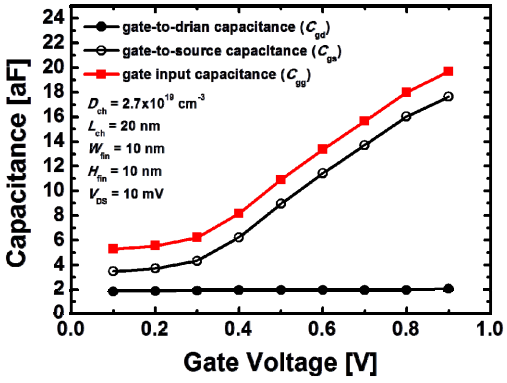
$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{2}$$

$$f_{max} \approx \frac{f_T}{\sqrt{4R_{g,eff}(g_{ds} + 2\pi f_T C_{gd})}} \tag{3}$$

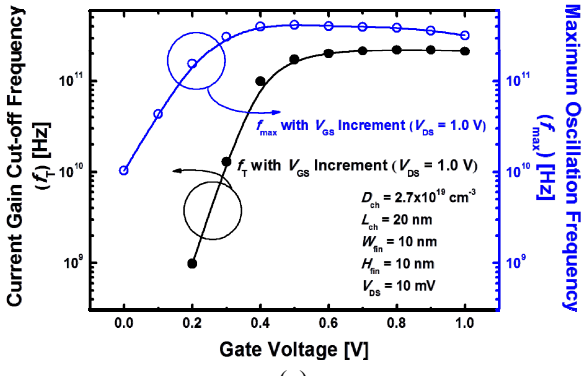
where g_m is the transconductance, C_{gg} is the gate input capacitance, $R_{g,eff}$ is the effective gate resistance comprising gate electrode resistance and distributed channel resistance, and C_{gd} is the gate-to-drain capacitance.



(a)



(b)



(c)

Fig. 13. (a) Capacitance and (b) resistance of optimized JL FinFET. (c) f_T and f_{max} as a function of V_{GS}. In both f_T and f_{max} are monotonically increases with voltages.

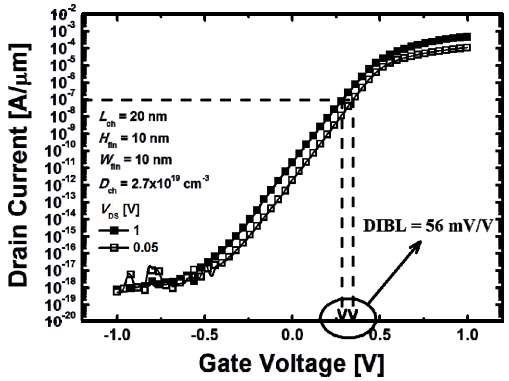


Fig. 14.IDS-VGS transfer curves for optimized JL FinFET and characteristics of DIBL.

Table 1. Optimized device performances and conditions summary

Channel Length (Lch)	20 nm
Fin Width (Wfin) Fin Height (Hfin)	10 nm 10 nm
Channel Doping Concentration (Dch)	2.7×10^{19} cm-3
Threshold Voltage (Vth)	0.3 V
On-state Current (Ion) Off-state Current (Ioff)	397A/m 1.32×10^{18} A/m
Subthreshold Swing (SS)	67.3 mV/dec
Current Gain Cut-off Frequency (fT) Maximum Oscillation Frequency (fmax)	213.3 GHz 366.6 GHz
Drain-induced barrier lowering (DIBL)	56 mV/V

Equation 2, it is known that to achieve high f_T, the large value of g_m should be needed. In Fig. 12, both g_m and g_{ds} increases and saturations near V_{GS} = 0.5 V. Thus, a desirable operation conditions to guarantee high f_T should be $V_{GS} > 0.5$ V.

Figs. 13 (a) and (b) shows the capacitance and resistance of optimized JL FinFET. These characteristics are related with f_T and f_{max} which expressed by equations (2) and (b). Fig. 13 (c) depicts the f_T and f_{max} as a function of V_{GS}. In both f_T and f_{max} are monotonically increases with voltages. The f_T and f_{max} was obtained 213.3 GHz and 366.6 GHz respectively at $V_{GS} = V_{DS} = 1$ V where an operation point.

Fig. 14 demonstrates the drain-induced barrier lowering (DIBL) characteristics of optimized JL FinFET. In terms of suppress SCEs (SS ≤ 100 mV/dec, DIBL ≤ 100 mV/V) [16], the optimized JL FinFET is efficiently satisfying these conditions.

5. Conclusion

In this paper, we have been performed 3D TCAD simulation of JL FinFET and confirmed the device performances. The JL FinFET is suitable semiconductor devices with LSPT applications and the optimum design of transistor was satisfying the requirement of ITRS roadmap. To optimize the JL FinFET, various DC parameters including V_{th}, I_{on}, I_{off}, SS, and g_m was considered. Through the simulation result, the optimum design conditions of JL FinFET with L_{ch} of 20 nm and t_{ox} of 2nm were as follows: D_{ch} of 2.7×10^{19} cm^{-3}, W_{fin} of 6 ~ 10 nm, and H_{fin} of under 10 nm. Finally, under the condition which D_{ch} of 2.7×10^{19} cm^{-3}, W_{fin} of 10 nm, and H_{fin} of 10 nm, the f_T and f_{max} were obtained as 213.3 GHz and 366.6 GHz respectively. Consequently, the optimized JL FinFET can be a promising structure of next-generation silicon-based LSPT transistors.

Acknowledgements

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