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Integrated Current-Mode DC-DC Buck Converter with Low-Power Control Circuit

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A low power CMOS control circuit is applied in an integrated DC-DC buck converter. The integrated converter is composed of a feedback control circuit and power block with 0.35 μm CMOS process. A current-sensing circuit is integrated with the sense-FET method in the control circuit. In the current-sensing circuit, a current-mirror is used for a voltage follower in order to reduce power consumption with a smaller chip-size. The N-channel MOS acts as a switching device in the current-sensing circuit where the sensing FET is in parallel with the power MOSFET. The amplifier and comparator are designed to obtain a high gain and a fast transient time. The converter offers well-controlled output and accurately sensed inductor current. Simulation work shows that the current-sensing circuit is operated with an accuracy of higher than 90% and the transient time of the error amplifier is controlled within 75 μsec. The sensing current is in the range of a few hundred μA at a frequency of 0.6~2 MHz and an input voltage of 3~5 V. The output voltage is obtained as expected with the ripple ratio within 1%.

Keywords: CMOS, Buck converter, Integrated, Current-sensing, Error amplifier, Sensing current

1. INTRODUCTION

Recently, a power management system has been used in many portable multimedia devices. The ULSI technology has developed the power system to be able to be integrated within multimedia devices. An integrated DC-DC converter is one of the important components in the system because it provides various supply voltages with low power consumption. The design of a high efficiency DC-DC converter [1-5] depends mostly on its control circuit. The converter is composed of a switching stage, LC filter, and feedback circuit. In this paper, a current-mode DC-DC buck converter is integrated with its feedback control stage. Among the various elements in the control stage, the current sensing circuit [6-9] and error amplifier [10] are crucial for the performance of the overall current-mode converter because the converter requires high accuracy of the PWM signal and fast dynamic response.

The current-sensing circuit requires low on-resistance transistors in order to obtain a full swing operation in the circuit. In the current-sensing technique by application of the sense-FET, a sense transistor measures the current in a power transistor to reduce the power consumption in a DC-DC converter. The application of a sensing transistor to measure the current in a power transistor usually requires an operational amplifier to achieve a high degree of accuracy. The operational amplifier forces the drain-source voltage of the power transistor to be the same as that of the sense transistor. If the sense transistor and the power device are constructed such that the sense transistor is K times smaller than the power transistor, then the drain current in the sense transistor is also K times smaller. In this work, the sensing circuit [6] does not use an operational amplifier because it will induce another consideration of the minimum supply voltage, the stability of the sensing circuit, and the input common-mode range. The operational amplifier is replaced with a simple voltage follower that keeps the follower's node voltages the same as the MOS current sources that dissipate low static power. Such a replacement can result in at least an order of magnitude improvement in speed as well as the reduction of power consumption.

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Another important element in the control circuit, the error amplifier, requires a high gain in the differential pair and high current-driving capability in the current sources to obtain a fast transient response without the slewing problem.

The structure of a current-mode boost converter is shown in Fig. 1, which is composed of a power stage and control stage. The power stage includes two n and p channel MOS switches and LC elements. The control stage is composed of an error amplifier, comparator, oscillator, pulse-width generator, and buffer. In order to provide low power and a fully integrated power module, a current-mode DC-DC buck converter with on-chip current sensor has been designed from post-layout simulation with a standard 0.35 μm CMOS process. The off-chip LC filter is designed with an inductance of 8 μH and capacitance of 1 mF. The input voltage of the error amplifier is obtained by the divider with R_1 and R_2.

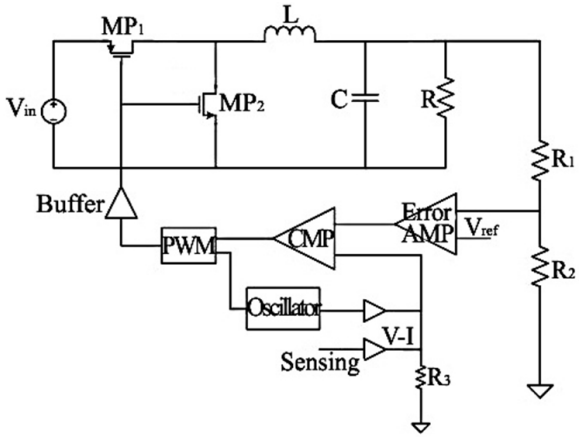

Fig. 1. Block diagram of a current-mode buck converter.

2. THEORY

2.1 Current-sensing circuit

A current-sensing circuit using a sensing FET requires an operational amplifier to act as a voltage mirror [1] and measure the current in the power MOSFET; however, the operational amplifier has the limitation of slew rate and offset voltage in the integrated circuit. In this current-sensing circuit, a current mirror replaces the operational amplifier and works as a voltage follower. Compared to an operational amplifier, the current mirror is a simple circuit to have a low on-resistance, therefore, a high accuracy of the sensing circuit with a low supply voltage is possible.

The current sensor in Fig. 2 is realized by the power PMOS transistor M_2 and SENSEFET M_0. The voltage follower with two MOSFETs M_4 and M_5 is applied, to make the source voltages of M_4 and M_5 the same. The voltage follower is used as a current mirror instead of an operational amplifier such that the scaled inductor current is matched to the sensing current I_{sense}.

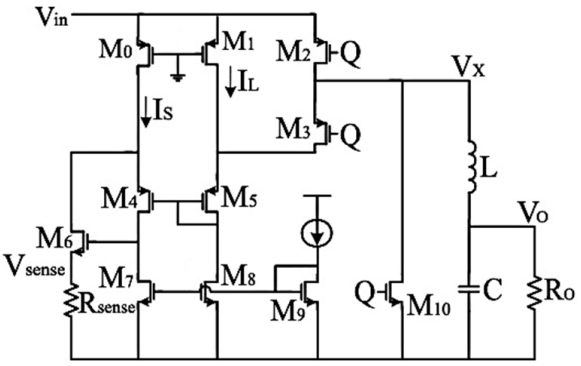

Fig. 2. Low-power current-sensing circuit.

The transistors M_3 and M_{10} are the switches for the ON-OFF states. The matching of transistors M_0 and M_2 depends on the parameters including channel length and width. Other process parameters are adjusted to be the same. In this design, the size ratio of the power MOSFET to the sensing transistor is K = 1,000 to reduce the power consumption in the sensing FET. Any change in the source voltage of M_4 will force a similar change in the other voltage of M_5. However, the transistors M_0 and M_2 are scaled so that the power transistor M_2, on the output side of the circuit, has an aspect ratio of 1,000:1, which is much greater than that of the transistor M_0 on the sensing side. Therefore, the sensing current I_s, which is the drain current of M_0, is much smaller than the output current that passes to the load resistor R_o. For the current mode DC-DC buck converter application, only the sensing-voltage, V_{sense}, is required in the control feedback loop during the on-state, and the signal from the power transistor M_2 during the turn-on is sensed.

During the ON period of the current-sensing circuit shown in Fig. 3, the MOS transistor M_{10} is turned off by setting Q low, while M_2 and M_3 are turned on. Because the voltage follower provides the source nodes of M_4 and M_5 the same, the drain current of the transistor M_2 is mirrored to the transistor M_0. As the transistors M_0 and M_2 have almost the same drain voltages, the drain currents of the transistors will depend on the aspect ratio of the channels. Thus, the output current I_{out}, which passes through the power transistor M_2, is much larger than the drain current on the sensing side. The sensing current I_{sense} passing through the resistor R_{sense} is the scaled inductor current. If K is the aspect ratio between the power FET M_2 and sensing FET M_0, the drain current in the transistor M_2 can be approximately written as $I_2 = K I_0$, where I_0 and I_2 are the currents in the transistor M_0 and M_2, respectively. Therefore, the sensing current I_{sense} can be approximately I_0 during the ON period.

During the OFF period of the sensing circuit as shown in Fig. 4, the MOS switches M_2 and M_3 are turned off while M_{10} is turned on. By switching off the transistors M2 and M_3, the sensing circuit is disconnected from the power stage. Therefore, the sensing current through the resistor R_{sense} is almost the same as the small drain current in the transistor M_9 which comes from the current mirror with M_7, M_8, and M_9. In the power stage, the inductor current flows through M_{10}, transferring the stored inductor current to the load R_o.

A current mirror is used as a voltage follower such that the sensing current, I_{sense}, is matched to the inductor current I_L. The sensing signal, V_{sense}, is given by:

$$V_{sense} = I_{sense} R_{sense} = \frac{I_L}{1000} R_{sense} \quad (1)$$

The resistor, R_{sense}, is used to convert the current signal to a voltage signal such that V_{sense} is proportional to the sensing current.

2.2 Error amplifier

The error amplifier in Fig. 5 is the cascoded OTA (opera-

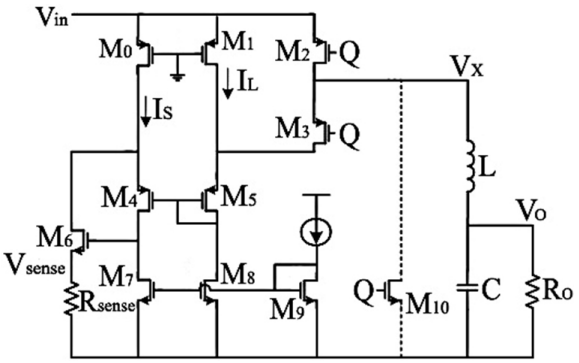

Fig. 3. Current-sensing circuit, during the ON period.

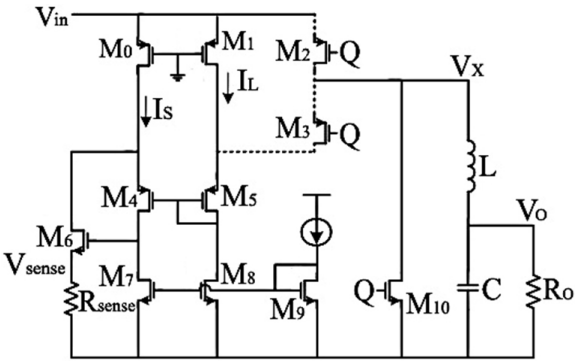

Fig. 4. Current-sensing circuit, during the OFF period.

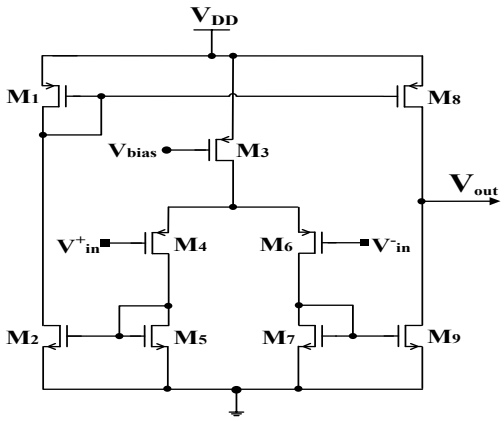

Fig. 5. Error amplifier in CMOS technology.

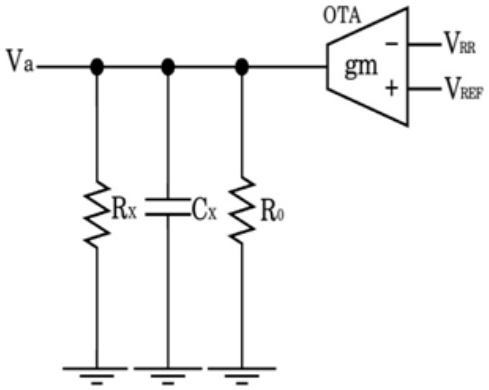

Fig. 6. Schematic of compensator with OTA.

tional trans-conductance amplifier). The OTA is composed of input differential stage and current mirrors. A compensation circuit is added to the amplifier in order to get the stability of frequency response and fast response-time. The compensator is composed of the capacitor and resistor to generate poles or zeros to yield a sufficient phase margin for high stability. OTA requires a large current supply for the compensating capacitor to be able to charge and discharge quickly. If the current supply is not enough, OTA has a limitation of its speed due to the low slew rate. The OTA has a p-MOS differential-amplifier, current-mirrors, and cascode bias. A source-follower is included as an output buffer to reduce power loss by the output impedance. A large current supply is obtained by the cascode bias and the geometrical ratios between transistors. The range of the output swing and DC operating current are carefully considered for large-signal operation. The differential-amplifier is designed with high trans-conductance and output resistance which are important parameters for a stable phase margin in frequency compensation.

The control-to-output transfer function in the current-mode converter is known to contain two poles and can be written in the following form [11]:

$$G(s) = k\frac{1}{1+(\frac{L}{R})s+LCs^2} \quad (2)$$

where K is a constant, and R, L, and C are the resistance, inductance, and capacitance in the power stage of the buck converter, respectively. Our work employed the two poles function (2) because the PWM signal in the current-mode converter is influenced by the sensing current and the LC filter.

The transfer function (2) can be approximated in the following form, depending on the range of the operating frequency. We are interested only in the function (4) in the high frequency range. As the other functions (3) and (5) provide a large enough phase margin in any condition, therefore, a compensation circuit or stability analysis is not required.

$$G(s) \simeq \frac{k}{1+(\frac{L}{R})s} \quad \text{(low frequency) (3)}$$

$$\simeq \frac{k}{(\frac{L}{R})s+LCs^2} \quad \text{(high frequency) (4)}$$

$$\simeq \frac{k}{1+LCs^2} \quad \text{(otherwise) (5)}$$

We can determine whether or not the converter circuit is stable by examining loop gain as a function of frequency. Figure 6 represents a compensator with OTA. The two resistors and a capacitor are used to generate another pole. The purpose of introducing a pole in the compensator is to provide a sufficient phase margin in the loop gain. The transfer function of the compensator is given by

$$A(s) \sim g_m R_t \frac{1}{1+sR_tC_x} \quad (6)$$

where g_m is the trans-conductance of the OTA and R_t is the equivalent resistance with Rx and R_o. The gain of the OTA is the multiplication of the trans-conductance and resistance. If the compensator resistance, Rx, is quite small compared to the output resistance R_o, the equivalent resistance in the transfer function can be approximately R_x. Because of the size limitation of the capacitor in an integrated circuit, the pole in the compensator to improve stability depends mostly on the resistance. The loop gain of the converter circuit depends on the multiplication of equations, (4) and (6). The purpose of introducing another pole due to the compensator is to provide a sufficient phase margin in the loop gain. When the pole frequency of the compensator is lower than the pole frequency of Eq. (4) which comes out from the power stage, the phase margin increases and more stability can be obtained. The frequency response of the transfer function (4) will be discussed later.

2.3 Comparator and buffer

The comparator in Fig. 7 is for the PWM control. One of the inputs in the comparator is the combined signal of the current-sensing and ramp signals. The ramp signal from the oscillator is added into the sensing current. As shown in the block diagram of Fig. 1, the two signals passing through the resistor R_3 add into a voltage which produces the PWM signal. The comparator is composed of current mirrors, input differential stage, and inverters. The bias circuit is the same as that of OTA in Fig. 3. The input differential stage is an active-loaded amplifier with a high trans-conductance. The load circuit consists of inverters connected to a current mirror configuration and thus presents the amplifier with a high resistance load.

The oscillator is implemented to obtain ramp signal and clock pulse. The oscillator and comparator are used for the PWM control. In pulse-width modulation (PWM) switching, the switch control signal is generated by comparing the output of the error amplifier with a repetitive waveform.

The buffer in Fig. 8 is composed of CMOS inverter chains, power transistors, and feedback loop. The feedback signal at A and B is used to control the gate driving signal such that the transistors M1 and M_2 do not switch simultaneously. The pull-up and pull-down transistors are driven by separate driving stages. The buffer can consume a large short circuit power during each switching transition and should be minimized for low power operation.

3. RESULTS AND DISCUSSION

The current-sensing circuit of the DC-DC buck converter has been designed in 0.35 μm CMOS technology with 2-poly and 4-metal process. The layout of the current-sensing circuit is shown in Fig. 9. The chip area is about 0.25 mm^2.

Figure 10 is the output wave forms of error amplifier (A) and comparator (B). This is obtained from the Cadence post-layout simulation of Fig. 1 which includes the power and control stages. The output of error amplifier (A) quickly settles down due to the high conductance g_m of the MOS differential amplifier. The comparator repeats the digital high and low logics after the signal (A) passes a transient response.

The transient time is about 75 μsec at the frequency of 200 KHz and supply voltage of 5 V. With variation of frequency and supply voltage, it was within 100 μsec down. This indicates that the proposed circuits of the error amplifier, compensator, and comparator work properly in the integrated DC-DC control circuit.

The stability of the control circuit is analyzed in terms of gain and phase margins. The transfer function (4), which relates to the natural frequency of the LC filter, can be rewritten in the following form which includes the poles.

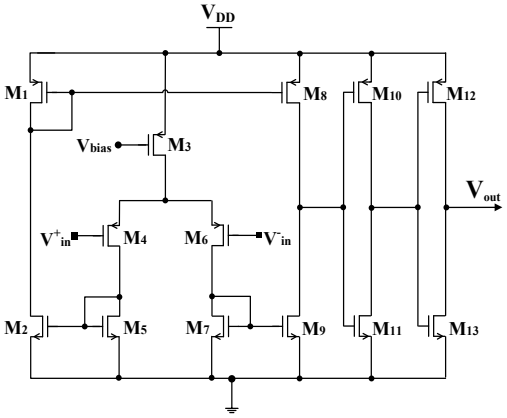

Fig. 7. Comparator.

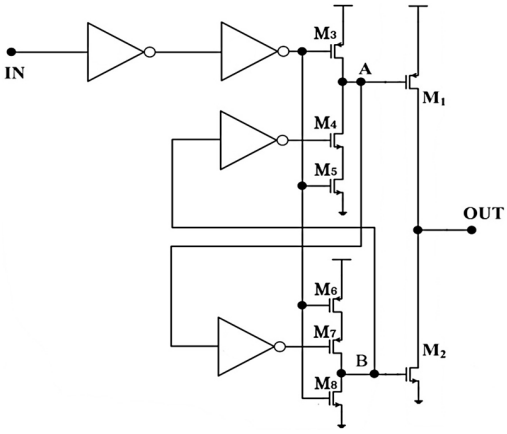

Fig. 8. Buffer.

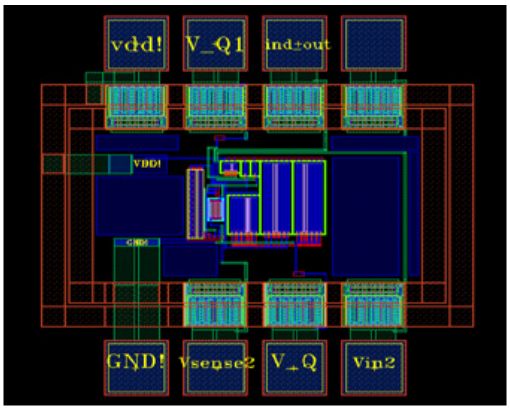

Fig. 9. Layout of the current-sensing circuit of the DC-DC buck converter.

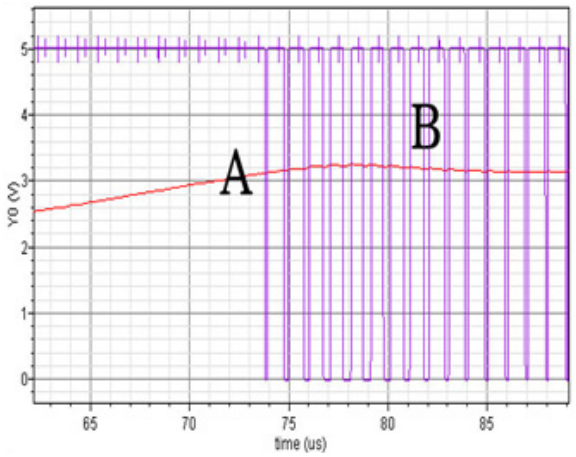

Fig. 10. Outputs of error amplifier (A) and comparator (B), at the frequency of 2 MHz.

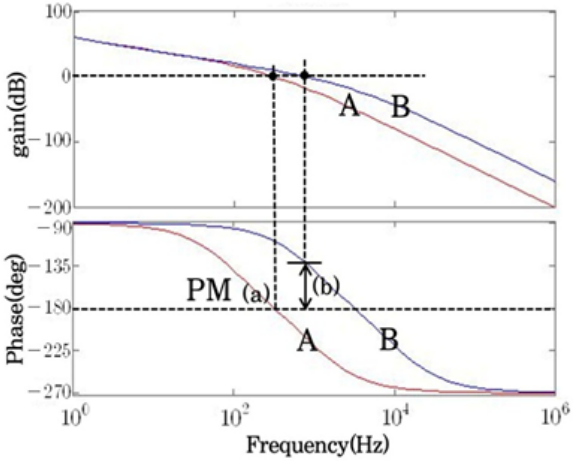

Fig. 11. Frequency response of the loop gain, with variation of the pole in the compensator.

$$G(s) \sim \frac{k}{s(1+sRC)} \tag{7}$$

Figure 11 is the Bode plot (magnitude and phase) of the loop gain, which is able to show the effect of the compensating circuit. It shows the frequency characteristics of the output of the error amplifier, which come from the multiplication of the equations (6) and (7). The frequency characteristic of the compensated error amplifier is combined into the control feedback loop characteristics of the DC-DC buck converter. The effects of the compensating circuit on the stability are studied in terms of the phase margin. The compensation pole comes from equation (6). The compensator pole frequency in graph A (B) is applied ten times higher (lower) than that of equation (7), which comes from the natural frequency of the LC filter. This shows that, if the compensator pole frequency is lower than the frequency of equation (7), the phase margin decreases and the stability deteriorates.

The frequency response in Fig. 11 shows the phase margin of (A) is lower than that of (B), where the phase margin (a) is almost 0°, while the phase margin (b) is 48°. The result indicates that the compensator frequency should be higher than the natural frequency, in order for the phase margin to increase and to provide a more stable condition in the frequency response. The optimal phase margin is over 60°.

Another element to affect the phase margin and stability is the gain of the error amplifier, as mentioned in equation (6). As the amplifier gain affects a quiescent current in the amplifier as well as the phase margin, we carefully consider both the DC operating condition and stability. The error amplifier is designed to maintain a small quiescent current during normal operation and be endurable to large-signal variation. In order to maintain the stability of the converter, the trans-conductance of the error amplifier is well controlled in this work.

Figure 12 is the sensing (A) and inductor (B) currents in the current-sensing circuit. This is obtained at the input voltage of 3 V and the switching frequency of 10 KHz. The sensing signal usually has a large time-delay between on-off switching state. In the sensing circuit in Fig. 2, the current mirror is used for the voltage follower and the current source, thus providing a larger current and smaller on-resistance. The sensing current (A) is almost matched to the inductor current (B) by the aspect ratio 1,000

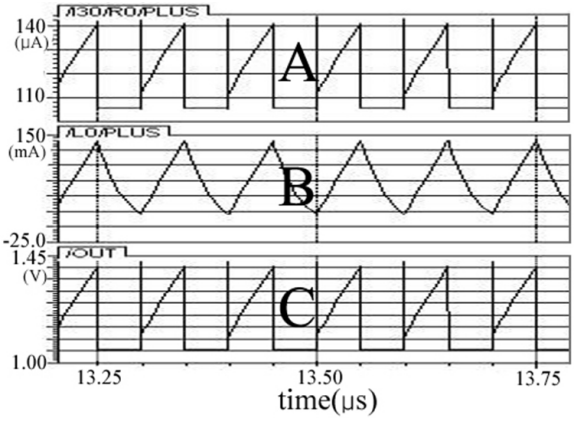

Fig. 12. Simulation result of the current-sensing circuit, sensing current (A), inductor current (B), and sensing voltage (C).

between the sense FET and power FET, corresponding to 125 μA with the inductor current of 135 mA. The accuracy is over 90%. The power consumption of the current-sensing circuit is under 0.2 mW.

The switching characteristic in the power stage is shown in Fig. 13, where the inductor voltage (A) and current (B) are shown at the duty-ratio of 65% and the inductor current is almost 17 mA. The inductor voltage V_x is measured after the inductor, in the block diagram of Fig. 1. This shows the continuous-conduction mode. The charging-discharging effect matches the duty ratio. The boundary between the continuous- and discontinuous-conduction mode depends mostly on the duty ratio. Figure 14 is the switching characteristics of the control circuit, where the outputs of comparator, V-I converter, and error amplifier are shown. The result is obtained as expected. The output of the comparator (A), which controls the PWM switching, is generated by comparing the amplifier output (C) with the repetitive waveform (B). As indicated in Fig. 1, the repetitive waveform (B) comes from the combination of the ramp signal from the oscillator and sensing signal. When the amplifier signal, which changes slowly with time, is smaller (larger) than the saw-tooth waveform, the output of the comparator becomes high, causing the switch to turn on (off).

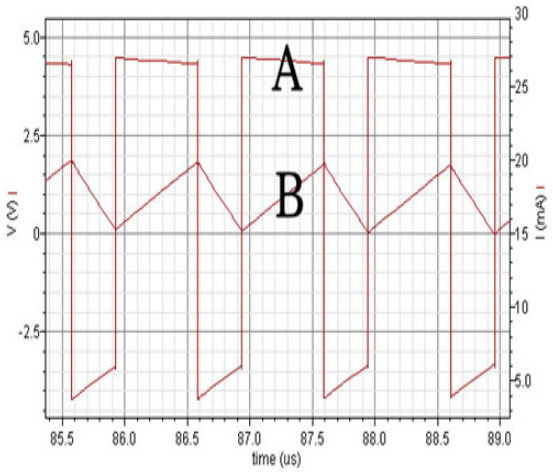

Fig. 13. Simulation voltage Vx before inductor (A) and inductor current (B) at the frequency of 0.6 MHz.

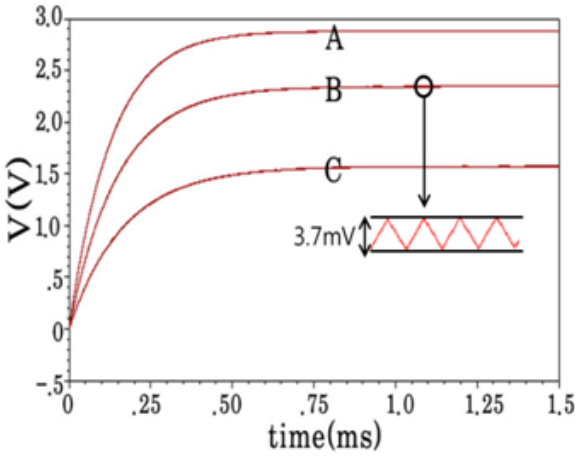

Fig. 15. Outputs with variation of the duty ratio (A: 70%, B: 50%, C: 30%).

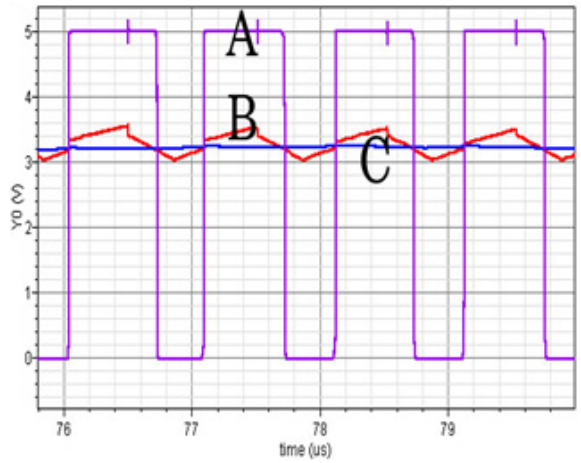

Fig. 14. Outputs of the comparator (A), V-I converter (B), and error amplifier (C).

The output of the DC-DC buck converter is shown in Fig. 15. With increase of the duty ratio, the output is supposed to increase linearly. At the duty ratio of 70%, the output obtained is smaller than expected. This may come from the voltage drop in p-MOSFET or the discontinuous-conduction mode. The output voltage (B) is 2.3 V with the ripple ratio under 1%, which is obtained at an input voltage of 5 V and duty ratio of 50%. The power consumption of the proposed converter is under 10 mW at a duty ratio of 50%.

4. CONCLUSIONS

A high performance current-sensing circuit and amplifier are introduced in an integrated current-mode DC-DC buck converter with 0.35 μm CMOS technology. The current-sensing circuit exploits a sense-FET and voltage-follower in order to significantly reduce the power consumption. The sense-FET and voltage-follower are used to match the inductor current accurately by the geometrical aspect ratio. In the error amplifier, a current-mirror OTA with high gain and large current source is used to obtain a fast transient response of within 75 μsec. From the post-layout simulation, the sensing accuracy of the current-sensing circuit is found to be over 90% with a power consumption of 0.2 mW. Simulation result of the sensing signal and output is obtained as expected at the input voltage of 5 V and frequency of 0.6 MHz.

ACKNOWLEDGMENTS

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