International Journal of Internet, Broadcasting and Communication Vol.5 No.2 11-14 (2013)
http://dx.doi.org/10.7236/IJIBC.2013.5.2.11

IJIBC 13-2-3

The Implementation of Sigma-Delta ADC/DAC Digital Block

Sang-Bong Park[1], Young Dae Lee[2] and Koki Watanabe[3]

[1]*Department of Information and Communication,semyung university, Korea*
psbcom@semyung.ac.kr

[2]*Department of Digital Media Engineering, Anyang University, Korea*

[3]*Department of Information and Communication Engineering, Fukuoka Institute of Technology, Japan*

Abstract

*This paper describes the sigma-delta ADC/DAC digital block with two channels. The ADC block has comb filter and three half band filters. And the DAC block has 5th Cascaded-of-Integrators Feedback DSM. The ADC and DAC support I2S, RJ, LJ and selectable input data modes of 24bit, 20bit, and 16bit. It is fabricated with 0.35um Hynix standard CMOS cell library. The chip size is 3700*3700um. It has been verified using NC Verilog Simulator and Matlab Tool.*

Keywords: *Sigma-Delta, ADC (Analog-to-Digital Converter), DAC (Digital-to-Analog Converter), Comb Filter, Half band Filter, Cascaded-of-Integrators Feedback.*

1. Introduction

The Sigma-delta modulation is very suitable structure for constructing high-performance A/D converter and D/A converter. Therefore, in this paper presents sigma-delta ADC/DAC for audio to perform high resolution and optimal SNR. The design is fabricated with 0.35 Hynix CMOS cell library. [1][2]

In section 2, we introduce sigma-delta ADC/DAC structure and explain in detail for each block. Section 3 describes about simulation and layout result. And section 4 shows a conclusion.

2. Sigma-Delta ADC/DAC

A Figure 1 shows a total block diagram. The block constructs digital ADC and DAC block. ADC digital block is inputted 1bit digital signal at 6.144MHz. It is used 128x oversampling and sampling frequency is 48 KHz. DAC block can select input mode as one of ADC output and external input. It has single and multi-bit output of 4bit per each channel by 5th sigma-delta modulator.

2.1 A. Sigma-Delta ADC Block

The sigma-delta ADC block consists of comb filter, three half band filter and two noaccum block. The combfilter is inserted input of +1 or -1 value through 3th analog sigma-delta modulator. [3]

The system of comb filter is as follows equation (1) and figure 2 is block diagram of comb filter.

Manuscript Received: Jun. 12, 2013 / Revised: Jul. 27, 2013 / Accepted: Aug. 9, 2013
Corresponding Author: psbcom@semyung.ac.kr
Tel: +82-43-649-1278, Fax: +82-43-649-1747
Dept. of Information and Communication, semyung university, Korea

$$H(z) = \left(\frac{1 - z^{-4}}{1 - z^{-1}}\right)^4 \left(\frac{1 - z^{-8}}{1 - z^{-4}}\right)^5 \left(\frac{1 - z^{-16}}{1 - z^{-8}}\right)^7 \qquad (1)$$

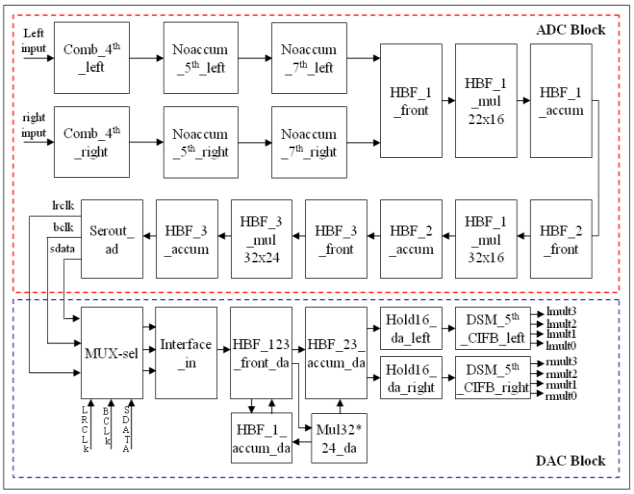

Figure 1. Sigma-Delta ADC/DAC Block Diagram

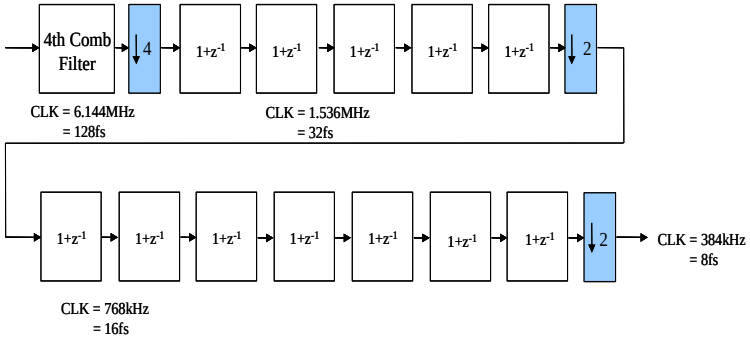

Figure 2. Comb filter System

Three half band filters follows comb filter. HBF can reduce hardware area and operation because it has 0 values in 2/n filter coefficient. HBF1 equation is (2). HBF2 and HBF3 take 22 and 116 coefficients respectively as the similar form of the equation of HBF1.

$$y[n] = c_0*x[n] + c_1*x[n-1] + c_2*x[n-2] + c_3*x[n-3] + c_4*x[n-4] + c_5*x[n-5] + c_6*x[n-6] + c_7*x[n-7] + c_8*x[n-8] + c_9*x[n-9] + c_{10}*x[n-10] + c_{11}*x[n-11] \quad (2)$$

2.2 B. Sigma-Delta DAC Block

The interface circuit determines input along bit mode (24bit, 20bit, 16bit) and interface mode (LJ, RJ, I^2S). It is outputted by 48 KHz. The output of interface is decoded on 32bit output signal and 24bit coefficient along HBF 1, 2, 3. HBF 1, 2, 3 is performed 2x oversampling for each filter. The hold block is the 16x oversampled. The 5^{th} digital sigma delta modulation is consisted of CIFB (Cascaded Integrators with distributed Feedback as well as distributed input coupling) structure. The input of DSM received 128x oversampled data from hold16 block. It generates output signal using noise shape to remove quantization error. It is outputted modulated signal of single bit and multi bit. The CIFB 5^{th} DSM is simulated SNR and characteristic using Matlab tool. The Xn is 32bit. But it uses 24bit of MSB. The coefficients of *bi* use 16bit.

The coefficients of *ai* have 0 or 1 value. If *yn* is 0, *ai* is *–bi*. But if *yn* is 1, *ai* is equal to *bi*. The second and third integrators, together with the feedback path –g1, computed output result with first integrator and coefficients. Similarly, the output of fourth and fifth integrators is computed with the feedback path –g2. Figure 3 shows a 5th CIFB DSM block diagram.

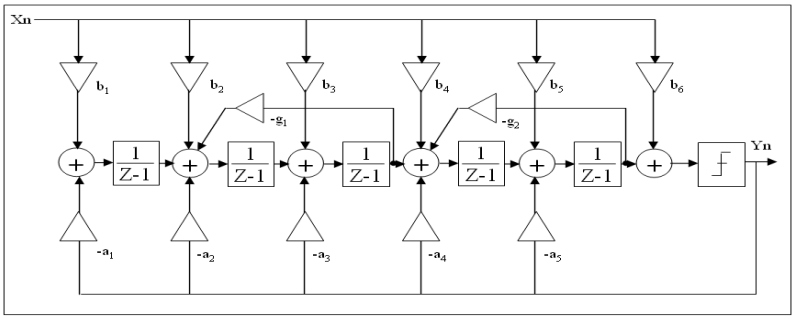

Figure 3. 5th CIFB DSM Block Diagram

3. Simulation and Layout Result

The top block verified using NC Verilog simulator tool. Figure 4 shows a layout result. It is used Hynix 0.35um Standard CMOS library. Figure 5 shows a post-simulation result.

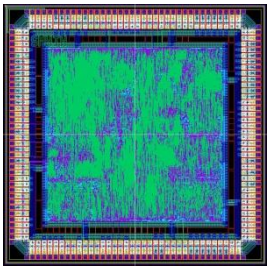

Figure 4. Layout Result

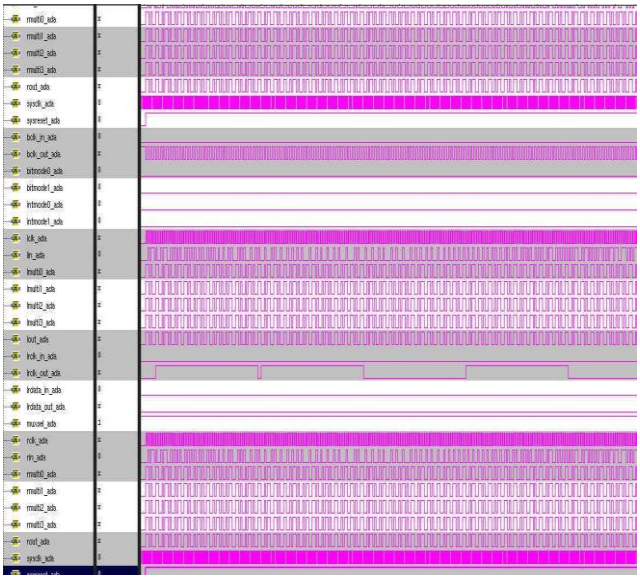

Figure 5. Simulation Result

4. Conclusion

In this paper, we described the sigma-delta ADC/ DAC digital block for audio. The characteristics of HBF and DSM have been simulated using Matlab tool. The logical block of ADC/DAC was described by using Verilig HDL and was verified by simulator tool. It was fabricated with Hynix 0.35um CMOS cell library. The chip size is 3700*3700um. Now we are testing with the chip and fabricated test board.

References

[1] Richard Schreier, Cabor C. Temes, "Understanding Delta-Sigma Data Converters", Wiley Interscience, 2005.
[2] James C. Candy & Gabor C. Temes, "Oversampling Delta-sigma Data Converters," IEEE PRESS, 1992.
[3] Implementation of sigma-delta A/D Converter IP for digital audio, ICEIC, pp 199-203, 2004.
[4] Data Manual, UDA 1360TS, Low-voltage low-power stereo audio ADC, Philips Semiconductor,March, 2001.
[5] Data Manual, 24-Bit 96 Khz Stereo Audio Codec, TEXAS Instruments, August, 1999.