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Communications

Single-Layer MoS_2 Field Effect Transistor with Epitaxially Grown $SrTiO_3$ Gate Dielectric on Nb-doped $SrTiO_3$ Substrate

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Over the past several decades, the aggressive scaling of Si-based metal-oxide-semiconductor field-effect transistor (MOSFET) devices has been successfully achieved. More recently, however, as the technology node approaches its physical limit down to 10 nm regime, alternative methodologies have been made for further extension of the Moore's law, which has mainly focused on implementation of high carrier mobility channel materials. Of various path findings, the advent of graphene, a fascinating two-dimensional (2D) crystal, has received intensive attention, especially due to its massless charge carriers.[1,2] Although the absence of intrinsic band gap limits its potential applications as novel channel materials, the discovery of the graphene has spurred the emergence of other material families with the layered structures including transition metal dichalcogenides (MoS_2, WS_2 and $NbSe_2$), and topological insulators (Bi_2Te_3 and Bi_2Se_3).[3-7] Interestingly, in contrast to the semimetal graphene, MoS_2 as one of the transition metal dichalcogenides has revealed the remarkable potential as the new channel owing to its semiconductor-like bandgap (a direct bandgap of ~1.8 eV for single-layer MoS_2), thermal stability, carrier mobility, and compatibility with the CMOS process.[4,5] To date, nevertheless, studies on MoS_2 electronics is still in their infancy, since only a few research groups have reported electrical properties of MoS_2-channel FETs based upon their theoretical predictions and experimental results.[4,8-10] In particular, further enhancement of its mobility is of upmost interest for the channel applicability because monolayer MoS_2 has previously showed poor mobility of < 30 $cm^2/V{\cdot}S$.[5,10,11] Though the field effect mobility could be significantly improved over ~1,000 $cm^2/V{\cdot}S$ from the dielectric screening effect by upper high-k dielectric passivation such as Al_2O_3 and HfO_2, it still requires more investigation with implementation of much higher permittivity dielectric.[12,13] In this work, therefore, we report properties of single-layer MoS_2 transistor with an epitaxially grown $SrTiO_3$ (STO) gate dielectric on a Nb-doped STO substrate.

Figure 1(a) schematically illustrates the MoS_2 nanosheet transistor. To begin with, the epitaxial STO film with a thickness of ~100 nm was deposited on Nb-doped STO (Nb:STO, Nb content ~1 wt % and resistivity ~0.001 Ω·cm) substrate by using pulsed laser deposition (PLD). To produce an atomically flat surface on the Nb:STO, which serves as a back-gate, it was dipped in a dilute HF solution, followed by high-temperature annealing at 1000 °C.[14,15] Then, the Nb:STO substrate had terraces with a uniform interval and step height of about 100 nm and 0.3 nm, respectively, and a very low surface roughness below 0.2 nm. After the 100 nm-thick epitaxial STO growth, monolayer MoS_2 sheet was exfoliated from commercially available bulk crystal (SPI Supplies) and then transferred to the STO/Nb:STO substrate. Finally, electrical source/drain (S/D) contacts were fabricated by electron-beam lithography and subsequent electron beam evaporation of 90 nm-thick Au. To improve the contact resistance, post annealing was carried out for 2 h in inert Ar atmosphere at 200 °C.

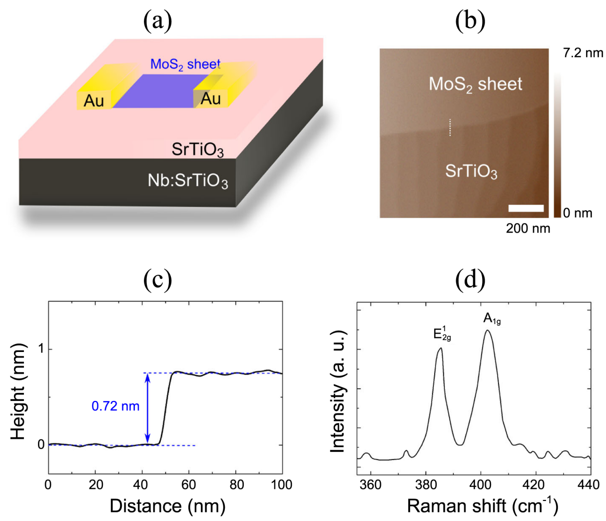

Figure 1. (a) Schematic illustration of the MoS_2 FET on STO/Nb:STO. (b) AFM image, (c) AFM cross-sectional profile, and (d) Raman spectrum of a single layer MoS_2 sheet on STO/Nb:STO.

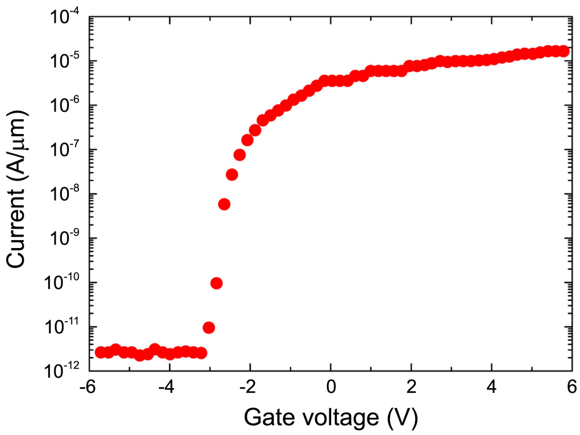

Figure 2. Transfer characteristic of the monolayer MoS_2 transistor with channel width and length of both 2 μm at V_{ds} = 0.5 V.

The surface morphology and thickness profile of the MoS_2 sheet were observed by atomic force microscope (AFM). Figure 1(b) exhibits the atomically flat surface morphology of the MoS_2 sheet, suggesting the formation of the layered MoS_2 structure. Besides, based on the AFM cross-sectional profile in Figure 1(c), the thickness of the MoS_2 film is ~0.72 nm, which corresponds to a monolayer MoS_2 flake elsewhere.[16] To further clarify the existence of monolayer MoS_2 sheet, Raman spectroscopy analysis was carried out. Raman characteristic bands at 386 and 404 cm^{-1}, which indicate two prominent peaks of E_{2g}^1 and A_{1g} modes, respectively, are clearly observed in Figure 1(d). Here, it is noted that the peak frequency difference (Δ) between E_{2g}^1 and A_{1g} modes can be used to identify the layer number of MoS_2 films. Accordingly, the Δ value of 18 cm^{-1} is well agreeing with that of monolayer MoS_2 in previous publications.[8,16]

Figure 2 shows the drain current-gate voltage (I_d-V_g) transfer curve of the MoS_2 FET. The current on/off ratio exceeds approximately ~10^7, which is comparable with the results elsewhere.[5,10] In addition to that, the maximum field effect mobility, $\mu = [dI_{ds}/dV_g] \times [L_g/WC_iV_{ds}]$, is calculated to be ~1460 cm^2/V·S at a drain voltage of V_{ds} = 0.5 V, whose value is much higher than that from previous reports.[12,13] It might be predominately attributed to the significant suppression in Coulomb scattering by charged impurities, which originated from surface adsorbates either at interface between MoS_2 and STO dielectric or on MoS_2 sheet. In other words, this scattering event can be reduced in MoS_2 on even higher permittivity STO dielectric due to more efficient dielectric screening of Coulomb potential, compared to SiO_2 and relatively lower high-k dielectrics such as Al_2O_3 and HfO_2.[17] Moreover, the high quality STO dielectric homoepitaxially grown on Nb:STO is also beneficial for effective reduction in surface scattering events due to its ultraflat surface.[18] However, it still needs more investigation as to which factor plays a significant role for the achievement of this high mobility.

In summary, we successfully fabricated the MoS_2 nanosheet transistor with epitaxially grown STO gate dielectric on Nb:STO substrate. The exfoliated MoS_2 sheet is found to be indeed single-layer, based on AFM and Raman analyses. Besides, it is envisaged that the MoS_2 transistor with high permittivity STO dielectric has great benefits for high-performance and low-power logic device applications due to its superior carrier mobility and on/off current ratio.

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