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실리콘 산화막에서 저레벨누설전류 특성

(The Characteristics of LLLC in Ultra Thin Silicon Oxides)

강 창 수*

(C. S. Kang©)

요 약

본 논문은 금속 산화물 반도체의 산화막 두께, 채널 폭과 길이에 따른 실리콘 산화막의 신뢰성 특성을 연구하였다. 스트레스전류와 전이전류는 스트레스 전압에 의하여 발생된다. 스트레스 유기 누설전류는 스트레스 전압 인가 동안과 인가 후의 실리콘 산화막에 나타난다. 이때 저레벨 스트레스 전압에 의한 저레벨 누설전류는 저전압 인가 동안과 인가 후의 얇은 실리콘 산화막에서 발생한다. 저레벨 누설전류는 각각 스트레스 바이어스 조건에 따라 스트레스전류와 전이전류를 측정하였다. 스트레스 채널전류는 일정한 게이트 전압이 인가동안 측정하였고 전이 채널전류는 일정한 게이트 전압을 인가한 후에 측정하였다. 본 연구는 소자의 구동 동작 신뢰성을 위하여 저레벨 스트레스 바이어스 전압에 의한 스트레스 전류와 전이전류가 발생되어 이러한 저레벨 누설전류를 조사하였다.

Abstract

In this paper, MOS-Capacitor and MOSFET devices with a Low Level Leakage Current of oxide thickness, channel width and length respectively were to investigate the reliability characterizations mechanism of ultra thin gate oxide films. These stress induced leakage current means leakage current caused by stress voltage. The low level leakage current in stress and transient current of thin silicon oxide films during and after low voltage has been studied from strss bias condition respectively. The stress channel currents through an oxide measured during application of constant gate voltage and the transient channel currents through the oxide measured after application of constant gate voltage. The study have been the determination of the physical processes taking place in the oxides during the low level leakage current in stress and transient current by stress bias and the use of the knowledge of the physical processes for driving operation reliability.

Keywords : Stress channel current, Low level current, Transient current, Stress current

Ⅰ. Introduction

Charge passing through the oxide of thin oxide MOS transistors has been observed to cause changes in transistor properties as a result of the generation of interface traps at the silicon oxide interface and the trapping of charge in the oxide. Both effects have led to threshold voltage shifts and transconductance changes and degradations of the oxide driving operations. If low voltage is applied to a thin oxide for sufficient lengths of time the oxide can low level leakage current. Since both trap generation and charge trapping have been considered to be causes of oxide leakage current. These effects have been considered important driving operation reliability problems.

* 정회원, 유한대학교 전자정보과
(Department of Electronic and Information Engineering, Yuhan University
© Corresponding Author(E-mail : cskang@yuhan.ac.kr)
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The charge injection reliability has been involved with the measurement and characterization of leakage current initiated by the passage of tunneling currents through the oxide. The study have been the determination of the physical processes taking place in the oxides during stress on time and stress off time and the use of the knowledge of the physical processes for reliability in the polarity dependence of the interface trap generation, the number and distribution of traps in a stressed oxide measured using low level stress currents, low level transient currents the effect of different gate materials and gate oxide thicknesses.

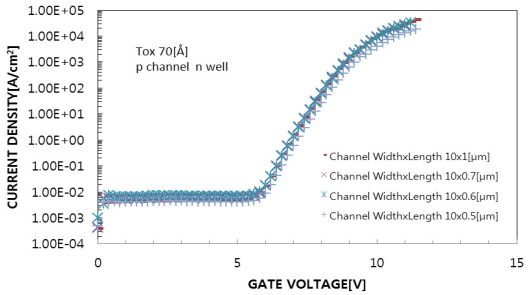

그림 1. 실리콘 산화막 70[Å], 채널 폭×길이 10×1[μm], 10×0.7[μm], 10×0.6[μm], 10×0.5[μm]인 소자에서 전압 대 전류밀도

Fig. 1. Current density vs. voltage characteristics of channel width×length 10×1[μm], 10×0.7[μm], 10×0.6[μm] and 10×0.5[μm] in a silicon oxides 70[Å].

Ⅱ. Discussion

The measurement methodology related to charge injection and trapping has been systematized to the following procedure in the initial current to voltage and current to time characteristics of the oxides were measured and then remeasured after various constant voltage stress levels had been applied. In the case of nondestructive testing of the oxides, the properties of unstressed oxides were first determined and were compared with the properties of oxides stressed at various levels. Current through the oxide was monitored in order to calculate the total charge that had passed through the oxide during the stress and the current to voltage measurements. Capacitors and transistors using n+ silicon gates were made on 2 to 5 ohm cm p-type silicon and 0.4 to 1.5 ohm cm n-type silicon, had been measured extensively and were used as and the capacitor areas varied from 5x10-5cm2 to 10-2cm2 and channel width×length 20×20[μm], 10×1[μm], 10×0.25[μm], 10×0.7[μm], 10×0.6[μm], 10×0.55[μm], 10×0.5[μm], 10×0.45[μm], 10×0.4[μm], 10×0.35[μm], 10×0.3[μm]. The larger area capacitors were used to confirm that the measurements reported here were representative of the intrinsic oxide and were not affected by either defects or perimeter effects. A gate oxide integrity test pattern involving many different oxide areas, perimeters, geometries, channel width and length, and fabrication processes was also used. The oxide thicknesses on these wafers varied from 41Å to 800Å in thickness. Typical plots of the current density to voltage characteristics of a silicon oxides 70[Å] in channel width×length 10×1[μm], 10×0.7[μm], 10×0.6[μm], 10×0.5[μm] have been shown in Figure 1.

The current density were measured using the ramped current to voltage characteristics with a sweep rate of 0.2 V/step and a step rate of 2 sec/step. The lack of a polarity dependence to the interface trap generation rate indicated that hot electrons were not involved in the trap generation process. The interface trap generation rate dropped as the fluence increased. The silicon oxide fluence of channel width×length 10×1[μm], 10×0.7[μm], 10×0.6[μm], 10×0.5[μm] were 1.03×109 [A/cm2], 4.30×108 [A/cm2], 4.01×108[A/cm2], 4.29×107 [A/cm2]. The electrons through the oxide at low fluences had a higher probability of breaking a low energy bond than did electrons that passed through the oxide at higher fluences. The interface trap generation rate was inversely proportional to the square root of the fluence. There was a voltage dependence to the interface trap generation at every fluence level measured.

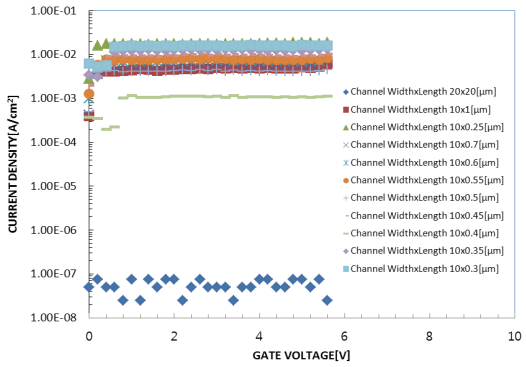

그림 2. 실리콘 산화막 70[Å], 채널 폭×길이 20×20[μm], 10×1[μm], 10×0.25[μm], 10×0.7[μm], 10×0.6[μm], 10×0.55[μm], 10×0.5[μm], 10×0.45[μm], 10×0.4[μm], 10×0.35[μm], 10×0.3[μm]인 소자의 전압 대 저전류밀도

Fig. 2. the low level current density vs. voltage characteristics of channel width×length 20×20[μm], 10×1[μm], 10×0.25[μm], 10×0.7[μm], 10×0.6[μm], 10×0.55[μm], 10×0.5[μm], 10×0.45[μm], 10×0.4[μm], 10×0.35[μm], 10×0.3[μm] in a silicon oxides 70[Å].

Typical plots of the low level current density to gate voltage characteristics of a silicon oxides 70[Å] in channel width×length 20×20[μm], 10×1[μm], 10×0.25[μm], 10×0.7[μm], 10×0.6[μm], 10×0.55[μm], 10×0.5[μm], 10×0.45[μm], 10×0.4[μm], 10×0.35[μm], 10×0.3[μm] have been shown in Figure 2.

The number of interface traps and oxide charges generated during high voltage stressing of the transistors was measured as a function of the stress voltage, polarity, substrate type, and fluence. It was found that the interface trap generation rate at the silicon oxide interface was independent of the stress polarity or the substrate type.

Typical plots of the time to current characteristics of a capacitor during and after dc stressing, with the p-type silicon surface in accumulation, have been shown in figure 3 and figure 4.

The low level current increased and the tunneling current decreased after the stress. The magnitude of this low level current was higher for higher stresses, but was not directly proportional to the stress or to the number of interface traps generated by the stress.

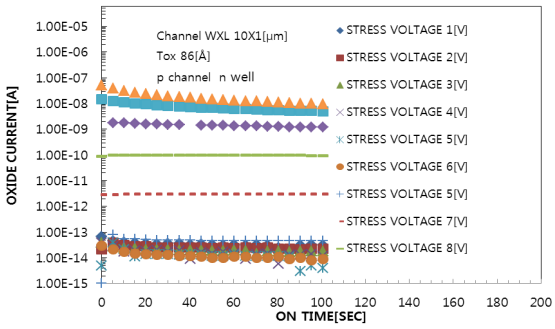

그림 3. 실리콘 산화막 86[Å]인 소자에서 고전압 인가 동안 시간에 따른 산화막 전류

Fig. 3. Current vs. on time characteristics of a 86[Å] thin silicon oxide during and after high voltage stressing.

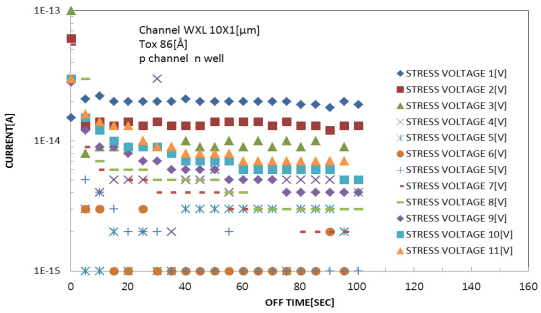

그림 4. 실리콘 산화막 86[Å]인 소자에서 고전압 인가 후의 산화막 전류

Fig. 4. Current vs. off time characteristics of a 86[Å] thin silicon oxide after high voltage stressing.

The negative differential current region often seen at low voltages was related to the variation in the flat band capacitance region and was a displacement current.

This I-V characteristic was characterized by a precipitous increase in current and was accompanied by the generation of a permanent low resistance path between the substrate and the gate. The generation of the interface traps was found to be dependent only on the fluence and field during the stress and on the stress polarity.

Channel current to time characteristics of thin oxide during and after application of a voltage pulse was shown in figure 5 and figure 6.

It had been observed that the transient low level

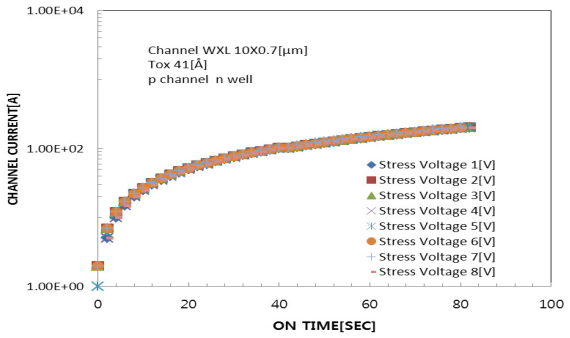

그림 5. 전압 펄스 인가 동안 실리콘 산화막의 채널 전류

Fig. 5. Channel current to on time characteristics of thin oxide during application of a voltage pulse.

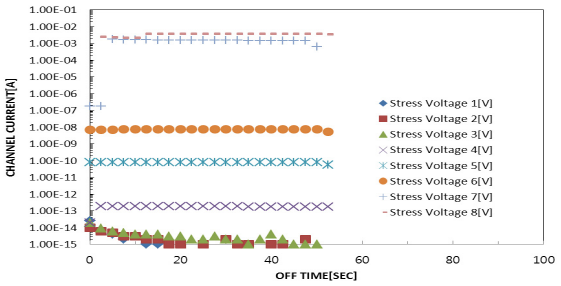

그림 6. 전압 펄스 인가 후의 실리콘 산화막의 채널전류

Fig. 6. Channel current vs. off time characteristics of thin oxide after application of a voltage pulse.

channel currents through stressed transistors did not have exponential decays with time. The low level channel current has been plotted as a function of time both when a voltage pulse was applied to the gate and after the pulse had been removed. For low voltages the decays, either when the voltage was on or after the voltage had been removed, were well fitted by exponential decays with an RC time constant that was appropriate for the transistors being studied. If the voltage pulse was high enough to create traps in the oxide, then the decays after the voltage pulse had been removed did not fit an exponential decay. Even at low voltages the decays after application or removal of a voltage pulse did not have an exponential decay if the transistor had been

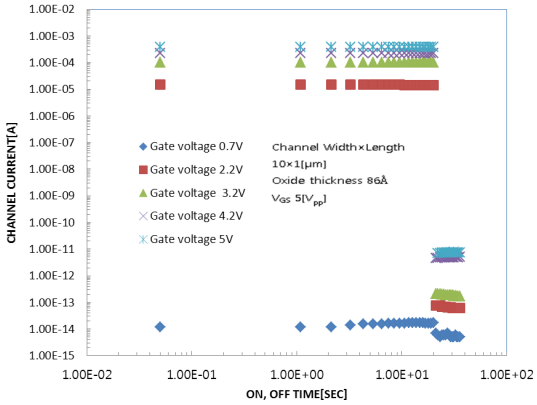

그림 7. 실리콘 산화막에서 전압 펄스 인가 동안과 인가 후의 채널전류

Fig. 7. Channel current vs. on off time characteristics of channel current during and after application of a voltage pulse in thin oxide.

stressed and traps had been generated in the oxide.

A typical current voltage characteristic for a thin silicon oxide was composed of three regions, the low level region, the tunneling region and the breakdown region. Onset tunneling voltage was measured 7.2[V] with fluence 1.07×10-8[C/cm2] and breakdown voltage was measured 17.5[V] with fluence 1.29×10-1[C/cm2] in oxide thickness 113.4Å. Prior to the onset of tunneling the currents were in the low ampere range. Constant voltages with tunneling currents were used to stress the oxides. The stress channel currents were measured on time during the stress and integrated to obtain the fluence through the oxide. The transient channel currents associated with the off time of the stress voltages were measured.

The stress channel currents through an unstressed oxide measured during application of constant gate voltage and the transient channel currents through the stressed oxide measured after application of constant gate voltage. The constant gate voltages were on time when the channel currents flowed and were off time when the channel currents flowed. As long as the applied voltages were less than the onset voltage of the tunneling current, the transient channel currents were represented by the charging and

discharging in silicon oxide.

The channel current after removal of a pulse and during pulse that generated traps in the oxide and charged these traps has been shown in figure 7.

When the voltages applied to the oxide were increased, the transient channel currents and stress channel currents were measured with transistor channel width×length 10×1[μm] during the channel applied voltage 5[V] after stress voltage 0.7[V], 2.2[V], 3.2[V], 4.2[V], and 5[V] in oxide thickness 86 [Å], as shown in figure 7.

The stress channel currents associated with the voltage application were on time for the voltages for which FN tunneling was significant. The stress channel currents reflected the changes in the shape of the tunneling barrier were due to trapping of electrons in the oxides. The transient channel currents after stress voltage were off time were decayed slowly. The transient channel currents followed an exponential decay. The transient channel currents were to stress the transistor at voltages and then measured the transient channel currents through the transistor at applied voltages after the stresses. The transient channel currents during the channel applied voltage 5[V] after stress voltage 0.7[V], 2.2[V], 3.2[V], 4.2[V], and 5[V]. The transistor in this case was stressed at 0.7[V], 2.2[V], 3.2[V], 4.2[V], and 5[V] for 100[sec] respectively. The stress and transient channel currents were measured after the stress at channel applied voltage 5[V] for 100[sec]. Higher stress voltages produced higher fluences through the oxides and associated with higher transient channel currents subsequently measured at low voltages. Both the charging and discharging oxide currents measured at the low voltages rose as the stress fluence rose.

The stress channel currents were to stress the transistor at stress bias voltages and then measured the stress channel currents through the transistor channel width and length 10×1[μm] in oxide thickness 41Å, 70Å, 86Å, 112Å, 139Å at applied voltages

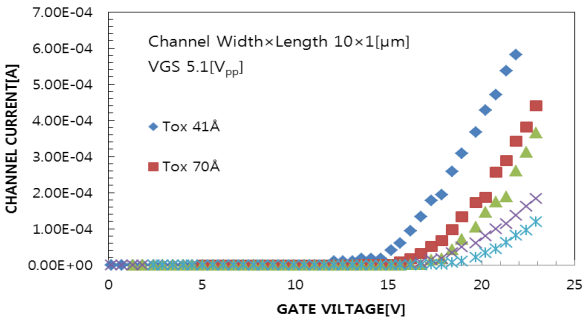

그림 8. 인가전압 5.1[V]에서 채널 폭×길이 10×1[μm]인 소자에서 실리콘 산화막 41[Å], 70[Å], 86[Å], 112[Å], 139[Å]에서 스트레스 채널전류

Fig. 8. The stress channel currents of the transistor with channel width and length 10×1[μm] in oxide thickness 41Å, 70Å, 86Å, 112Å, 139Å at applied voltages 5.1[V].

after the stresses as shown in figure 8.

The transistor in this data was stressed at applied voltage 5.1[V] for the transistor with channel width and length 10×1[μm] in oxide thickness 41Å, 70Å, 86Å, 112Å, 139Å respectively. The stress channel currents were measured after the stress at 5[V]. Whenever the measurement voltage was bias to the device, measurement had a period interval time change the charge state of the traps. After the 5.1[V] voltages were applied to an oxides thickness 41Å, 70Å, 86Å, 112Å, 139Å respectively, the channel currents decayed due to the oxide thickness charged traps generated respectively. The trap generation processes the traps were remained in their positions inside the oxides. Thicker oxide thickness produced lower fluences through the oxides and associated with lower channel currents subsequently measured at low voltages.

Channel current to voltage characteristics of an oxide bias voltage during sawtooth wave stressing through the transistor with channel width and length 10×1[μm] in oxide thickness 41Å, 70Å, 86Å, 112Å, 139Å as shown in figure 9.

The excess current present during the first measurement was traced to the charging of traps generated by the stress. If these traps were near the silicon oxide interface than a shift in the flat band

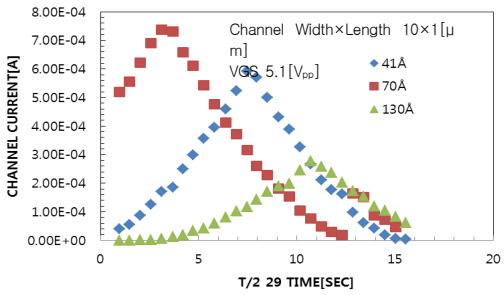

그림 9. 실리콘 산화막 41[]Å], 70[Å], 86[Å], 112[Å], 139[Å], 채널 폭×길이 10×1[μm]인 소자에서 톱니파 스트레스 전압 인가 동안 채널전류

Fig. 9. Channel current vs. voltage characteristics of an oxide bias voltage during sawtooth wave stressing through the transistor with channel width and length 10×1[μm] in oxide thickness 41Å, 70Å, 86Å, 112Å, 139Å

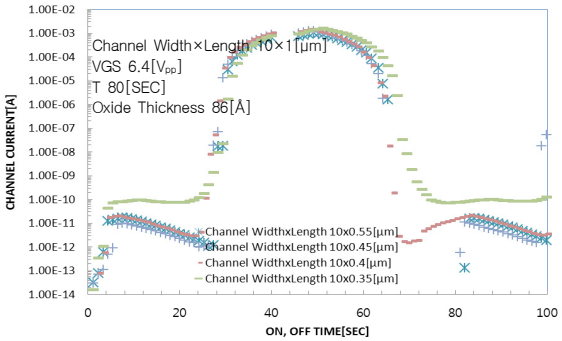

그림 10. 실리콘 산화막 86Å, 채널 폭×길이 10×0.35[μm], 10×0.4[μm], 10×0.45[μm], 10×0.55[μm]인 소자에서 구형파 Vpp 6.4[V]를 인가하는 동안 채널전류

Fig. 10. Channel current to time characteristics of an oxide bias voltage during rectangular wave pulse V_{pp} 6.4[V] stressing through the transistor with channel width and length 10×0.35[μm], 10×0.4[μm], 10×0.45[μm], 10×0.55[μm] in thickness 86Å thin oxides after stressing.

voltage from the first to subsequent measurements was observed. If these traps were at the oxide gate interface, the excess low level leakage current was still observed, but no shift in the flat band voltage was observed as shown. Similar I-V data was taken on transistors stressed at applied sawtooth voltage 5.1[V] for the transistor with channel width and length 10×1[μm] in oxide thickness 41Å, 70Å, and 139Å respectively. The position and charge state of the traps generated at the silicon oxide and gate oxide interfaces will be determined as a function of stress level, stress polarity, and polarity of the surface after the application of the stress. The room temperature relaxation of the oxide charge and interface traps will be measured.

Channel current-voltage characteristics of an oxide bias voltage during rectangular wave pulse Vpp6.4[V]stressing through the transistor with channel width and length 10×0.35[μm], 10×0.4[μm], 10×0.45[μm], 10×0.55[μm] in thickness 86Å thin oxides after stressing as shown in figure 10.

The decay channel current after removal of a pulse that generated traps in the oxide and charged these traps has been shown in figure. where the currents and tine have both been plotted on log axes. The channel current decayed with a 1/t time dependence indicating a uniform trap distribution within the oxide. The trap distribution derived from the decay current has been plotted in Figure.

LLLC as a function of transistors with channel width and length, oxide thickness measurement of the charge state of stress generated traps. It had also been shown that the charge state of these traps could be changed to application of a low voltage pulse at the end of the stress. It had been observed that the low level leakage current increased after low voltage stressing. The increase in the low level leakage current was dependent on the sign of the stress voltage and the sign of the voltage used to measure the low level leakage current. A portion of this increased current was identified with the charging or discharging of traps near the interfaces. The currents measured after stress were measured with the opposite polarity from the stress voltage.

III. Conclusions

The channel currents associated with low voltage pulses applied to thin oxide of the polysilicon gate

Metal Oxide Semiconductor capacitors and field effect transistors have been analyzed in terms of the charging and discharging of stress generated traps in the oxide.

The low level leakage current was used to explain the time dependence of the decay current after application of a low voltage pulse. It had been observed that the low level leakage current increased after low voltage stressing. The increase in the low level leakage current was dependent on the sign of the stress voltage and the sign of the voltage used to measure the low level leakage current. The trap densities derived within the oxide were the same order of magnitude as the interface trap densities measured at the silicon oxide interface on similarly stressed oxides.

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저 자 소 개

전자공학회 논문지
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