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A Simple Current Ripple Reduction Method for B4 Inverters

Dong-Myung Lee†, Jae-Bum Park* and Hamid A. Toliyat*

Abstract – This paper proposes a simple current compensation method to improve the control performance of B4 inverters. Four-switch inverters so called B4 inverters employ only four switches. They have a split dc-link and one phase of three-phase motors is connected to the center-tap of split dc-link capacitors in B4 inverters. The voltage ripples in the center tap of the dc-link generate unbalanced three-phase voltages causing current ripples. To solve this problem, this paper presents a simple compensation method that adjusts switching times considering dc-link voltage ripples. The validity of the proposed method is verified by simulations and experiments carried out with a 1 HP induction machine.

Keywords: B4 inverters, Current ripple reduction, Split dc-link.

1. Introduction

In order to save energy and improve the control performance, variable speed drive systems using inverters are adopting widely. In spite of the benefits from employing inverter systems, due to the cost increased by inverters, much research is carried out to find out ways of getting high quality product with lower cost. For one of cost-effective driving schemes, an inverter topology, so called B4 inverter, using four switches instead of six switches for controlling 3 phase motors has been introduced [1].

PWM schemes for generating balanced three-phase voltage with the component minimized inverter scheme has been investigated in [2, 3]. B4 inverters have serially connected dc-link capacitors, and the center point of dc-link is connected to one phase of three phase motors or loads. Among switching operation, there exists switching modes in which only one part(upper or lower part) of dc-link capacitors is involving in power delivery, which causes voltage difference between the upper capacitor and that in the lower part of dc-link capacitors. This voltage difference results in the discrepancy between the generated voltage vector and reference voltage in magnitude and angle, and generates current ripples due to the unbalanced three phase voltage. In order to solve this problem, many researches for generating balanced three phases with the consideration of voltage distortion have been presented [4-8].

In [4], to take into account voltage imbalances, measured dc-link capacitors voltages was used in the equations for calculating switching times. In [6], a space vector PWM method for B4 has been proposed, but the procedure for generating PWM pattern for that is complicate. In [7], the current flowing through the center point of dc-link capacitors was involved for determining the switching time to reduce current ripples. In [8], the cause and effect of dc-link imbalance have been investigated in detail.

B4 inverters are researched as a low cost driving scheme for induction motors as well as brushless DC motors [9-11]. Also they are considered as a provision for the emergency operation against inverter failure [12]. In addition, beyond motor drive applications, the adaption of B4 topology for the area of renewable energy and power quality compensators has been proposed [13, 14]. B4 inverters are widely studying and their application area is expending recently. Therefore, research for the B4 topology is highly required, especially the reduction of current ripples due to its split dc-link capacitor.

This paper expends the research done in [5] by the same author. In [5], a current ripple reduction method achievable by a low grade microcontroller has been presented. Meanwhile, in [5] the current ripple reduction method was applied to a wye(Y)-connection motor and demonstrated by simulation studies. The magnitude of phase voltages generated by B4 inverters is smaller than that by conventional inverters, and delta(Δ)-connection has a higher phase voltage compared with Y-connection. Hence, it is worth to apply and analyze the ripple reduction method applied in Δ-connected motors as well. Therefore this paper presents a current ripple compensation method for motors having Y or Δ-connection. The validity of the proposed method is experimentally verified with an induction motor.

2. B4 inverters

2.1 Configuration and operational principle

Conventional 2-level inverters, so called B6 inverters, have six switches, and each pole of the inverter is connected to each terminal of the motor. On the other hand,

† Corresponding Author: School of Electronic and Electrical Engineering, Hongik University, Korea. (dmlee@hongik.ac.kr)
* Dept. of Electrical and Computer Engineering, Texas A&M University, USA.
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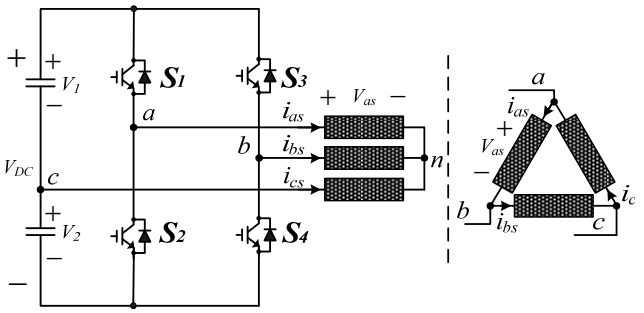


Fig. 1. Configuration of B4 inverters for Y or Δ-connected motors or loads.

the so called B4 inverter shown in Fig. 1 has four switches and one of the motor phases is connected to the central point of dc-link capacitors.

With conceptually applied the reverse phase voltage in the motor phase connected to the middle point of dc-link, B4 inverters generate three-phase voltages as shown in Fig. 2. As a result, the generated two inverter pole voltages has components of balanced three-phase voltages and zero sequence voltages, thus enable to control three phase motors [1]. Fig. 2 shows voltage phasor diagrams for (a) Y and (b) Δ-connected motors with the condition that the motor phase C is connected to the middle point of dc-link capacitors. Through this paper, it is assumed that the phase C of the motor is connected to the dc-link for the analysis as well as simulations and experiments. Where V_a and V_b are the pole voltages. V_{as}, V_{bs}, and V_{cs} are motor phase voltages.

Fig. 2 shows the magnitude of phase voltage for Y-connection is less by $1/\sqrt{3}$ compared to the inverter pole voltage. While, that of Δ-connection is the same as the magnitude of pole voltage. From Fig. 2(a) for Y-connection, it can be known that V_a and V_b can be expressed as (1). T_a and T_b are switching time of S_1 and S_3 for generating V_a and V_b, having 60° difference between them. m_a ranges from 0 to 1, and T_a and T_b are obtained as that from sinusoidal PWM. Where, m_a, T_s, or θ is modulation index, sampling time, or angle of reference voltage. V_o is the magnitude of phase voltage.

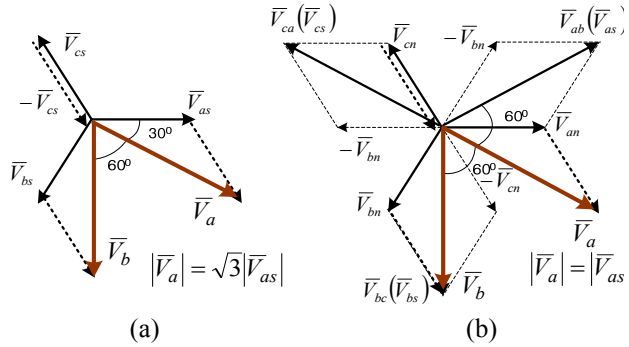


Fig. 2. Voltage phasor diagrams of B4 inverters with (a) Y-connection and (b) Δ-connection.

$$
\begin{aligned}
V_a &= \sqrt{3}V_o \sin\left(\omega t - \pi/6\right) \\
\Rightarrow T_a &= \frac{1}{2}\left[1 + m_a \sin\left(\theta - \pi/6\right)\right]\cdot T_s \\
V_b &= \sqrt{3}V_o \sin\left(\omega t - \pi/2\right) \\
\Rightarrow T_b &= \frac{1}{2}\left[1 + m_a \sin\left(\theta - \pi/2\right)\right]\cdot T_s
\end{aligned}
\tag{1}
$$

The reference pole voltage for Δ-connection can be obtained as (2). Comparing to Y-connection, Δ-connection has a 30 degree difference, and $\sqrt{3}$ times bigger phase voltages.

$$
\begin{aligned}
V_a &= V_o \sin\left(\omega t - \pi/3\right) \\
\Rightarrow T_a &= \frac{1}{2}\left[1 + m_a' \sin\left(\theta - \pi/3\right)\right]\cdot T_s \\
V_b &= V_o \sin\left(\omega t - 2\pi/3\right) \\
\Rightarrow T_b &= \frac{1}{2}\left[1 + m_a' \sin\left(\theta - 2\pi/3\right)\right]\cdot T_s
\end{aligned}
\tag{2}
$$

In each connection, generated phase voltages according to (1) and (2) have 4 different effective voltage vectors as listed in Tables 1 and 2. Where, 0 or 1 represents the switch in the lower side or the upper side of the leg is turned-on, respectively. Table 1 summarizes the phase voltages for Y-connected motors operated by B4 inverters. Where, V_1 or V_2 means the voltage magnitude in the capacitor at the top or the bottom of dc-link. Where phase voltages of Δ-connected motors are listed in Table 2.

B4 inverters have no zero voltage and all 4 voltage vectors are effective vectors. These four switching states are noted as four modes according to switching status. In mode 1(0,0) of Tables 1 and 2, it can be known that only the bottom capacitor is involved in the power transfer to motors, and in mode 4(1,1) only the top capacitor transfers power to the motor. Depending on the mode, the capacitor transferring power to the motor is changed, so that the power flow in and out of this neutral point of dc-link causes voltage difference between the upper and lower capacitors.

Table 1. Phase voltages in Y-connection

mode	S_1	S_3	V_{as}	V_{bs}	V_{cs}
1	0	0	$-\frac{1}{3}V_2$	$-\frac{1}{3}V_2$	$\frac{2}{3}V_2$
2	0	1	$-\frac{1}{3}(2V_2+V_1)$	$\frac{1}{3}(2V_2+V_1)$	$\frac{1}{3}(V_2-V_1)$
3	1	0	$\frac{1}{3}(2V_1+V_2)$	$-\frac{1}{3}(2V_2+V_1)$	$\frac{1}{3}(V_2-V_1)$
4	1	1	$\frac{1}{3}V_1$	$\frac{1}{3}V_1$	$-\frac{2}{3}V_1$

Table 2. Phase voltages in Δ-connection

mode	V_{ab} (V_{as})	V_{bc} (V_{bs})	V_{ca} (V_{cs})
1	0	$-V_2$	V_2
2	$-V_1-V_2$	V_1	V_2
3	V_1+V_2	$-V_2$	$-V_1$
4	0	V_1	$-V_1$

2.2 Voltage distortion in B4 inverters

With alignment of the real axis to $u_1(0,0)$ vector, the real and imaginary voltage components for the Y and Δ-connected motors can be obtained as Table 3. From Table 3, it can be known that each voltage component of Δ-connection is $\sqrt{3}$ times bigger than that for Y-connection, and it has 30^O angle difference as shown in Fig. 3.

Fig. 3 shows effective vectors from B4 inverters for Y and Δ-connected motors, and it is assumed that $V_1 = V_2$, which is an ideal case and under this situation four vectors of B4 inverters are perpendicular each other.

Table 3. Real and imaginary components for each connection

	mode	Y-connection		Δ-connection	
		Re.	***Im.***	***Re.***	***Im.***
u_1	*1*	V_2	0	$\sqrt{3}V_2$	0
u_4	*2*	$\frac{1}{2}(V_2-V_1)$	$-\frac{\sqrt{3}}{2}(V_1+V_2)$	$\frac{\sqrt{3}}{2}(V_2-V_1)$	$-\frac{3}{2}(V_1+V_2)$
u_2	*3*	$\frac{1}{2}(V_2-V_1)$	$\frac{\sqrt{3}}{2}(V_1+V_2)$	$\frac{\sqrt{3}}{2}(V_2-V_1)$	$\frac{3}{2}(V_1+V_2)$
u_3	*4*	$-V_1$	0	$-\sqrt{3}V_1$	0

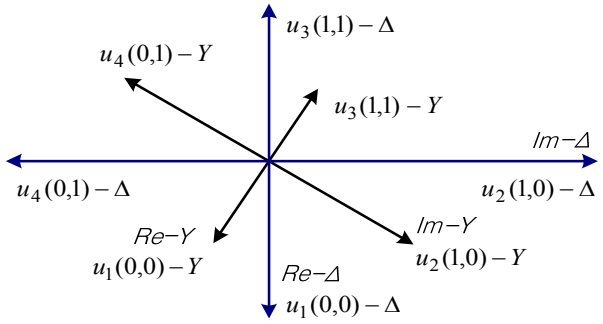


Fig. 3. Four effective voltage vectors with based on u_1 voltage vector for each Y and Δ-connection.

2.3 Proposed current ripple reduction scheme

The voltage distortion in B4 inverters due to the discrepancy between V_1 and V_2 can be known from Fig. 4. In the left side of Fig. 4(a) illustrates four effective voltage vectors when $V_1=V_2$, and that under the condition $V_2>V_1$ is shown at the right side. The voltage vectors that are orthogonal each other when $V_2=V_1$ are tilled to the right if $V_2>V_1$.

As shown in Table 3, u_1 becomes bigger than u_3 if $V_2>V_1$.

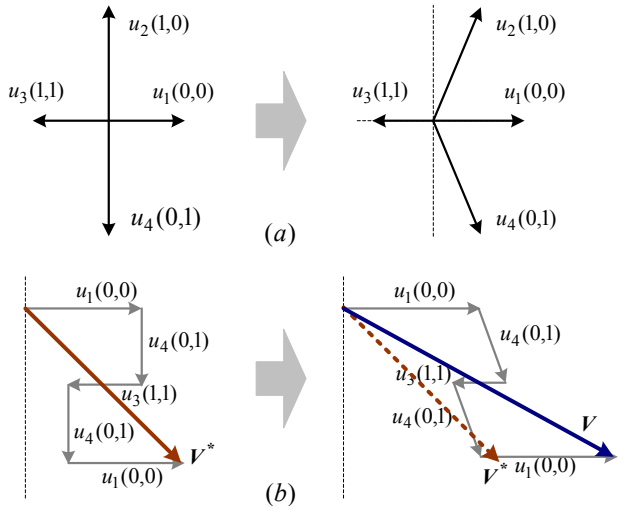


Fig. 4. (a) Voltage vectors for the ideal case(left) and that for $V_2>V_1$ (right), and (b) reference voltage(left) and developed vector affected by the dc-link voltage variation (right).

Table 3 also shows that real voltage components are zero if $V_1=V_2$, but they are positive values for $V_2>V_1$. If T_a and T_b calculated by (1) or (2) applied without modification, it results in the voltage vector slanted to the right compared to the reference voltage obtained under the condition $V_1=V_2$ as illustrated in Fig. 4(b).

As noted previously, real and imaginary components for Y and Δ-connection shown in Table 3 has the same form with different scale. Even severity of the voltage distortion depends on $|V_1-V_2|$, the tendency that slanted to the right when $V_2>V_1$ or toward to the left if $V_1>V_2$ is identical regardless of connection types. Therefore, the current ripple reduction method can be applied to both connection types (Y and Δ) in the same way.

The proposed current ripple reduction method can be explained as follows. From Fig. 4(b), it can be known that in order to reduce voltage error, switching time for making the voltage vector tilted to the right should be shortened and that for the left direction should be lengthen. In case of $V_1> V_2$, the duration time for u_1 should be decreased and that for u_3 should be increased.

Fig. 5 shows the switching times and corresponding voltage vectors, which are located in region I or II, by the center aligned PWM method. Where, t_x denotes the duration time for u_x such as t_1 time for u_1 vector and t_3 for u_3, and T_s is the sampling time. Region I is the first and second quadrants, and equivalent to the condition of $T_a>T_b$. One the other hand, region II is the third and fourth quadrants, and the voltage vector in that region has the switching time of $T_b>T_a$. As shown in (1) and (2), only T_a and T_b are involved, so that the vector duration time such as t_1 and t_3 are required to be calculated by using already determined values of T_s, T_a, and T_b for implementation. In region I, from Fig. 5(a) it can be known that $t_1=T_s-T_a$, and $t_3=T_b$, Where, in region II $t_1=T_s-T_b$, and $t_3=T_a$.

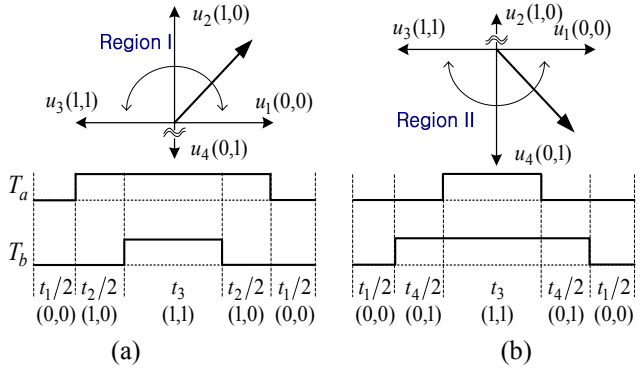


Fig. 5. Determination of region by using the magnitude of T_a and T_b with voltage vector located in (a) region I and (b) region II.

In order to reduce the voltage error due to V_2>V_1, as previously mentioned, t_3 for u_3 should be increased, and t_1 for u_1 should be decreased. Fig. 5(a) shows that making t_1 longer and t_3 shorten is equivalent to increasing both T_a and T_b. By contrast, in case of V_1>V_2, it is necessary to decrease both T_a and T_b, which is the same as making t_1 larger and t_3 smaller.

The rule for changing switching times in region I can be applied in region II with an identical manner. When V_2>V_1, it is required to increase t_1 and reduce t_3, which is the same as increment of T_a and T_b. Hence, regardless of regions, for current ripple compensation, in case of V_2>V_1, T_a and T_b should be increased, and required to be shorten when V_1>V_2.

In the implementation, the switching time obtained by (1) or (2) is modified with the form of $t+\Delta t$ corresponding to the voltage difference in dc-link capacitors. Where, the region is simply determined by comparing the magnitude of T_a and T_b, i.e. when T_a>T_b, region is I, and if T_b>T_a the voltage vector is located in region II. The compensation time (Δt) consists of V_2–V_1, t_1, t_3, and k. Where, k is the compensation constant. It has nominal value of 1/2 to reflect the impact of the voltage difference equally to the switching time making the generated voltage vector to the right and that to the left. In some noisy environments, this k value can be adjusted to smaller than 1/2 to reduce the effect caused by the detection error in voltage measurement. The voltage distortion is proportional to the voltage difference in dc-link (V_2–V_1), and to compensate the distortion duration times of u_1 and u_3 are utilized. Therefore, compensation time in region I is expressed as (3). Similarly, the amount of compensation in region II can be obtained as (4). Fig. 6 illustrates the flow chart of the proposed compensation scheme.

$$\Delta T_a = k\frac{V_2 - V_1}{V_{dc}} t_1, \Delta T_b = k\frac{V_2 - V_1}{V_{dc}} t_3 \quad (3)$$

$$\Delta T_a = k\frac{V_2 - V_1}{V_{dc}} t_3, \Delta T_b = k\frac{V_2 - V_1}{V_{dc}} t_1 \quad (4)$$

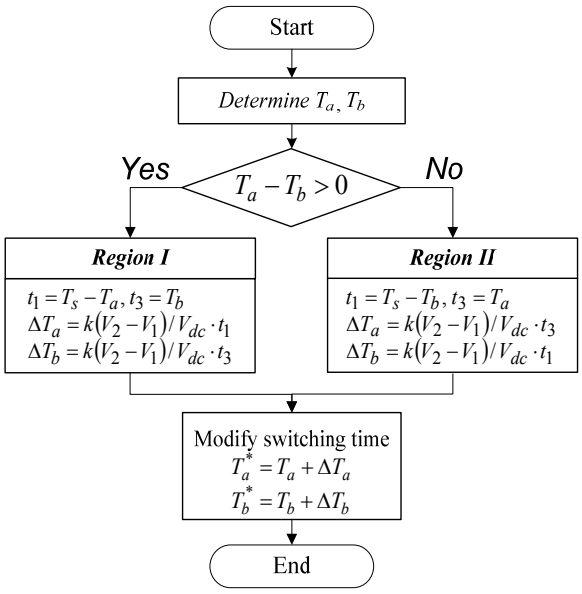


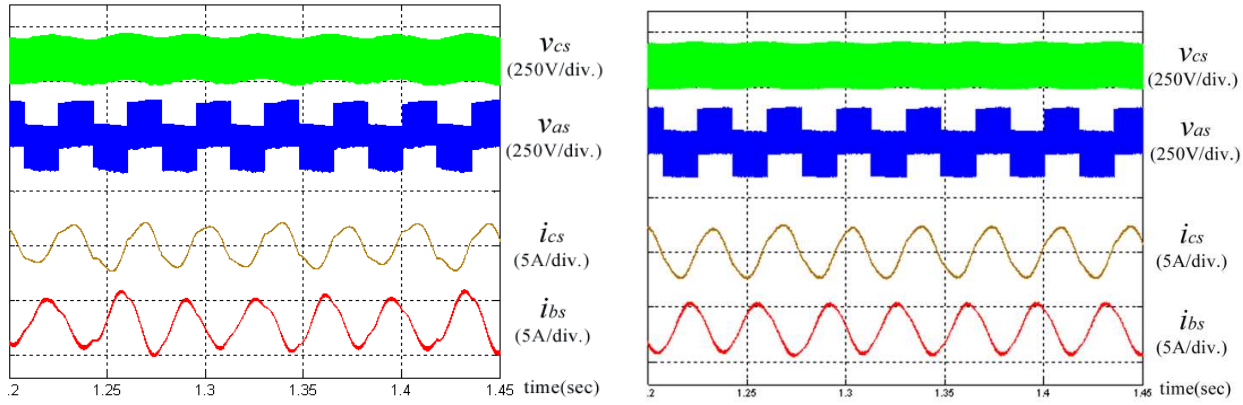
Fig. 6. Flow chart for the proposed method.

3. Verifications

3.1 Simulation results

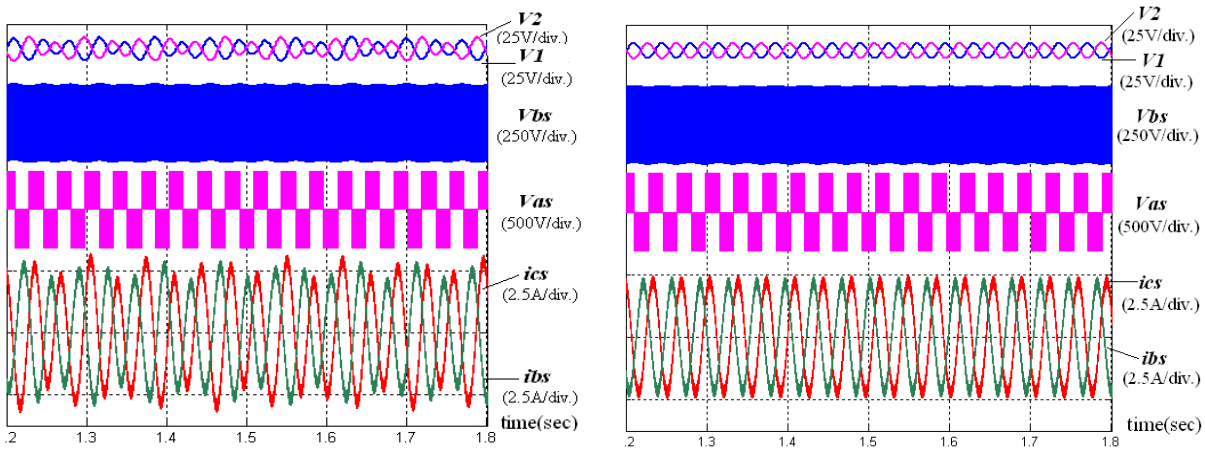
Figs. 7(a), (b) show simulation waveforms carried out by a Y-connected 1-HP induction motor without and with the proposed current ripple reduction method, respectively. In Fig. 7, from top to bottom, C and A-phase voltages and phase currents of C and B-phase are illustrated. Comparing with Figs. 7(a) and 7(b), it is obvious that the proposed method makes phase currents more sinusoidal and reduces the magnitude difference between phase currents. THD of i_{cs} and i_{bs} with 15.31% and 11.23% before compensation has been reduced to 5.91% and 5.09% after the compensation. Figs. 8(a), (b) show simulation results obtained from Δ-connected induction motor. The waveforms in Fig. 8 are V_1&V_2, V_{bs}, V_{as}, i_{cs}, and i_{bs}. The amount of current ripple in Fig. 8(a) without compensation is reduced remarkably by the proposed method as shown in Fig. 8(b). Besides the current ripple reduction, the ripple reduction in the voltages of dc-link capacitors (V_1 and V_2) is observed.

The peak value of the waveforms showing phase voltage in Fig. 8 has the voltage magnitude listed in Table 2. The magnitude of A-phase voltage has -V_1-V_2 in mode 2, and V_1+V_2 in mode 4, otherwise zero voltage so that voltage ripples are not shown in V_{as} of Δ-connected motors. On the other hand, the voltage ripples in V_1 and V_2 are shown in V_{bs} waveforms because the B-phase voltage has the form of V_2 and $-V_1$ corresponding to different mode as listed in Table 2. From Figs. 7 and 8, it can be known that all the phase voltages in Y-connected motors are affected by voltage ripples in V_1 and V_2, but in case of Δ-connection A-phase voltage is not affected by voltage ripples.



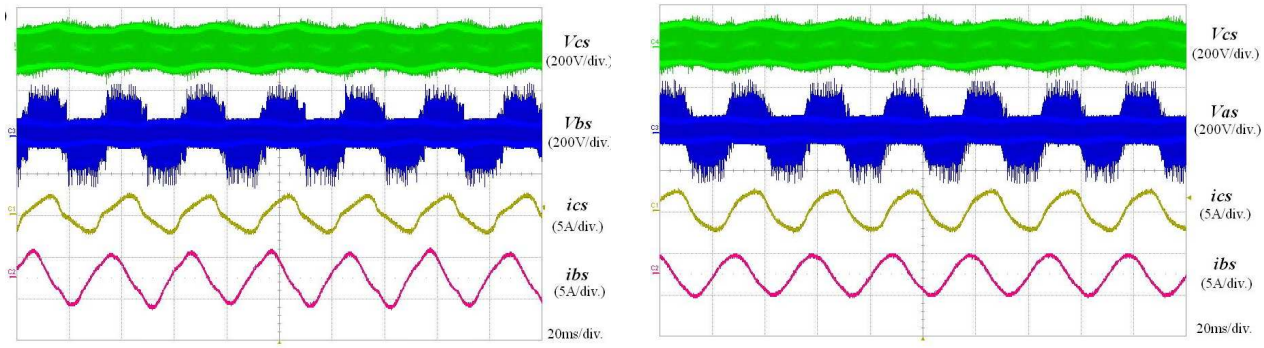
(a) (b)

Fig. 7. Simulation results with Y-connected motors (a) without and (b) with the proposed method.



(a) (b)

Fig. 8. Simulation results with Δ-connected motors (a) without and (b) with the proposed method.



(a) (b)

Fig. 9. Experimental results with Y-connected motors, (a) without and (b) with the proposed method.

3.2 Experimental results

In order to verify the validity of the proposed system, experiments using an induction motor were performed with the same condition of simulations. The proposed algorithm was implemented by TM320F28335 digital signal processor with 8 *kHz* sampling time, and voltage measurements of upper and lower dc-link capacitors. Each capacitor in dc-link has the capacitance of 100μF for Y-connected and 940μF for Δ-connected motors. As shown in Table 2 for Δ-connection, the magnitude of voltage transition between modes is larger than that for Y-connection. In addition, when remaining voltage to frequency ratio (V/F ratio) for

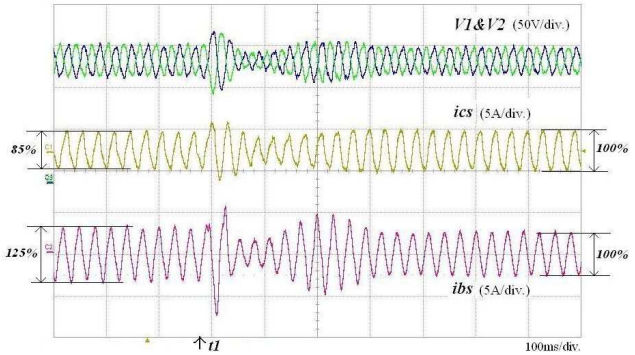
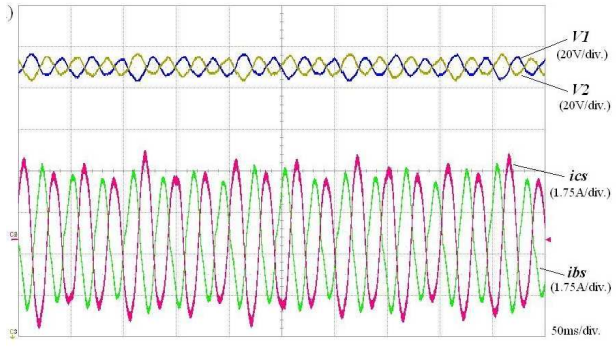
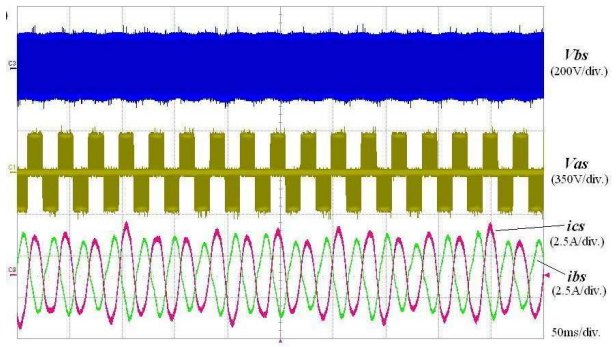


Fig. 10. Experimental results with Y-connected motors applying the compensation algorithm at $t=t_1$



(a)

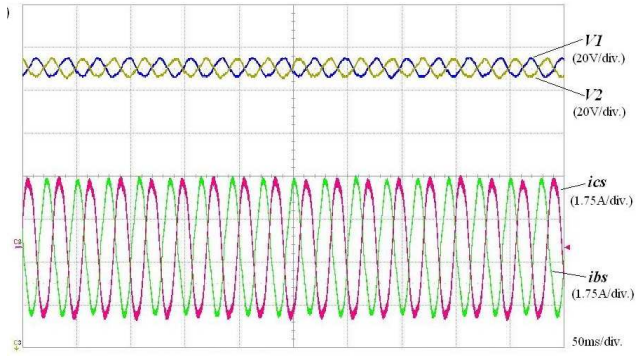


(b)

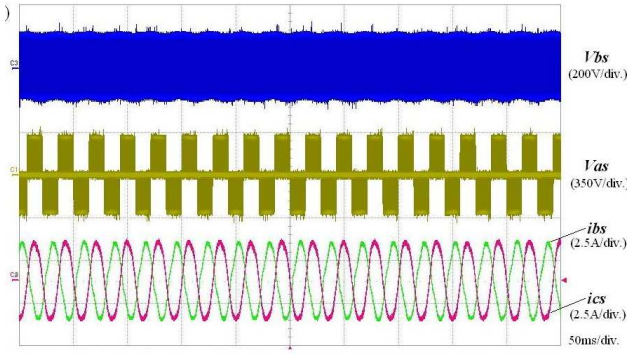
Fig. 11. Experimental results from Δ-connected motors without ripple compensation.

the induction motor constant, the line current for the Δ-connection is $\sqrt{3}$ times larger than that for Y-connection, it results in higher capacitance needed in Δ-connection comparing to Y-connection.

Fig. 9 shows the experimental waveforms for a Y-connected motor. Same as Fig. 7, the current shapes become more sinusoidal, and the magnitude deference between each phase current is reduced by the proposed method. In Fig. 10, the current ripple reduction scheme start working at $t=t_1$. Fig 10 shows that the unbalanced currents as i_{cs} and i_{bs} having 85% and 125% of the nominal values becomes balanced three phase currents after



(a)



(b)

Fig. 12. Experimental results with the proposed compensation method applying for Δ-connected motors.

applying the proposed method. Experimental results for Δ-connected motors without the ripple compensation are shown in Fig. 11. In Fig. 11(a), the measured dc-link voltages and phase currents of B & C phases are illustrated, and measured V_{bs}, V_{as}, and phase currents are shown in Fig. 11(b). It should be noted that the division for V_{bs} is $200V$ whereas V_{as} is $350V$.

It can be seen that the phase voltages of experimental results are the same as Fig. 8 obtained from simulations model. Fig. 12 shows the experimental results carried out with the proposed method. Comparing Fig. 11, it can be known that the proposed method reduces current ripples significantly. The experimental results illustrate the validity of the proposed method for Y and Δ- connection with ripple reduction of phase currents by a simple modification of switching time.

4. Conclusion

In this paper, the simple current ripple compensation method employing simple calculation and decision process for B4 inverter has been proposed. The voltage distortion phenomenon caused by the voltage difference between the dc-link capacitors was analyzed. In order to do simulation for Y as well as Δ-connected motors analytic models based

on differential equations were developed. The compensation method based on modification of switching time was applied to both connection types. The simulation and experimental results applied in an induction motor with Y and Δ-connection have verified the control performance and the validity of the proposed method.

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Dong-Myung Lee He received his B.S. and M.S. in Electrical Engineering from Hanyang University, Seoul, Korea, in 1994 and 1996, respectively, and his Ph.D. in Electrical and Computer Engineering from the Georgia Institute of Technology, Atlanta, Georgia, USA, in 2004. From 1996 to 2000, He worked for LG Electronics Inc., Seoul, Korea. From 2004 to 2007, he was employed by the Samsung SDI R&D Center, Yongin, Korea, as a Senior Engineer. From 2007 to 2008, he was with the Department of Electrical Engineering, Hanyang University, as a Research Professor. Since 2008, he has been an Associate Professor with the School of Electronic and Electrical Engineering, Hongik University, Seoul, Korea. He was a visiting scholar of Texas A&M University in 2012. His current research interests include variable speed drives, power quality compensation devices, and power conversion systems for renewable energy sources.

Jae-Bum Park He received the B.Sc degree in electrical engineering in 2002 and the M.Sc degree in Electrical Engineering from the ECL(Energy Conversion Laboratory) at Hanyang University, Seoul, Korea in 2005. His M.Sc thesis topic was "Single-Phase Switched Reluctance Motor Optimum

Design Using Response Surface Methodology and Finite Element Method". During his time as a graduate student, he completed an internship which focused on a control system of PM Linear machines for the baggage claim at Nuremberg Airport with SIEMENS AG in Erlangen, Germany. Then he joined Motor Lab. in LG Components R&D Center, Korea as a research engineer in 2004. He has worked on machine design and control drives for ODD and EV applications. In August 2010, he began working towards a Ph.D in electrical engineering at Texas A&M University and He is associated with the EMPE(Electrical Machines & Power Electronics) Laboratory working with Dr. Hamid A. Toliyat. Jae-Bum's research interests include machine design (such as IPM, SPM, PMa-SynRM, SRM, IM, and BF-SRM) and DSP based control drives (power converters & inverters) for HEV and EV applications. He is currently working on multi-phase PMSM & BF-SRM design for green car applications and inverter circuit for 6MW PMSM and 3kW PMa-SynRM.

Hamid A. Toliyat He received the B.S, degree from Sharif University of Technology, Tehran, Iran in 1982, the M.S. degree from West Virginia University, Morgantown, WV in 1986, and the Ph.D. degree from University of Wisconsin-Madison, Madison, WI in 1991, all in electrical engineering. Following receipt of the Ph.D. degree, he joined the faculty of Ferdowsi University of Mashhad, Mashhad, Iran as an Assistant Professor of Electrical Engineering. In March 1994 he joined the Department of Electrical and Computer Engineering, Texas A&M University where he is currently Raytheon endowed professor of electrical engineering.

Dr. Toliyat has received the prestigious CyrillVeinott Award in Electromechanical Energy Conversion from the IEEE Power Engineering Society in 2004, Patent and Innovation Award from Texas A&M University System Office of Technology Commercialization's in 2007, TEES Faculty Fellow Award in 2006, Distinguished Teaching Award in 2003, E.D. Brockett Professorship Award in 2002, Eugene Webb Faculty Fellow Award in 2000, and Texas A&M Select Young Investigator Award in 1999. He has also received the Space Act Award from NASA in 1999, and the Schlumberger Foundation Technical Awards in 2001 and 2000.

Dr. Toliyat was an Editor of IEEE Transactions on Energy Conversion. He was Chair of the IEEE-IAS Industrial Power Conversion Systems Department of IEEE-IAS, and is a member of Sigma Xi. He is a fellow of the IEEE, the recipient of the 2008 Industrial Electronics Society Electric Machines Committee Second Best Paper Awardas well as the recipient of the IEEE Power Engineering Society Prize Paper Awards in 1996 and 2006 and the 2006 IEEE Industry Applications Society Transactions Third Prize Paper Award. His main research interests and experience include analysis and design of electrical machines, variable speed drives for traction and propulsion applications, fault diagnosis of electric machinery, and sensorless variable speed drives. Prof. Toliyat has supervised more than 50 graduate students, published over 385 technical papers (over 115 papers are in IEEE Transactions), presented more than 80 invited lectures all over the world, and has 13 issued and pending US patents. He is the author of DSP-Based Electromechanical Motion Control, CRC Press, 2003, the co-editor of Handbook of Electric Motors - 2nd Edition, Marcel Dekker, 2004, and the co-author of Electric Machines – Modeling, Condition Monitoring, and Fault Diagnosis, CRC Press, Florida, 2013.

He was the General Chair of the 2005 IEEE International Electric Machines and Drives Conference in San Antonio, Texas. Dr. Toliyat is a Professional Engineer in the State of Texas.