

Full-Range Analytic Drain Current Model for Depletion-Mode Long-Channel Surrounding-Gate Nanowire Field-Effect Transistor

Yun Seop Yu

Abstract—A full-range analytic drain current model for depletion-mode long-channel surrounding-gate nanowire field-effect transistor (SGNWFET) is proposed. The model is derived from the solution of the 1-D cylindrical Poisson equation which includes dopant and mobile charges, by using the Pao-Sah gradual channel approximation and the full-depletion approximation. The proposed model captures the phenomenon of the bulk conduction mechanism in all regions of device operation (subthreshold, linear, and saturation regions). It has been shown that the continuous model is in complete agreement with the numerical simulations.

Index Terms—Silicon nanowire, depletion-mode, accumulation charge, full-depletion approximation

I. INTRODUCTION

Recently, extensive studies of semiconducting nanowire field-effect transistor (NWFET) device physics and transport mechanism have been performed [1-5]. These transistors have demonstrated promising field-effect transistor (FET) characteristics in top-gate [6, 7], bottom-gate [8], and surround-gate [9, 10] FET geometries. Most NWFETs operate in accumulation or depletion modes [6-11]. Among these, the surrounding-gate NWFET (SGNWFET) allows a best control of the

channel charge in the nanowire channel [11]. Due to the interest in this device, simple compact models of the SGMOSFETs will be needed for efficient circuit simulation. Only a compact model of depletion-mode surrounding-gate NWFET (SGNWFET) has been developed by us so far [12]. However, our SGNWFET model [12] has convergence problems by using the piecewise approach. Therefore, it is required to develop the SGNWFET model that can continuously cover every operation region.

In this paper, we will present a full-range drain current model for depletion-mode long-channel n-type SGNWFET for efficient circuit simulation. The model is derived from the solution of the 1-D cylindrical Poisson equation including dopant and mobile charges, by using the Pao-Sah gradual channel approximation and the full-depletion approximation. To verify the validity of our model, its results are compared with the 3-dimensional (3D) device simulation results of SGNWFET.

II. MODEL FORMATION

1. Intrinsic Channel Current Model

Fig. 1 shows a three-dimensional schematic diagram and cross-section in substrate direction at the location y in an n-type cylindrical SGNWFET channel. The nanowire is a semiconductor doped with n-type impurities. The metals for ohmic contacts of the drain and source are used, and a metal of the surrounding-gate contacts to modulate the nanowire channel are used. Here, R , L , and N_d are the radius, length, and n-type doping

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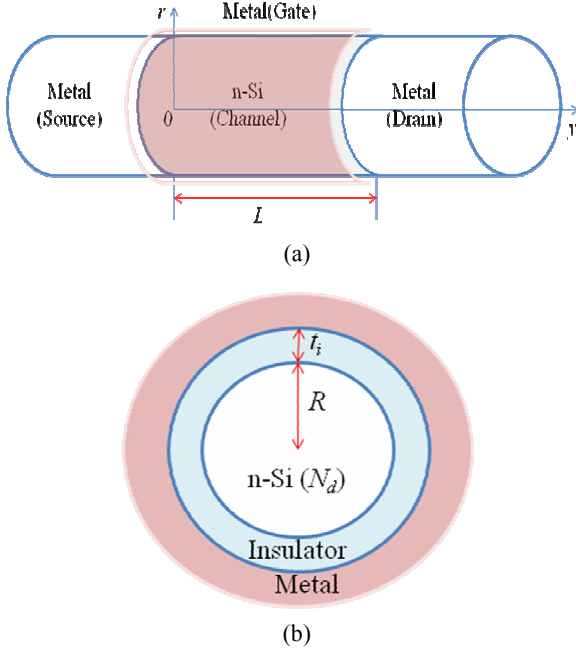


Fig. 1. (a) 3-D schematic diagram, (b) cross-section of a cylindrical n-type SGNWFET channel. Device parameters are indicated.

concentration of the nanowire, respectively, and t_i is the insulator thickness.

The conduction mechanism for depletion-mode SGNWFET is explained as follows [12]. When $V_g < V_{TH}$, the channel is fully depleted, and the device is under a subthreshold regime. Here V_g and V_{TH} are the gate voltage and the threshold voltage, respectively. When $V_{TH} < V_g < V_{FB}$, the channel is partially depleted, and the current can flow through the center of the channel by the bulk conduction mechanism (volume inversion). Here V_{FB} is the flat-band voltage. When $V_g = V_{FB}$, a completely neutral channel is created, and the current can flow through the entire channel. When $V_g > V_{FB}$, the mobile carrier (electron) density is increased at the surfaces, and the current conduction is governed by the mobile carriers that accumulate at the surface in channel (surface accumulation). This way, in the linear and subthreshold regions, the current mechanism for depletion-mode SGNWFET is primarily composed of the bulk current.

In a doped SGNWFET, in the normal operating regimes, the minority carrier concentration (holes) is negligible in comparison with the electron carrier concentration, and by using the gradual channel approximation, the standard cylindrical coordinate formulation of the Poisson's equation in the doped n-type

SGNWFET is represented as

$$\frac{d^2}{dr^2} \phi + \frac{1}{r} \frac{d}{dr} \phi = -\frac{qN_d}{\epsilon_{si}} \{1 - \exp[\beta(\phi - V_{ch})]\}, \quad (1)$$

where ϕ is the electrostatic channel potential, ϵ_{si} is the silicon dielectric constant, r is the cylindrical coordinate along the radius direction, V_{ch} is the electron quasi-Fermi potential, q is the electronic charge, and $\beta = q/kT$ is the inverse of the thermal voltage with the Boltzman constant k and the temperature T . Eq. (1) must satisfy the following boundary conditions:

$$\left. \frac{d\phi}{dr} \right|_{r=0} = 0, \quad \phi|_{r=R} = \phi_s, \quad \phi|_{r=0} = \phi_0, \quad (2)$$

where ϕ_s and ϕ_0 are the surface potential and the center potential, respectively. Multiplying both sides of Eq. (1) by r and integrating from $r = 0$ to r , Eq. (1) can be rearranged as

$$\frac{d\phi}{dr} = -\frac{qN_d r}{2\epsilon_{si}} + \frac{qN_d}{r\epsilon_{si}} \int_0^r \exp[\beta(\phi - V_{ch})] \cdot r \cdot dr. \quad (3)$$

The first and second terms of the right-hand side in Eq. (3) mean the depletion charge and the mobile charge, respectively. There is no analytical solution for Eq. (3). Using the subthreshold approximation method in [13, 14], $d\phi/dr$ at $r = R$ can be expressed as

$$\begin{aligned} \left. \frac{d\phi}{dr} \right|_{r=R} &= -\frac{Q_{dep}}{\epsilon_{si}} \\ &- \frac{Q_{dep}}{Q_{dep} + Q_m} \frac{2}{\beta R} \exp[\beta(\phi_s - V_{ch})] \cdot \{1 - \exp[\beta(\phi_0 - \phi_s)]\}. \end{aligned} \quad (4)$$

where $Q_{dep} = qN_d R/2$ is the depletion charge density per unit gate area and Q_m is the mobile charge density per unit gate area. Using Eq. (4), Gauss's law can be represented as

$$\begin{aligned} Q_{tot} = Q_{dep} + Q_m &= -\epsilon_{si} \left. \frac{d\phi}{dr} \right|_{r=R} \\ &= Q_{dep} + \frac{Q_{dep}}{Q_{dep} + Q_m} \frac{2\epsilon_{si}}{\beta R} \exp[\beta(\phi_s - V_{ch})] \cdot \{1 - \exp[\beta(\phi_0 - \phi_s)]\}. \end{aligned} \quad (5)$$

From Eq. (5), Q_m can be expressed as

$$Q_m = \frac{Q_{dep}}{Q_{dep} + Q_m} \frac{2\epsilon_{si}}{\beta R} \exp[\beta(\phi_s - V_{ch})] \cdot \{1 - \exp[\beta(\phi_0 - \phi_s)]\}. \quad (6)$$

Taking the logarithm of Eq. (6) gives a charge-based solution of for the SGNWFET as

$$\begin{aligned} \beta\phi_s = & \beta V_{ch} + \ln \frac{\beta R}{2\epsilon_{si}} - \ln\{1 - \exp[\beta(\phi_0 - \phi_s)]\} \\ & + \ln Q_m + \ln \left(1 + \frac{Q_m}{Q_{dep}}\right), \end{aligned} \quad (7)$$

Under the full depletion approximation in n-type Si, the channel potential can be expressed as

$$\phi(r) = \phi_0 - \frac{qN_d r^2}{4\epsilon_{si}}. \quad (8)$$

In this condition, $\phi_0 - \phi_s = qN_d R^2 / 4\epsilon_{si} = RQ_{dep} / 2\epsilon_{si}$ and it can be applied to Eq. (7), and then Eq. (7) can be rearranged as

$$\begin{aligned} \phi_s = & V_{ch} + \frac{1}{\beta} \ln \frac{\beta R}{2\epsilon_{si}} - \frac{1}{\beta} \ln \left[1 - \exp\left(\frac{\beta R Q_{dep}}{2\epsilon_{si}}\right)\right] \\ & + \frac{1}{\beta} \ln Q_m + \frac{1}{\beta} \ln \left(1 + H \frac{\beta Q_m}{C_i}\right). \end{aligned} \quad (9)$$

where H reflects the impact of geometry and doping on subthreshold region of the SGNWFET ($= C_i / \beta Q_{dep}$ in the subthreshold region), and $C_i = \epsilon_i / (R \ln(1 + t_i / R))$ is the capacitance of silicon which ϵ_i is the insulator dielectric constant [13]. The expression for an H factor has to be modified to cover the full operation region including the accumulation region [13].

The total charge in the channel can be obtained by $Q_{total} = Q_m + Q_{dep}$, and the charge conservation equation can be written as

$$C_i (V_{GS} - \Delta\phi - \phi_s) = Q_{total} = Q_{dep} + Q_m, \quad (10)$$

where V_{GS} is the gate-source bias, $\Delta\phi$ is the work function difference. Substituting Eq. (9) into Eq. (10), Eq. (10) can be rearranged as

$$V_{GS} - V_{th} - V_{ch} = -\frac{Q_m}{C_i} + \frac{1}{\beta} \ln Q_m + \frac{1}{\beta} \ln \left(1 + H \frac{\beta Q_m}{C_i}\right), \quad (11)$$

$$\begin{aligned} V_{th} = & V_{th0} + \Delta V_{th} \\ = & \Delta\phi - \frac{Q_{dep}}{C_i} - \frac{1}{\beta} \ln \frac{2\epsilon_{si}}{\beta R} - \frac{1}{\beta} \ln \left[1 - \exp\left(\frac{\beta R Q_{dep}}{2\epsilon_{si}}\right)\right], \end{aligned} \quad (12)$$

$$\begin{aligned} V_{th0} = & \Delta\phi - \frac{Q_{dep}}{C_i} - \frac{1}{\beta} \ln \frac{4\epsilon_{si} Q_{dep}}{\beta R}, \\ \Delta V_{th} = & -\frac{1}{\beta} \ln \left\{ \frac{1}{2Q_{dep}} \left[1 - \exp\left(\frac{\beta R Q_{dep}}{2\epsilon_{si}}\right)\right] \right\}. \end{aligned} \quad (13)$$

To make Eq. (11) be similar to the charge-control equation developed by Iñiguez *et al.* [15], Eq. (11) can be arranged as

$$V_{GS} - V_{th} - V_{ch} = -\frac{Q_m}{C_i} + \frac{1}{\beta} \ln \left(Q_m + \frac{Q_m^2}{Q_0}\right), \quad (14)$$

where $Q_0 = C_i \beta H$. It leads to a revised and physical-based solution of H factor as [13]

$$H = \frac{C_i}{\beta} \exp(-\beta \Delta V_{th}) = \frac{C_i}{\beta} \left\{ \frac{1}{2Q_{dep}} \left[1 - \exp\left(\frac{\beta R Q_{dep}}{2\epsilon_{si}}\right)\right] \right\}. \quad (15)$$

Using Eq. (14), Q_0 can be expressed as

$$Q_0 = \frac{2Q_{dep}}{1 - \exp\left(\frac{\beta R Q_{dep}}{2\epsilon_{si}}\right)}. \quad (16)$$

Eq. (14) can be solved by the numerical Newton-Raphson iterative method.

Along the channel y direction, the quasi-Fermi-potential V_{ch} varies from the source to the drain. The functional dependence of $V_{ch}(y)$ and $Q_m(y)$ is determined by the current continuity equation, which requires the following drift-diffusion current independent of V_{ch} or y .

$$I_{DS} = \mu_{eff} (2\pi R) Q_m \frac{dV_{ch}}{dy} = \text{constant}, \quad (17)$$

where μ_{eff} is the effective electron mobility. Integrating

$I_{DS}dy$ from the source to drain, the drain current can be represented as [15]

$$I_{DS} = \mu_{eff} \frac{2\pi R}{L} \int_0^{V_{DS}} Q_m(V_{ch}) dV_{ch}. \quad (18)$$

Here, the source in the device is grounded, and the voltage V_{DS} is applied to the drain. To obtain an expression of in terms of the carrier charge densities, from Eq. (14) we obtain the following relation:

$$dV_{ch} = -\frac{1}{\beta} \frac{dQ_m}{Q_m} - \frac{1}{\beta} \frac{1}{Q_0 + Q_m} dQ_m + \frac{dQ_m}{C_i}. \quad (19)$$

Integrating Eq. (18) using Eq. (19), between Q_{ms} and Q_{md} ($Q_{ms} = Q_m$ at the source end and $Q_{md} = Q_m$ at the drain end), Eq. (18) is represented as

$$I_{DS} = \frac{2\pi\mu_{eff}R}{L} \left[\frac{2}{\beta} (Q_{ms} - Q_{md}) + \frac{Q_{md}^2 - Q_{ms}^2}{2C_{ox}} + \frac{Q_0}{\beta} \ln \left(\frac{Q_{md} + Q_0}{Q_{ms} + Q_0} \right) \right]. \quad (20)$$

To implement the current model of SGNWFET into SmartSpice, it employed Verilog-A language, on the basis of Eq. (20) [16].

III. MODEL VERIFICATIONS

To verify a validity of the proposed model, a 3D numerical simulation using ATLAS [17] was carried out.

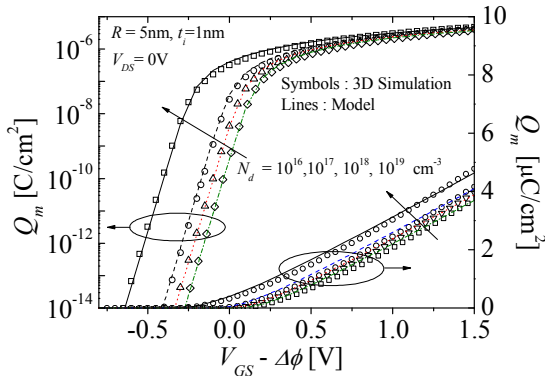
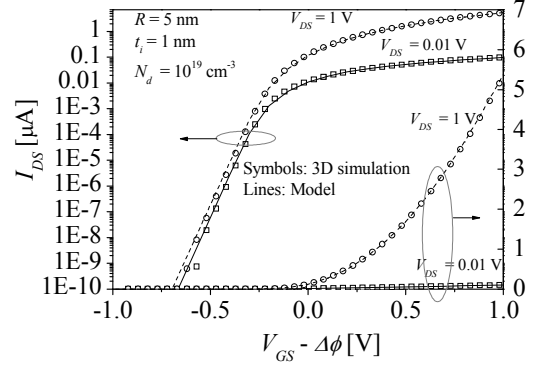
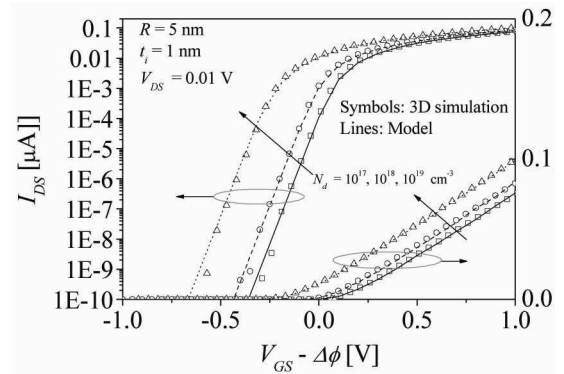


Fig. 2. Linear and logarithm Q_m as a function of V_{GS} of a cylindrical n-type Si SGNWFET for different N_d 's at $V_{DS}=0$ V, $t_i=1$ nm, and $R=5$ nm. Symbols and lines denote the simulation results of 3D device simulator and proposed analytic model, respectively.

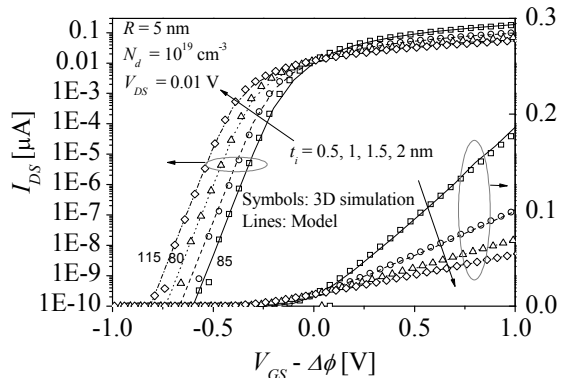
The constant mobility model is employed; $\mu_{eff}=100$ cm^2/Vs . Device parameters used in this study are $R=5$ nm and $L=1$ μm . Fig. 2 shows mobile charge density per unit gate area as function of gate voltage for different doping concentrations. Figs. 3(a)-(c) show the drain current-gate voltage ($I_{DS}-V_{GS}$) characteristics of a cylindrical n-type Si



(a)



(b)



(c)

Fig. 3. Linear and logarithm $I_{DS}-V_{GS}$ characteristics of a cylindrical n-type Si SGNWFET as a function of (a) V_{DS} at $N_d = 10^{19}$ cm^{-3} , (b) N_d at $V_{DS}=0.01$ V, (c) t_i at $V_{DS}=0.01$ V and $N_d=10^{19}$ cm^{-3} . Symbols and lines denote the simulation results of 3D device simulator and proposed analytic model, respectively.

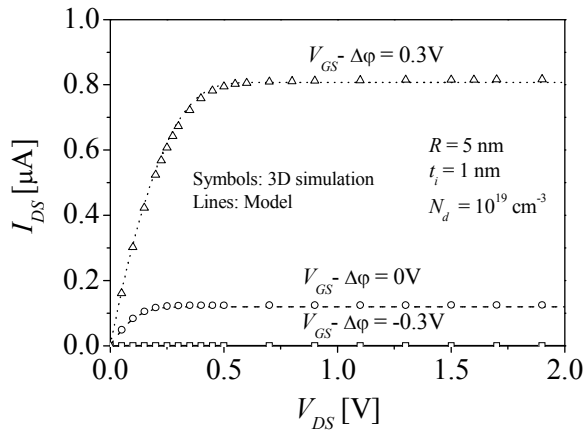


Fig. 4. I_{DS} - V_{DS} characteristics of a cylindrical n-type Si SGNWFET for different V_{GS} 's at $N_d=10^{19}$ cm⁻³ and $t_i=1$ nm. Symbols and lines denote the simulation results of 3D device simulator and proposed analytic model, respectively.

SGNWFET for the different drain voltages, doping concentrations, and insulator thickness, respectively. Fig. 4 shows the drain current-drain voltage (I_{DS} - V_{DS}) characteristics of a cylindrical n-type Si SGNWFET for the different gate voltages. Symbols and lines denote the simulation results of 3D device simulator and proposed analytic SGNWFET model, respectively. The results simulated from the proposed analytic SGNWFET model reproduce those simulated from 3D device simulator considerably well. Further, it continuously predicts the characteristics of SGNWFETs in all regions of operation (subthreshold, linear, and saturation regions).

IV. CONCLUSIONS

We have introduced a compact model for depletion-mode n-type SGNWFET. The model was derived from the solution of the 1-D cylindrical Poisson equation which includes dopant and mobile charges, by using the Pao-Sah gradual channel approximation and the full-depletion approximation. The results simulated from the proposed SGNWFET model reproduced the 3D simulation results considerably well. Thus, the proposed model captured all current conduction mechanisms of the SGNWFET in all regions of device operation (subthreshold, linear, and saturation regions). In order to improve the proposed model, further physical effects such as quantum mechanical effects, short-channel effects, field dependence mobility, and parasitic resistance effects should be added.

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REFERENCES

- [1] H. Yan, H. S. Choe, S. W. Nam, Y. Hu, S. Das, J. F. Klemic, J. C. Ellenbogen, and C. M. Lieber, "Programmable nanowire circuits for nanoprocessors," *Nature*, Vol. 470, pp. 240-244, 2011.
- [2] N. Clément, K. Nishiguchi, J. F. Dufreche, D. Guerin, A. Fujiwara, and D. Vuillaume, "A silicon nanowire ion-sensitive field-effect transistor with elementary charge sensitivity," *Appl. Phys. Lett.* Vol. 98, pp. 014104, 2011.
- [3] A. Gao, N. Lu, P. Dai, T. Li, H. Pei, X. Gao, Y. Gong, Y. Wang, and C. Fan, "Silicon-Nanowire-Based CMOS-Compatible Field-Effect Transistor Nanosensors for Ultrasensitive Electrical Detection of Nucleic Acids," *Nano Lett.* Vol. 11, pp. 3974-3978, 2011.
- [4] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science*, Vol. 294, pp. 1313-1317, 2001.
- [5] Z. Zhong, D. Wang, Y. Cui, M. W. Bockrath, and C. M. Lieber, "Nanowire Crossbar Arrays as Address Decoders for Integrated Nanosystems," *Science*, Vol. 302, pp. 1377-1379, 2003.
- [6] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature*, Vol. 441, pp. 489-483, 2006.
- [7] H. Jung, "The analysis of breakdown voltage for the double-gate MOSFET using the Gaussian doping distribution," *Journal of Information and Communication Convergence Engineering*, Vol. 10, pp. 200-204, 2012.
- [8] T. L. Wade, X. Hoffer, A. D. Mohammed, J.-F. Dayen, D. Pribat, and J.-E. Wegrowe, "Nanoporous alumina wire templates for surrounding-gate nanowire transistors," *Nanotechnology*, Vol. 18, pp. 125201, 2007.
- [9] V. Schmidt, H. Riel, S. Senz, S. Karg, W. Riess,

and U. Gesele, "Realization of a silicon nanowire vertical surround-gate field-effect transistor," *Small*, Vol. 2, pp. 85-88, 2006.

- [10] <http://www.itrs.net/reports.html>: International Technology Roadmap for Semiconductors, 2011.
- [11] Y. S. Yu and H. K. Park, "Analytic modeling of a depletion-mode cylindrical surrounding-gate nanowire field-effect transistor," *J. Nanoscience Nanotechnology* Vo, 12, pp. 10809-10812, 2011; Y. S. Yu, in *proceeding of Nano Korea 2011*, pp. P1107_002, 2011.
- [12] F. Liu, J. He, L. Zhang, J. Zhang, J. Hu, C. Ma, and M. Chan, "A Charge-Based Model for Long-Channel Cylindrical Surrounding-Gate MOSFETs from Intrinsic Channel to Heavily Doped Body," *IEEE Trans. Electron Devices*, Vol. 55, pp. 2187-2194, 2008.
- [13] Y. S. Yu, N. Cho, S. W. Hwang, D. Ahn, "Implicit Continuous Current-Voltage Model for Surrounding-Gate Metal-Oxide-Semiconductor Field-Effect Transistors (SGMOSFETs) Including Interface Traps," *IEEE Trans. Electron Devices*, Vol. 58, pp. 2520-2524, 2011.
- [14] B. Iñíguez, D. Jiménez, J. Roig, H. A. Hamid, L. F. Marsal, and J. Pallarès, "Explicit continuous model for long-channel undoped surrounding gate MOSFETs," *IEEE Trans. Electron Devices*, Vol. 52, pp. 1868-1873, 2005.
- [15] SILVACO, Inc. SMARTSPICE Users' Manual. (2012). [Online]. Available: <http://www.silvaco.com>.
- [16] ATLAS ver. 5.18.3. R Manual, Silvaco International, Santa Clara, CA (2012).



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