Gate-to-Drain Capacitance Dependent Model for Noise Performance Evaluation of InAlAs/InGaAs Double-gate HEMT

Monika Bhattacharya[*], Jyotika Jogi[**], R. S. Gupta[***], and Mridula Gupta[*]

Abstract—**In the present work, the effect of the gate-to-drain capacitance (C_{gd}) on the noise performance of a symmetric tied-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ double-gate HEMT is studied using an accurate charge control based approach. An analytical expression for the gate-to-drain capacitance is obtained. In terms of the intrinsic noise sources and the admittance parameters (Y_{11} and Y_{21} which are obtained incorporating the effect of C_{gd}), the various noise performance parameters including the Minimum noise figure and the Minimum Noise Temperature are evaluated. The inclusion of gate-to-drain capacitance is observed to cause significant reduction in the Minimum Noise figure and Minimum Noise Temperature especially at low values of drain voltage, thereby, predicting better noise performance for the device.**

Index Terms—**Double-gate, HEMT, gate-to-drain capacitance, InAlAs/InGaAs, noise, minimum noise figure**

Manuscript received Jul. 13, 2012; accepted Mar. 26, 2013

[*] Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus
[**] Department of Electronic Science, A.R.S.D. College, University of Delhi, South Campus, New Delhi-110021, India
[***] Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, Sector-22, Rohini, New Delhi-110086, India
E-mail : mridula@south.du.ac.in

I. INTRODUCTION

InAlAs/InGaAs double-gate HEMTs have proved to be the most promising candidates for the future ultra-high frequency and low-noise applications with the maximum frequency of oscillation (f_{max}) as high as 286 GHz and the extrinsic Minimum Noise Figure (NF_{min}) as low as 2.1 dB at the operating frequency of 94 GHz reported for the 100 nm gate-length device [1-7]. However, for improving the accuracy of microwave and millimeter-wave circuit design, a comprehensive and accurate active device model is imperative. The authors in their recent work proposed a charge control model based on Pucel's noise theory [8-10] for the noise performance evaluation of a symmetric tied-gate InAlAs/InGaAs double-gate HEMT [11]. Superior noise performance was observed for the DG-HEMT as compared to the SG-HEMT in terms of lower noise resistance and lower Minimum Noise Figure. The analytical results thereby obtained for the operating frequency of 94 GHz and at a high drain voltage of 0.5V were observed to show good agreement with the ATLAS device simulation results [12] and the earlier reported Monte Carlo simulation and experimental results [1]. In that approach the effect of the gate-to-drain capacitance (C_{gd}) on the noise performance of the device was not taken into account. However, at lower value of drain voltages, i.e., under low field conditions, the gate-drain capacitance exhibits a very high value. Therefore, it can have a very significant effect on the noise performance of the device which must be incorporated in the analytical model for accurate evaluation of Minimum Noise Figure and other noise performance parameters.

In several other analytical noise models also which have been previously developed for the accurate noise performance evaluation, the effect of the gate-to-drain capacitance has been neglected [13, 14]. A noise model proposed by Cappy [15], although includes the effect of C_{gd}, is not suited for device design due to its numerical approach.

In the present work, the effect of gate-to-drain capacitance (C_{gd}) has been incorporated in the analytical model and its effect on the noise performance of the device is investigated. Analytical expression for the gate-to-drain capacitance is obtained. Drain noise coefficient (P), gate-noise coefficient (R) and the correlation coefficient (C) are then evaluated in terms of the intrinsic noise sources and the gate-to-drain capacitance dependent admittance parameters (Y_{11} and Y_{21}). The inclusion of gate-to-drain capacitance in the analytical model is observed to result in improved noise performance of the device in terms of reduced Minimum Noise Figure and Minimum Noise Temperature. However, at the same time, it leads to lower cut-off frequency (f_T).Therefore, while, higher gate-to-drain capacitance leads to improved noise performance, a lower value of C_{gd} is required for a higher cut-off frequency.

II. CHARGE CONTROL MODEL

Fig. 1 shows the schematic of $In_{0.52}Al_{0.48}As$ /$In_{0.53}Ga_{0.47}As$ DG-HEMT. Following the earlier proposed accurate charge control model based on Pucel's noise theory, the channel beneath the gate is divided into two regions: (I) linear region in which the electron velocity is directly proportional to the electric field and (II) saturation region in which the electrons travel with their saturation velocity.

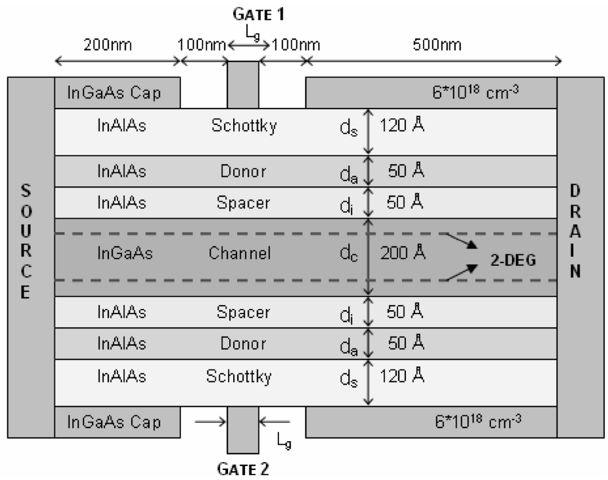

Fig. 1. Schematic of InAlAs/InGaAs DG-HEMT.

Incorporating the variation of fermi potential (E_f) with sheet carrier concentration (n_s) as $E_f = k_1 + k_2\sqrt{n_s} + k_3 n_s$ where, k_1, k_2 and k_3 are the temperature dependent constants whose values are computed as *-0.143 V*, *2.609 x10^{-7} V. cm* and *-5.469x10^{-14} V.cm^2* respectively at 300°K [16], the sheet carrier concentration in a 2DEG is evaluated as:

$$n_s(x) = \frac{\left(\sqrt{k_2^2 + 4k_4\left|V_{off}\right|w} - k_2\right)^2}{4k_4^{\,2}} \tag{1}$$

where $V_{off} = V_{th} + k_1$, $k_4 = k_3 + \frac{qd}{\varepsilon}$ and $w = \frac{V_{gs} - V_{off} - V(x)}{\left|V_{off}\right|}$;

V_{th} is the threshold voltage of the device [11], q= electron charge=*1.6x10^{-19} C*, d=total InAlAs layer thickness=$d_d + d_i$, d_d=d_s + d_a, ε = permittivity of InGaAs = $12.03\varepsilon_o$; ε_o=permittivity of free space=*8.85 x10^{-12} F/m* , V_{gs} is the applied gate-source voltage, $V(x)$ is the potential at any point x along the channel.

Using (1) and piecewise linear velocity field relation, the expression for drain current is obtained as [11]:

$$I_d = \begin{cases} \dfrac{qZ\mu_o}{4k_4^{\,3}L_1}\left[\dfrac{1}{4}(s_1^{\,2} - p_1^{\,2}) - \dfrac{2k_2}{3}(s_1^{\frac{3}{2}} - p_1^{\frac{3}{2}}) + \dfrac{k_2^{\,2}}{2}(s_1 - p_1)\right]; 0 < x < L_1 \\ \dfrac{qZv_{sat}}{2k_4^{\,2}}\left(\sqrt{p_1} - k_2\right)^2 \quad ; L_1 < x < L_g \end{cases} \tag{2}$$

where, $s_1 = k_2^{\,2} + 4k_4\left|V_{off}\right|s$; $s = w(x=0)$, $p_1 = k_2^{\,2} + 4k_4\left|V_{off}\right|p$; $p = w(x = L_1)$, x = L_1 is the point in the channel where the electron velocity saturates, v_{sat} is the saturation velocity *(=2.63 x 10^5 m/s)*, μ_o is the electron mobility *(=0.83 m^2/V.s)*, L_g is the gate-length *(=100 nm)* and Z is the channel width *(=100 μm)*.

The equality of the linear region drain current and saturation region drain current at x=L_1, gives the expression for linear region length as:

$$L_1 = \frac{\mu_o}{2k_4 v_{sat}\left(\sqrt{p_1} - k_2\right)^2}\left\{\frac{1}{4}(s_1^2 - p_1^2) - \frac{2k_2}{3}(s_1^{\frac{3}{2}} - p_1^{\frac{3}{2}}) + \frac{k_2^2}{2}(s_1 - p_1)\right\} \tag{3}$$

and correspondingly saturation region length, $L_2 = L_g - L_1$

This point $x=L_1$ along the channel (at which the critical electrical field is reached) shifts towards the source side ($x=0$) with increase in V_{ds} which in-turn leads to increase in the saturation region length (L_2). Therefore, L_2 increases with increase in drain-source voltage and eventually approaches saturation at high values of V_{ds}. A greater saturation region length leads to higher drain current and transconductance which in turn results in better RF and noise performance in terms of higher cut-off frequency and lower Minimum Noise Figure.

In the previous work [7], the transfer characteristics (I_{ds} vs V_{gs}) of 100 nm gate-length InAlAs/InGaAs single-gate (SG) and symmetric tied-geometry double-gate (DG) HEMT obtained using the analytical model were compared and found to agree well with the experimental measurements reported by *Vasallo et.al.* [2], thereby, proving the validity of the proposed model.

The various small-signal parameters including transconductance (g_m), drain resistance (r_d) and gate-source capacitance (C_{gs}) used in the noise performance characterization of the device are obtained following directly the detailed analysis already given in [11, 17] and are expressed as:

$$g_m = \left.\frac{dI_d}{dV_{gs}}\right|_{V_{ds}} = \frac{2qZv_{sat}}{k_4}\frac{\left(\frac{\sqrt{p_1}-k_2}{\sqrt{p_1}}\right)\left(\left(\sqrt{p_1}-k_2\right)^2 - 2\cosh\left(\frac{\pi L_2}{2d}\right)f(s_1)\right)}{\left(\sqrt{p_1}-k_2\right)^2 - 2\cosh\left(\frac{\pi L_2}{2d}\right)\left[2k_4E_cL_1\left(\frac{\sqrt{p_1}-k_2}{\sqrt{p_1}}\right)+f(p_1)\right]} \tag{4}$$

where $f(s_1) = \frac{s_1}{2} - k_2\sqrt{s_1} + \frac{k_2^2}{2}$ and $f(p_1) = \frac{p_1}{2} - k_2\sqrt{p_1} + \frac{k_2^2}{2}$; $E_c = v_{sat}/\mu_o$ is the critical electric field

$$r_d = \left(\frac{dV_{ds}}{dI_d}\right)_{V_{gs}} = \frac{k_4}{2qZv_{sat}}\left(\frac{\sqrt{p_1}}{\sqrt{p_1}-k_2}\right) \times \left[\frac{2\cosh\left(\frac{\pi L_2}{2d}\right)}{\left(\sqrt{p_1}-k_2\right)^2}\left\{2k_4L_1E_c\left(\frac{\sqrt{p_1}-k_2}{\sqrt{p_1}}\right)+f(p_1)\right\}-1\right] \tag{5}$$

$$C_{gs} = \frac{qZ}{k_4^2E_c}\left[\left\{\frac{f_1(s_1)}{\left(\sqrt{p_1}-k_2\right)^2}+f(s_1)\right\}+ \left(\frac{dp}{ds}\right)_{V_{gd}}\left\{2k_4E_cL_g\left(\frac{\sqrt{p_1}-k_2}{\sqrt{p_1}}\right)-\frac{f_1(p_1)}{\left(\sqrt{p_1}-k_2\right)^2}+f(p_1)\right\}\right] \tag{6}$$

where

$$\left(\frac{dp}{ds}\right)_{V_{gd}} = \frac{-2\cosh\left(\frac{\pi L_2}{2d}\right)f(s_1)}{\left(\sqrt{p_1}-k_2\right)^2 - 2\cosh\left(\frac{\pi L_2}{2d}\right)\left[2k_4E_cL_1\left(\frac{\sqrt{p_1}-k_2}{\sqrt{p_1}}\right)+f(p_1)\right]}$$

$$f_1(s_1) = \frac{s_1^2}{2} - 2k_2s_1^{\frac{3}{2}} + 3k_2^2s_1 - 2k_2^3\sqrt{s_1} + \frac{k_2^4}{2}$$

$$f_1(p_1) = \frac{p_1^2}{2} - 2k_2p_1^{\frac{3}{2}} + 3k_2^2p_1 - 2k_2^3\sqrt{p_1} + \frac{k_2^4}{2}$$

III. INFLUENCE OF GATE-TO-DRAIN CAPACITANCE

The conventional equivalent circuit used for noise performance evaluation [8, 11] is shown with solid lines in Fig. 2, whereas in our present model, an additional gate-to-drain capacitance (C_{gd}), is added, which is denoted by dotted line.

Gate-to-drain Capacitance which is defined as the rate of change of total charge in the 2DEGs with respect to drain-to-source voltage (V_{ds}) when the gate-source voltage (V_{gs}) is constant is expressed as:

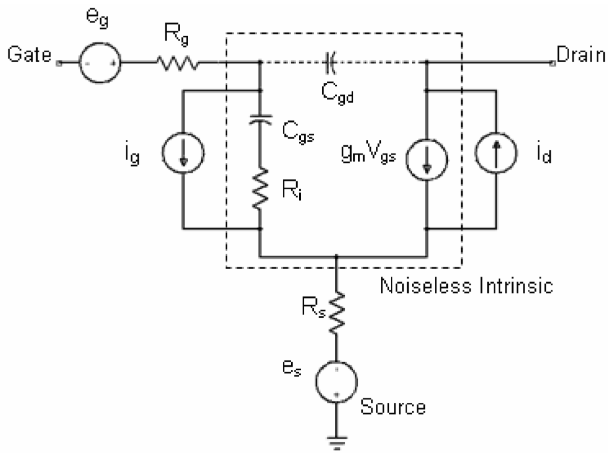

Fig. 2. Equivalent Circuit of symmetric tied-gate InAlAs /InGaAs double-gate HEMT used for Noise Modeling.

$$C_{gd}=\left(\frac{dQ_1}{dV_{ds}}\right)_{V_{gs}}+\left(\frac{dQ_2}{dV_{ds}}\right)_{V_{gs}} \tag{7}$$

where Q_1 is the total charge in the linear region I obtained using (1) as:

$$\begin{aligned}Q_1&=\int_0^{L_1}2qZn_s(x)dx\\&=\frac{q^2Z^2\mu_o}{8k_4^5I_d}\left[\left(\frac{s_1^3-p_1^3}{6}\right)-4k_2\left(\frac{s_1^{5/2}-p_1^{5/2}}{5}\right)+3k_2^2\left(\frac{s_1^2-p_1^2}{2}\right)\right.\\&\left.\qquad-4k_2^3\left(\frac{s_1^{3/2}-p_1^{3/2}}{3}\right)+k_2^4\left(\frac{s_1-p_1}{2}\right)\right]\end{aligned} \tag{8}$$

and Q_2 is the total charge in the saturation region II obtained using (1) as:

$$\begin{aligned}Q_2&=2qZn_s(L_1)L_2\\&=\frac{qZ}{4k_4^3E_c}\left[2k_4E_cL_g\left(\sqrt{p_1}-k_2\right)^2\right.\\&\left.\qquad-\left(\frac{1}{4}(s_1^2-p_1^2)-\frac{2k_2}{3}(s_1^{\frac{3}{2}}-p_1^{\frac{3}{2}})+\frac{k_2^2}{2}(s_1-p_1)\right)\right]\end{aligned} \tag{9}$$

Therefore, substituting (8) and (9) in (7), we obtain the total gate-to-drain capacitance as:

$$\begin{aligned}C_{gd}=\frac{qZ\left|V_{off}\right|}{k_4^2E_c}\left(\frac{dp}{dV_{ds}}\right)_{V_{gs}}&\left[\frac{-f_1(p_1)}{\left(\sqrt{p_1}-k_2\right)^2}\right.\\&\left.+\left\{2k_4E_cL_g\left(\frac{\sqrt{p_1}-k_2}{\sqrt{p_1}}\right)+f(p_1)\right\}\right]\end{aligned} \tag{10}$$

where

$$\left(\frac{dp}{dV_{ds}}\right)_{V_{gs}}=\frac{\left(\sqrt{p_1}-k_2\right)^2}{\left|V_{off}\right|\left[-\left(\sqrt{p_1}-k_2\right)^2+2\cosh\left(\frac{\pi L_2}{2d}\right)\left\{2k_4E_cL_1\left(\frac{\sqrt{p_1}-k_2}{\sqrt{p_1}}\right)+f(p_1)\right\}\right]}$$

For short channel devices, $R_i\cdot C_{gs}$ can be approximated by L_g/v_{sat} .Therefore, $R_i=\frac{L_g}{v_{sat}C_{gs}}$ and the cut-off frequency (f_T) of the device is given as:

$$f_T=g_m\big/2\pi\left(C_{gs}+C_{gd}\right) \tag{11}$$

The short circuit admittance parameters Y_{11} (input admittance) and Y_{21} (forward transfer admittance) are expressed in terms of transconductance (g_m), gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) as:

$$Y_{11}=\frac{\omega^2C_{gs}^2R_i}{D_1}+j\omega\left(\frac{C_{gs}}{D_1}+C_{gd}\right) \tag{12}$$

$$Y_{21}=\frac{g_m}{1+j\omega C_{gs}R_i}-j\omega C_{gd} \tag{13}$$

where $D_1=1+\omega^2R_i^2C_{gs}^2$ and where, $\omega=2\pi f$ is the angular frequency *(f = 94GHz).*

IV. Intrinsic Noise Sources

1. Drain Noise Current

Following the detailed analysis already presented in [11] the open circuit drain voltage fluctuation due to Johnson Noise in linear region (I) is expressed as:

$$\overline{V_{d1}^2}=\frac{4kT_o\Delta f\left|V_{off}\right|}{I_d}\cosh^2\left(\frac{\pi L_2}{2d}\right)\left[\frac{1}{p^2}\left(\frac{s^3-p^3}{3}\right)+\delta p\ln\left(\frac{s}{p}\right)\right] \tag{14}$$

and the open circuit drain voltage fluctuation due to diffusion noise in the saturation region (II) is expressed as:

$$\begin{aligned}\overline{V_{d2}^2}&=\frac{16qD\Delta fI_d(d+b)^3}{\pi^5\varepsilon^2Z^2v_{sat}^3b^2}\sin^2\left(\frac{\pi b}{2(d+b)}\right)\\&\times\left(3+\exp\left(\frac{\pi L_2}{(d+b)}\right)-4\exp\left(\frac{\pi L_2}{2(d+b)}\right)+\frac{\pi L_2}{(d+b)}\right)\end{aligned} \tag{15}$$

where L_2 = L_g-L_1 = saturation region length, Δf = bandwidth, T_o = *300 K* , δ = noise temperature constant (=*1*), *D* = diffusion coefficient (= *35 cm²/s*) and b is the effective channel thickness expressed as:

$$b=\frac{\varepsilon}{q}\frac{d}{dn_s}\left(E_f(L_1)\right)=\frac{\varepsilon}{q}\left(\frac{k_2k_4}{\left(\sqrt{p_1}-k_2\right)}+k_3\right) \tag{16}$$

Then, the mean square drain noise current is expressed as:

$$\overline{i_d^2} = \left(\overline{V_{d1}^2} + \overline{V_{d2}^2}\right) \Big/ r_d^2 \tag{17}$$

2. Gate Noise Current

Short circuit gate current fluctuation due to Johnson noise in linear region (I) is expressed as [10]:

$$\overline{i_{g1}^2} = \frac{8kT_o \Delta f \omega^2 L_1^2 \left|V_{off}\right| k_4^2}{qZr_d^2 v_{sat}^3 \left(\sqrt{p_1} - k_2\right)^6} \cosh^2\left(\frac{\pi L_2}{2d}\right)(R_o + R_1 + R_2 + R_3) \tag{18}$$

and the Short circuit gate current fluctuation due to diffusion noise in Region II is expressed as:

$$\overline{i_{g2}}^2 = \frac{16q^3\omega^2 D\Delta f (d+b)^3 \kappa'^2 L_1^2}{\pi^5 v_{sat}^3 \varepsilon^2 b^2 k_4^4 I_d r_d^2} \sin^2\left(\frac{\pi b}{2(d+b)}\right) \times \left\{3 + \exp\left(\frac{\pi L_2}{(d+b)}\right) - 4\exp\left(\frac{\pi L_2}{2(d+b)}\right) + \left(\frac{L_2 \pi}{(d+b)}\right)\right\} \tag{19}$$

V. NOISE PERFORMANCE PARAMETERS

The intrinsic admittance parameter dependent drain noise coefficient (P), gate-noise coefficient (R) and correlation coefficient (C) can be written as follows:

$$P = \frac{\overline{i_{d1}^2}}{4kT_o|Y_{21}|f} + \frac{\overline{i_{d2}^2}}{4kT_o|Y_{21}|f} = P_1 + P_2 \tag{20}$$

$$R = \frac{\overline{i_{g1}^2}|Y_{21}|}{4kT_o|Y_{11}|^2 f} + \frac{\overline{i_{g2}^2}|Y_{21}|}{4kT_o|Y_{11}|^2 f} = R_1 + R_2 \tag{21}$$

$$C = C_{11}\sqrt{\frac{P_1 R_1}{PR}} + C_{22}\sqrt{\frac{P_2 R_2}{PR}} = C_1 + C_2 \tag{22}$$

where $C_{11} = \frac{\overline{i_{g1} * i_{d1}}}{j\sqrt{\overline{i_{g1}^2} \cdot \overline{i_{d1}^2}}}$ and $C_{22} = \frac{\overline{i_{g2} * i_{d2}}}{j\sqrt{\overline{i_{g2}^2} \cdot \overline{i_{d2}^2}}} = 1$

(Notations 1 and 2 correspond to the linear and saturation regions respectively).

$\overline{i_{g1} * i_{d1}}$ is the correlation between the Johnson noise induced drain noise current and gate noise current which is expressed as [11]:

$$\overline{i_{g1} * i_{d1}} = -\frac{j\omega 2kT_o \Delta f q Z \left|V_{off}\right| L_1}{k_4^2 I_d^2 r_d^2} \cosh^2\left(\frac{\pi L_2}{2d}\right)(S_o + S_1 + S_2 + S_3) \tag{23}$$

The drain noise conductance *(g_{dn})* and the gate noise conductance *(g_{gn})* are expressed in terms of noise coefficients and admittance parameters as [17-19]:

$$g_{dn} = P|Y_{21}| \tag{24}$$

$$g_{gn} = R\frac{|Y_{11}|^2}{|Y_{21}|} \tag{25}$$

The noise conductance (g_n), noise resistance (r_n) and the correlation impedance (Z_c) are given by:

$$g_n = \left|\frac{Y_{11}}{Y_{21}}\sqrt{g_{dn}} - jC\sqrt{g_{gn}}\right|^2 + (1 - C^2) \cdot g_{gn} \tag{26}$$

$$r_n = R_s + R_g + \frac{g_{dn}}{|Y_{21}|^2}\left(\frac{(1 - C^2) g_{gn}}{g_n}\right) \tag{27}$$

$$Z_c = R_s + R_g + \frac{1}{g_n}\left[g_{dn} \cdot \frac{Y_{11}^*}{|Y_{21}|^2} + \frac{jC\sqrt{g_{gn} \cdot g_{dn}}}{Y_{21}}\right] \tag{28}$$

where, R_s is the parasitic source resistance *(=1.8 Ω)* and R_g is the gate metallization resistance (*=1.7* Ω) [2].

The Minimum Noise Figure *(NF_{min})* and the Minimum Noise Temperature *(T_{min})* are defined as:

$$NF_{\min} = 1 + 2g_n\left[\mathrm{Re}(Z_c) + \mathrm{Re}(Z_{sopt})\right] \tag{29}$$

and

$$T_{\min} = 2T_o g_n\left(\mathrm{Re}(Z_c) + \mathrm{Re}(Z_{sopt})\right) \tag{30}$$

where, Z_{sopt} is the optimum source impedance which is expressed as:

$$Z_{sopt} = R_{sopt} + jX_{sopt},$$

where $R_{sopt} = \sqrt{\left(\mathrm{Re}(Z_c)\right)^2 + \frac{r_n}{g_n}}$; $X_{sopt} = -X_c$

VI. RESULTS & DISCUSSION

Fig. 3 shows the variation of Gate-to-drain capacitance with drain voltage (V_{ds}) for different gate voltages. It is observed that the gate-to-drain capacitance decreases very rapidly with increase in the drain voltage and eventually saturates at higher value of $V_{ds.}$ The saturation of gate-to-drain capacitance is attributed to saturation in the drain current at higher V_{ds}. Therefore, due to very high value of C_{gd} at low values of drain voltage, its inclusion in the equivalent circuit for noise modeling is expected to cause a significant impact on the various noise performance parameters of the device especially at low values of drain voltage. Lower value of gate-to-drain capacitance is observed for lower value of V_{gs} due to decrease in the carrier concentration.

Fig. 4(a) shows the variation of the Drain Noise Coefficient (P) with gate voltage for different drain voltages (V_{ds}). At higher values of drain voltage, a lower value of P is observed. This is due to increased transconductance (g_m) and higher value of drain resistance at a higher drain voltage. The inclusion of the gate-to-drain capacitance (C_{gd}) results in higher magnitude of forward transfer admittance (Y_{21}) which in turn leads to lower values of P especially at lower values of drain voltages. Fig. 4(b) shows the value of P with and without the inclusion of C_{gd} at V_{gs}=-0.1 V and for V_{ds} =0.1 V, 0.2 V and 0.5 V .It is observed that the reduction in the value of P with inclusion of gate-drain capacitance is greater for lower value of drain voltages at which C_{gd} exhibits a higher value.

From Fig. 5(a) it is observed that the gate-noise coefficient (R) is lower for lower drain voltage. This occurs due to lower value of transconductance (g_m) at lower drain voltage which results in lower magnitude of forward transfer admittance (Y_{21}). In addition to this, it is observed that the inclusion of the gate-to-drain capacitance (C_{gd}) leads to further reduction in the values of the R. This is attributed to the higher magnitude of input admittance (Y_{11}) which is seen to dominate due to the fact that the R is inversely proportional to the square of the magnitude of Y_{11}.

Fig. 5(b) shows the value of Gate Noise Coefficient (R) with and without the inclusion of C_{gd} at V_{gs}=-0.1Vand V_{ds}= 0.1 V, 0.3 V and 0.5 V. The reduction in the value of gate noise coefficient (R) with the inclusion of

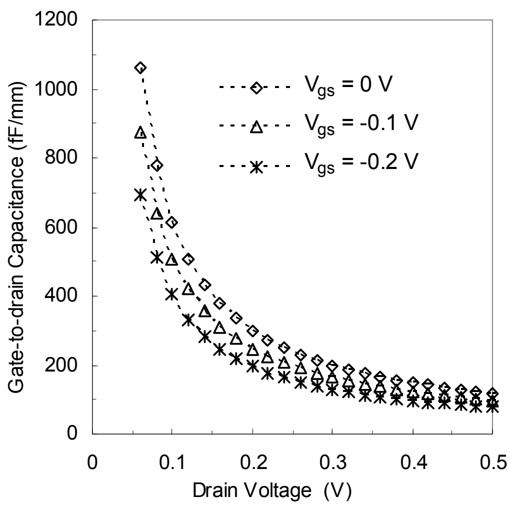

Fig. 3. Variation of Gate-to-drain capacitance (C_{gd}) with Drain Voltage (V_{ds}) for different values of gate voltage (V_{gs}).

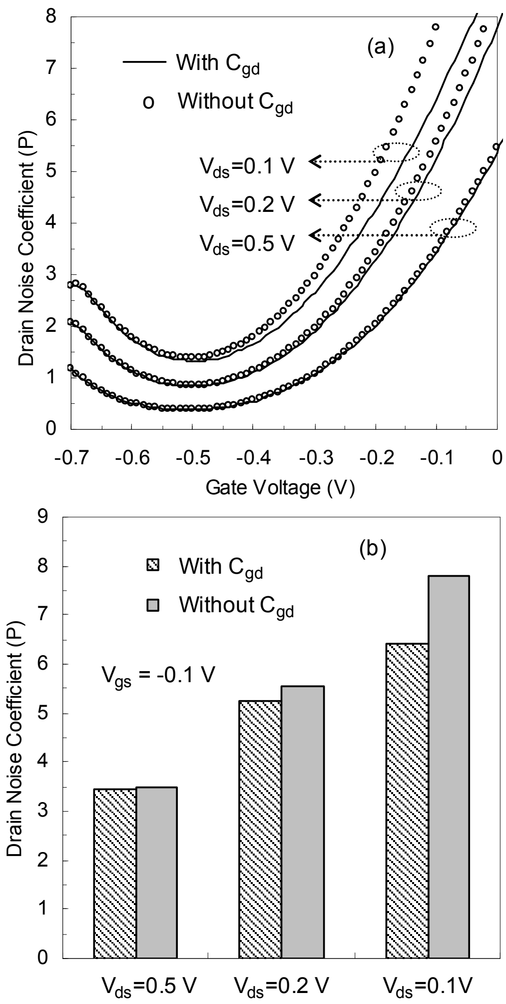

Fig. 4. (a) Variation of Drain Noise Coefficient (P) with Gate Voltage (V_{gs}) at different values of drain voltages (V_{ds}), (b) Effect of C_{gd} on P for different V_{ds} and at V_{gs}=-0.1 V.

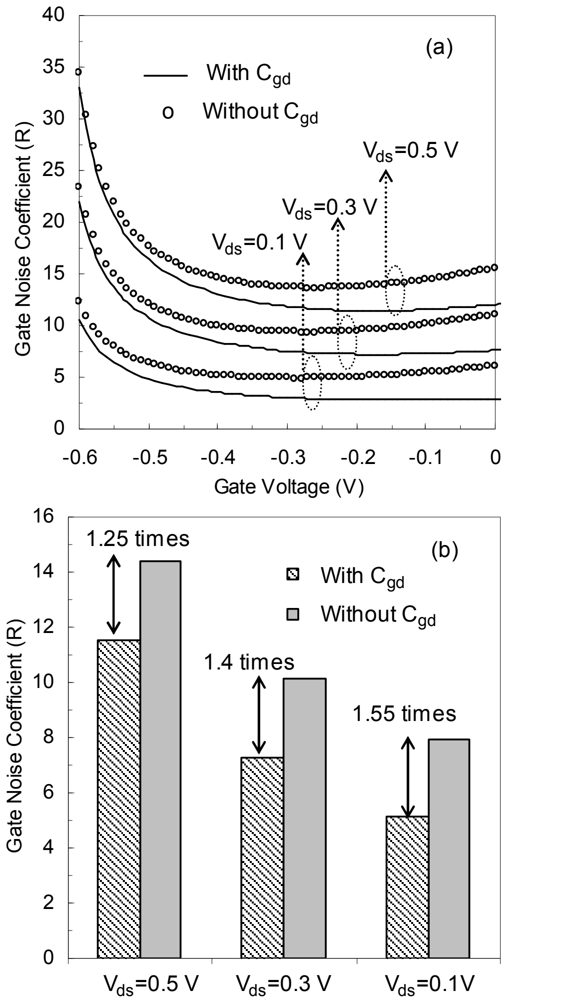

Fig. 5. (a) Variation of Gate Noise Coefficient (R) with Gate Voltage (V_{gs}) at different values of drain voltages (V_{ds}), (b) Effect of C_{gd} on R for different V_{ds} and at V_{gs}=-0.1 V.

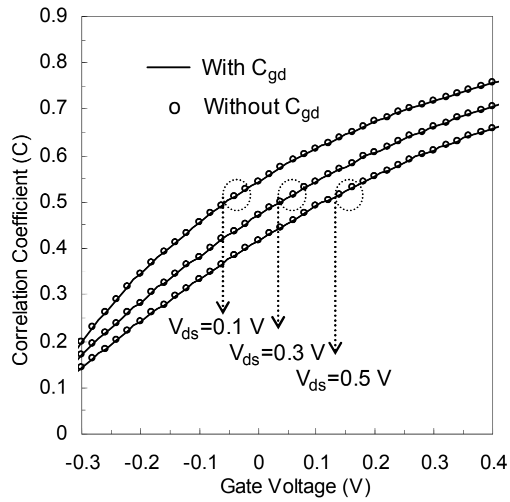

Fig. 6. Variation of Correlation Coefficient (C) with Gate Voltage (V_{gs}) at different values of drain voltages (V_{ds}).

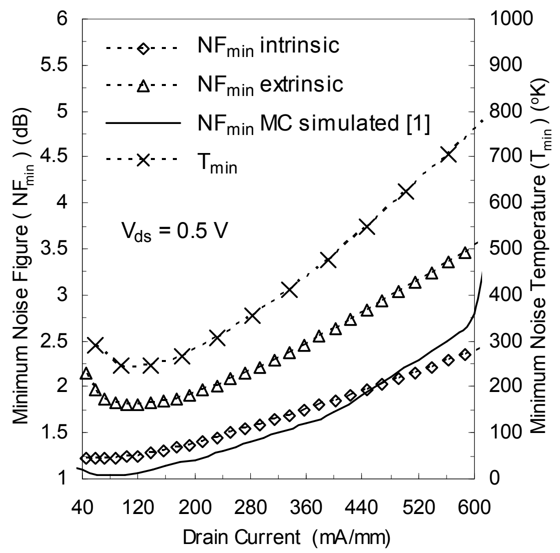

Fig. 7. Variation of NF_{min} and T_{min} with drain current.

gate-to-drain capacitance is observed to be more prominent for lower values of drain voltage.

Fig. 6 shows the variation of Correlation Coefficient (C) with gate voltage for different values of drain voltage. Although, the drain noise coefficient (P) and the gate noise coefficient (R) decrease with the inclusion of gate-to-drain capacitance, it is observed to cause no significant effect on the correlation coefficient (C). Lower value of C is observed for higher value of drain voltage which is attributed to the reduced correlation between the thermal noise induced drain noise current and gate noise current in the linear region.

Fig. 7 illustrates the variation of intrinsic and extrinsic Minimum Noise Figure and Minimum Noise Temperature with drain current. The analytically obtained variation of intrinsic Minimum Noise Figure with drain current is observed to show good agreement with that obtained using the Monte-Carlo simulation data [1]. The increase in NF_{min} and T_{min} at low values of drain current occurs due to decrease in transconductance (g_m) which results in the increase in the drain noise coefficient (P) and also due to the reduction in the gate-source capacitance (C_{gs}) which leads to higher value of gate noise coefficient (R). At higher drain current, the increase in the NF_{min} and T_{min} is attributed to increase in the diffusion noise.

Fig. 8 shows the variation of cut-off frequency (f_T)

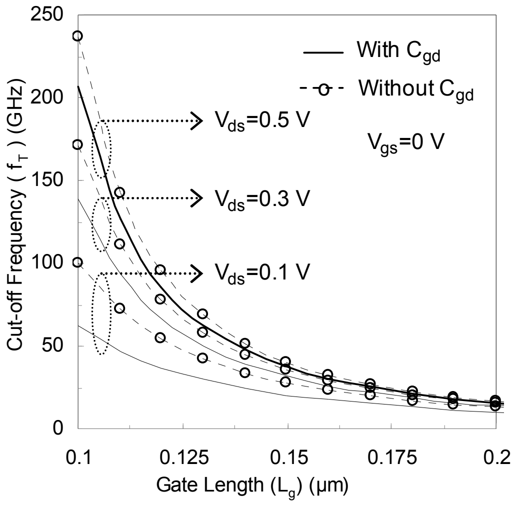

Fig. 8. f_T Vs gate-length for different values of drain voltage.

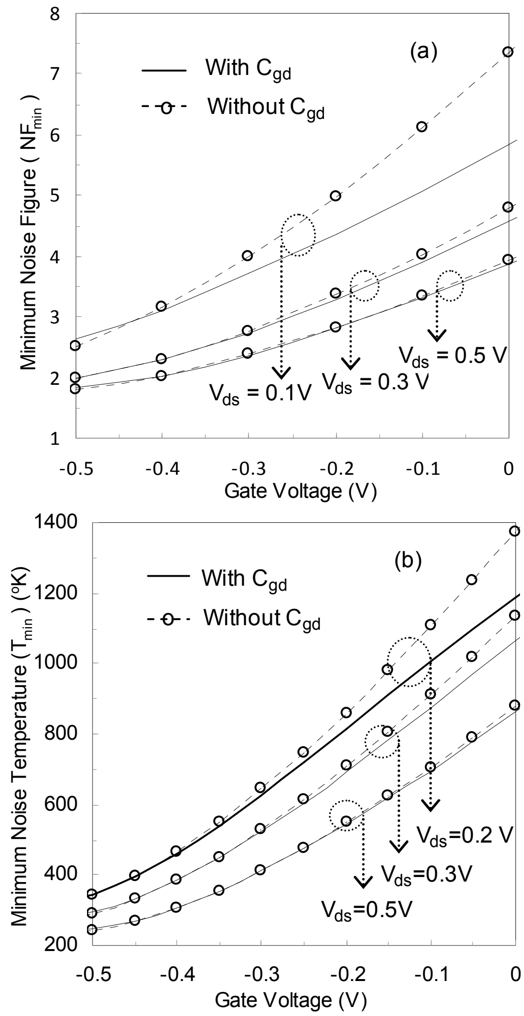

Fig. 9. Variation of (a) NF_{min}, (b) T_{min} with V_{gs} at different V_{ds}.

with gate-length at different values of drain voltages. The cut-off frequency is observed to increase with decrease in gate-length. This is attributed to the decrease in the gate-to-source capacitance (C_{gs}) with reduction in gate-length. The inclusion of C_{gd} in the evaluation of f_T results in lower value of cut-off frequency. This reduction in the cut-off frequency with the inclusion of C_{gd} is more prominent at low drain voltages at which the magnitude of C_{gd} is very high. Therefore, a lower value of C_{gd} is desirable for a higher cut-off frequency.

Fig. 9 illustrates the variation of Minimum Noise Figure (NF_{min}) and Minimum Noise Temperature (T_{min}) with gate voltage for different values of drain voltage. The inclusion of C_{gd} causes reduction in NF_{min} and T_{min}. This reduction is observed to be more significant for lower values of drain voltage at which the gate-to-drain capacitance is higher. This improvement in the noise performance with inclusion of C_{gd} is attributed to lower values of P and R which lead to lower value of noise resistance and hence lower Minimum Noise Figure and Minimum Noise Temperature. Higher value of NF_{min} and T_{min} at lower drain voltage is attributed to lower value of g_m which leads to higher value of P.

V. Conclusions

In the present work, the effect of the gate-drain capacitance (C_{gd}) has been incorporated in the earlier proposed charge control based noise model for a more accurate evaluation of the Minimum Noise Figure and Minimum Noise Temperature, especially at a lower values of drain voltage at which the value of C_{gd} is very high to cause a significant impact on the noise coefficients and hence on the overall noise performance of the device. While, the incorporation of feedback capacitance (C_{gd}) in the equivalent circuit model at low drain voltage predicts better noise performance in terms of lower minimum noise figure, at the same time, it also predicts lower cut-off frequency.

Therefore, at low values of V_{ds}, the impact of the gate-drain capacitance (C_{gd}) (which represents the level of feedback) should not be neglected for accurate evaluation of RF and noise performance of the device (in terms of various figures of merit such as NF_{min} and f_T) that corresponds well with the experimental measurements.

ACKNOWLEDGMENTS

The authors are grateful to the University Grants Commission for providing support for carrying out this research work.

REFERENCES

[1] B.G. Vasallo , N. Wichmann, S. Bollaert, Y. Roelens, A. Cappy, T. Gonzalez , D. Pardo and J. Mateos, "Comparison Between the Noise Performance of Double- and Single- Gate InP Based HEMTs", *Electron Devices, IEEE Transactions on,* Vol.55, No. 6, pp. 1535-1540, 2008.

[2] B.G. Vasallo , N.Wichmann, S. Bollaert, Y. Roelens, A. Cappy, T. Gonzalez , D. Pardo, and J. Mateos, "Comparison Between the Dynamic Performance of Double- and Single- Gate InP Based HEMTs" *, Electron Devices*, *IEEE Transactions on* , Vol.54, No.11, pp. 2815-2822, 2007.

[3] B.G. Vasallo , Nicolas Wichmann, Sylvain Bollart, Yannick Roelens, A. Cappy, Tomas Gonzalez , Daniel Pardo, and Javier Mateos, "Monte Carlo Comparison Between InP-Based Double–Gate and Standard HEMTs", *Ist European Microwave Integrated Circuits Conference*, *Proceedings of the*, pp. 304-307,September, 2006.

[4] N. Wichmann, I. Duszynski, S. Bollart, X. Wallart, Javier Mateos, A. Cappy, **"**InGaAs/InAlAs Double-Gate HEMTs on transferred substrate", *Electron Device Letters*, *IEEE*, Vol.25, No. 6, pp. 354-356, 2004.

[5] N. Wichmann ,I. Duszynski, S. Bollaert, X. Wallart, J. Mateos, A. Cappy, "100nm InAlAs/InGaAs Double-Gate HEMT using transferred substrate", *IEDM Tech. Dig.*, pp. 1023-1026, December, 2004.

[6] N. Wichmann, I. Duszynski, T. Parenty, S. Bollaert, J. Mateos, X. Wallart, A. Cappy, "Double Gate HEMTs on Transferred Substrate", *Indium Phosphide and related materials*, *International Conference on*, pp. 118- 121, 2003.

[7] M. Bhattacharya, J. Jogi, R.S. Gupta, M. Gupta, "Scattering parameter based modeling and simulation of symmetric tied-gate InAlAs/InGaAs DG-HEMT for millimeter-wave applications", *Solid-State Electronics*, Volume 63, No. 1, pp. 149-153, September, 2011.

[8] R.A. Pucel, H.A. Haus , H. Statz, "Signal and Noise properties of GaAs microwave FET", *Advances in electronics and electron physics, Academic, New York* , Vol. 38, pp. 195-265, 1975.

[9] Y. Ando, T. Itoh, "DC, Small-signal, and Noise Modeling for Two Dimensional Electron Gas Field-Effect Transistors Based on Accurate Charge-Control Characteristics", *Electron Devices*, *IEEE Transactions on* ,Vol.37, No. 1, pp. 67-78, 1990.

[10] A.F.M Anwar and K.W. Liu, "A noise model for high electron mobility transistors", *Electron Devices* , *IEEE Transactions on*, Vol. 41, No. 11, pp. 2087-2092, 1994.

[11] M. Bhattacharya, J. Jogi, R.S. Gupta, and M. Gupta., "An Accurate Charge Control Based Approach for Noise Performance Assessment of a Symmetric Tied-gate InAlAs/InGaAs DG-HEMT", *Electron Devices, IEEE Transactions on,* Vol .59, No. 6, pp. 1644-1652, 2012.

[12] ATLAS Device Simulator, SILVACO International 2010.

[13] H. Fukui, "Optimal Noise Figure of microwave GaAs MESFETs", *Electron Devices, IEEE Transactions on,* Vol. 26, No. 7, pp. 1032-1037, 1979.

[14] T.M. Brooks, "The Noise properties of High Electron Mobility Transistors", *Electron Devices, IEEE Transactions on,* Vol. 33, No. 1, pp. 52-57, 1986.

[15] A. Cappy and W. Heinrich, "High frequency FET noise performance: A new approach", *Electron Devices, IEEE Transactions on,* Vol. 36, no. 2, pp. 403-409, 1989.

[16] N. Dasgupta, A. Dasgupta, "An Analytical expression for sheet-carrier concentration Vs gate-voltage for HEMT modeling, *Solid-State Electronics*, Vol. 36, No. 2, pp. 201-203,1993.

[17] Vandana Guru, H.P. Vyas, Mridula Gupta, R.S. Gupta, "Analytical Noise Model of a High Electron Mobility Transistor for Microwave Frequency Application", *Microwave and Optical Technology Letters*, Vol. 40, No. 5, pp. 410-417, 2004.

[18] H. Statz, H.A. Haus, R.A. Pucel, "Noise characteristics of Gallium Arsenide Field Effect

Transistors, *Electron Devices*, *IEEE Transactions on*, Vol.21, No. 9, pp. 549-562, 1974.

[19] Vandana Guru , H.P. Vyas, Mridula Gupta, R.S. Gupta, "Evaluation of Scattering Parameters, Gain, and Feedback-Capacitance Dependent Noise Performance of a Pseudomorphic High Electron Mobility Transistor", *Microwave and Optical Technology Letters*, Vol. 47, No. 1, pp. 51-56, 2005.

Monika Bhattacharya received her B.Sc. degree and M.Sc. degree in Electronics from the University of Delhi, Delhi, in 2007 and 2009 respectively. She is pursuing research at Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus on RF and noise performance modeling and simulation of double gate InAlAs/InGaAs High Electron Mobility Transistor. Her other interests invlove fabrication and experimental study of such high performance devices.

Jyotika Jogi received B.Sc. degree in Physics, M.Sc. degree in Electronic Science, M.Phil. degree in Electronic Science, and Ph.D. degree in Micro-Electronics from the University of Delhi, Delhi, India, in 1986, 1988, 1990, and 2003, respectively. She worked as a Lecturer in Sri. Venkateswara College, University of Delhi from 1988 to 1991 and has been teaching at Atma Ram Sanatan Dharma College, University of Delhi since 1991, as an Associate Professor in Electronic Science. She is presently on deputation as Faculty at Cluster Innovation Centre, University Of Delhi. Her main research interests are in the field of modeling and simulation of ultrahigh speed devices and quantum heterostructures. She is currently working on Modeling, Simulation and Study of Noise Performance and Noise Characteristics of Double Gate InP-based InAlAs/InGaAs High Electron Mobility Transistors for High Power and Tera Hz Frequency Applications

R. S. Gupta received the B.Sc. and M.Sc. degrees from Agra University, Agra, India, in 1963 and 1966, respectively, and the Ph.D. degree in electronic engineering from the Institute of Technology, Banaras Hindu University, Varanasi, India, in 1970. In 1971, he was with Ramjas College, University of Delhi, Delhi, India. In 1987, he was with the Department of Electronic Science, University of Delhi South Campus, New Delhi, as a Reader and later as a Professor from 1997 to 2008. He was CSIR Emeritus Scientist with the Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, until March 2009. He heads several major research projects sponsored by the Ministry of Defense, the Department of Science and Technology, the Council of Science, and the Industrial Research and University Grants Commission. In 1988, he was a Visitor with the University of Sheffield, Sheffield, U.K., under the ALIS Link exchange program and also visited several U.S. and Spanish universities in 1995 and 1999, respectively. He also visited the Czech Republic in August 2003; Korea in November 2003; Rensselaer Polytechnic Institute, Troy, NY, in August 2004; and China in December 2005. In Dec 19, 2007 he visited Rome, Italy and in 2009 he visited North Texas University and Southeast Missouri State University USA. He contributed the chapter entitled "MOSFET Modeling" in the *Encyclopedia on RF and Microwave Engineering* (Wiley, 2005). His current interests and activities include modeling of SOI sub-micrometer MOSFETs and LDD MOSFETs, modeling and design of HEMTs, hot-carrier effects in MOSFETs, and modeling of GaAs MESFETs for high-performance microwave and millimeter-wave circuits and quantum-effect devices. Prof. Gupta was an Executive Member of the IEEE Electron Devices Society/Microwave Theory and Techniques Society Chapter of the IEEE India Council. Prof Gupta is Life Senior Member IEEE and was Chairman of IEEE EDS Delhi Chapter. His name also appeared in the Golden List of the IEEE TRANSACTIONS ON ELECTRON DEVICES in December 1998, 2002, and 2004. He is a Fellow of the Institution of Electronics and Telecommunication Engineers (India), a Life Member of the Indian Chapter of the International Centre for Theoretical

Physics, and a Life Member of the Semiconductor Society of India and chairman of society for microelectronics and VLSI. He was the Secretary of ISRAMT'93 and the 1996 Asia–Pacific Microwave Conference (APMC'96), and the Chairman of the Technical Programme Committee of APMC'96. He edited the proceedings of both of these international conferences. He was the Chairman of APMC'2004 held in New Delhi in December 2004. He has been listed in *Who's Who in the World*. Prof Gupta was chairman of 12^{TH} ISMOT 2009 held in Dec 2009 in India. He is the author/coauthor of over 600 papers in various international and national journals and conference proceedings. 42 students have received their Ph.D. under his guidance. In addition to this he is currently supervising 8 students. He is currently a Professor and Head of the Department of Electronics & Communication Engineering, Maharaja Agrasen Institute of Technology (GGIP University, Delhi).

Mridula Gupta received the B.Sc. degree in physics, the M.Sc. degree in Electronics, the M.Tech. degree in Microwave Electronics, and the Ph.D. degree in optoelectronics from the University of Delhi, Delhi, India, in 1984, 1986, 1988, and 1998, respectively. Since 1989, she has been with the Department of Electronic Science, University of Delhi South Campus, New Delhi, India, where she is currently working as Professor and is also associated with Semiconductor Device Research Laboratory. She is the author/coauthor of approximately 235 publications in international and national journals and conference proceedings. She has supervised 14 Ph.D. students. She contributed the chapter entitled "MOSFET Modeling" in the *Encyclopedia on RF and Microwave Engineering* (Wiley, 2005). Her current research interests include modeling and simulation of MOSFETs, MESFETs, and HEMTs for microwave-frequency applications.