

Multi-channel 5Gb/s/ch SERDES with Emphasis on Integrated Novel Clocking Strategies

Changchun Zhang^{*,**,***}, Ming Li^{*}, Zhigong Wang^{**}, Kuiying Yin^{*}, Qing Deng^{*},
Yufeng Guo^{***}, Zhengjun Cao^{*}, and Leilei Liu^{***,****}

Abstract—Two novel clocking strategies for a high-speed multi-channel serializer-deserializer (SERDES) are proposed in this paper. Both of the clocking strategies are based on groups, which facilitate flexibility and expansibility of the SERDES. One clocking strategy is applicable to moderate parallel I/O cases, such as high density, short distance, consistent media, high temperature variation, which is used for the serializer array. Each group within the strategy consists of a full-rate phase-locked loop (PLL), a full-rate delay-locked loop (DLL), and two fixed phase alignment (FPA) techniques. The other is applicable to more awful I/O cases such as higher speed, longer distance, inconsistent media, serious crosstalk, which is used for the deserializer array. Each group within the strategy is composed of a PLL and two DLLs. Moreover, a half-rate version is chosen to realize the desired function of 1:2 deserializer. Based on the proposed clocking strategies, two representative ICs for each group of SERDES are designed and fabricated in a standard 0.18 μm CMOS technology. Measurement results indicate that the two SERDES ICs can work properly accompanied with their corresponding clocking strategies.

Index Terms—SERDES, clocking strategy, phase-locked loop, delay-locked loop, fixed phase alignment

I. INTRODUCTION

Moore's Law predicts that the complexity of integrated circuits (ICs) doubles every 18 months, which suggests that the communication throughout between ICs and external worlds should increase proportionally; however, Rent's rule forecasts that the input/output (I/O) number will rise at a slower pace. Consequently, in order for a system consisting of ICs to exhibit a maximum performance, each I/O bandwidth should be increased, in addition to parallel interconnect strategies [1]. A high-speed multi-channel or parallel serializer-deserializer (SERDES) is regarded as an excellent choice, nowadays.

It is well known that almost I/O communication can work properly, only accompanied with appropriate clocking strategies. Especially, as for a high-speed multi-channel SERDES, because of the existence of high density, skew and jitter, and so on, clocking strategies play a critical role in its quality, density, throughout, etc.

Based on an extensive survey, two novel clocking strategies for a high-speed multi-channel SERDES are proposed, which have such advantages as reliability, compactness, and no need of reference clock and off-chip tuning. Furthermore, these clocking strategies are based on groups, which facilitate the expansibility of the SERDES. Finally, each representative group within the serializer and deserializer arrays for the 5 Gb/s/ch SERDES is designed and fabricated in a standard 0.18 μm CMOS technology, respectively. Measured results shows the SERDES ICs can function properly with the

Manuscript received Jan. 27, 2013; accepted May. 7, 2013

^{*}Nanjing Research Institute of Electronics Technology, Nanjing 210013, China

^{**}Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China

^{***}Nanjing University of Posts and Telecommunications, Nanjing 210046, China

^{****}State Key Laboratory of Millimeter Waves, Southeast University, Nanjing Jiangsu 210096, China

E-mail : changchunzhang2007@hotmail.com

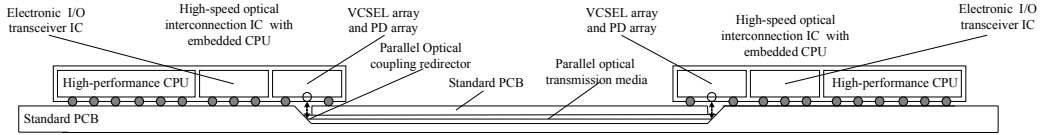


Fig. 1. Experimental platform about the interconnection between high-performance CPUs.

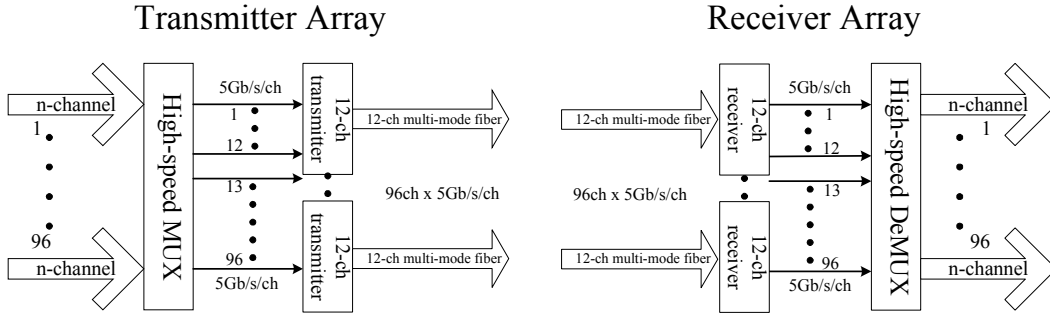


Fig. 2. High-speed I/O transceiver array between CPUs.

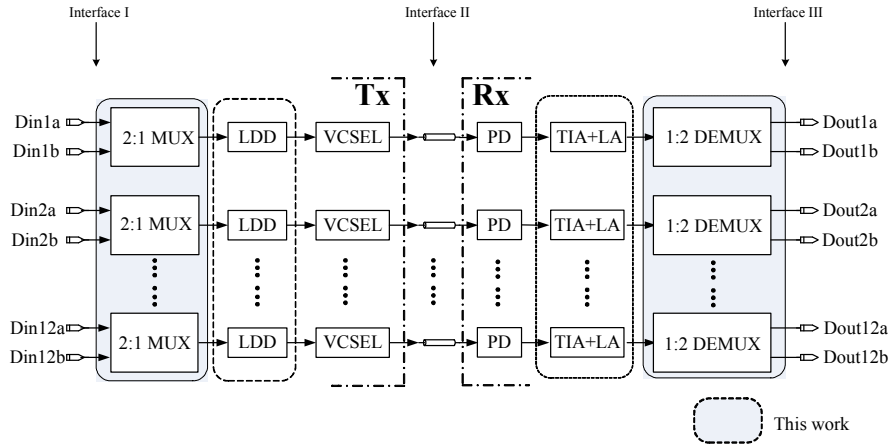


Fig. 3. Block diagram of a 12-ch high-speed parallel optical link.

proposed clocking strategies.

II. TARGET APPLICATION SYSTEM

This work aims at the high-speed interconnection between high-performance CPUs, which is shown in Fig. 1. The target application system is mainly composed of two high-speed optical interconnection ICs with embedded CPUs, which are mounted on the surface of a standard PCB, and parallel optical transmission media, usually 850 nm multimode fiber, buried in the PCB. The interconnection ICs consist of high-performance CPUs, electronic I/O transceiver ICs, and optical VCSEL/PD arrays.

Fig. 2 indicates the high-speed I/O transceiver array between CPUs. As for the transmitter array, a number of low-speed data from CPUs are multiplexed into fewer high-speed data (5 Gb/s/ch), which are then converted into optical signals along fiber array by transmitters; as for the receiver array, optical signals from fibers are converted into electronic higher-speed data by the receiver array, which are then demultiplexed into low-speed data, eventually fed into another CPU. Totally, 96-ch fiber (I/O) arrays are able to carry up to 480 Gb/s data throughout.

According to Fig. 2, it can be found that a 12-ch transceiver array is the basic unit. Fig. 3 shows that the block diagram of a 12-ch high-speed parallel optical link,

which consists basically of multiplexer (MUX), laser-diode driver (LDD), vertical cavity surface emitting laser (VCSEL) diode, photodiode (PD), trans-impedance amplifier (TIA), limiting amplifier (LA), and demultiplexer (DeMUX) array. VCSEL and PD array are usually standard optical devices, and others are designed in standard 0.18 μm CMOS technology. LDDs, VCSELs, PDs, TIAs and LAs are media-dependent; however, MUX/DeMUX array, that is, SERDES (serializer/deserializer) array are media-independent, so researches on them are of universal significance. Here, the MUX and DeMUX are also called serializer and deserializer, respectively.

III. PROPOSED MIXED CLOCKING STRATEGIES

Taking a cursory glance, it seems that an I/O interface, e.g. Fig. 3, is irrelevant to clocking. However, virtually, any digital I/O interface, esp. SERDES, can function only under the premise of sophisticated clocking strategies.

1. Clocking Issues Related with Parallel I/O Interfaces

Skew and jitter are the two basic problems related to clocking [2]. Skew characterizes the spatial variation, or static variation of a clock phase, which mainly results from path mismatch, parasitic capacitance and so on. Whereas jitter depicts the dynamic variation of a clock phase, which usually results from power/ground noise, crosstalk, device noise and so on. The jitter below 10 Hz is also called as wander. Finally, it should be pointed out that the so-called clock here includes the clock inherent in data stream.

Compared to a single-channel I/O interface, as shown in Fig. 4, besides jitter, a multi-channel I/O interface should account for some other issues related to skew, e.g. skew between data from different channels, skew between data and clock, skew between clocks, and so on.

2. Conventional Clocking Strategies

As shown in Table 1, according to the relative magnitude among UI (bit unit width), inter-channel skew, and jitter, the clocking strategies for parallel I/Os can be

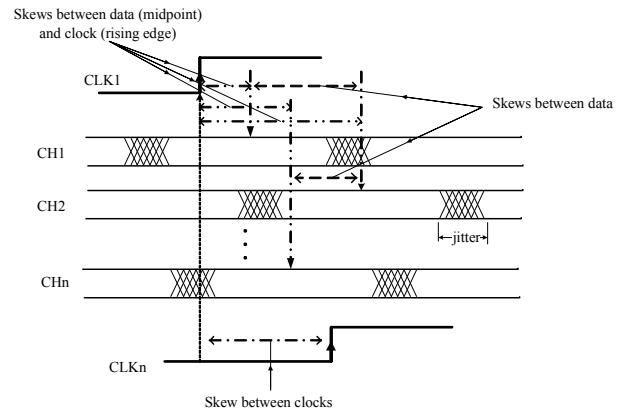


Fig. 4. Jitter and skew Issues in parallel interconnection.

classified into the below three categories.

As for application A, the situations are excellent, which usually exhibit characteristics of low speed, short distance, constant temperature and so on, so the conditions that skew is much smaller than UI, and jitter is much smaller than UI, can be satisfied. For this kind of application, it is sufficient that only the phase relationship between any channel of data and the clock is assured by some means, and then clocking tree strategies, e.g. H-type tree, are applied to make sure that all clock phases to their corresponding channel of data are almost same.

As for application B, the situations are just moderate, where, usually, speed is not too high, but I/O distance is a little long, or/and the temperature varies slowly, and so on, so the conditions that skew is comparable to, even bigger than UI can be satisfied. For this kind of application, de-skew strategies can be used to tune the phase relationships between data and their corresponding clocks. Usually, at the stage of startup, a segment of special code pattern is needed to accomplish the de-skew task. In consideration of wander, the de-skew operation is usually carried out every other some time.

As for application C, the situations are tough, where, usually, speed is high, crosstalk is serious, or/and the temperature varies largely, and so on. For this kind of application, automatic phase identification/tracking strategies, such as feed-forward, feedback, blind-over-sampling techniques, are required, which can continuously track the phase variations inherent within data.

In the above discussion, the de-skew between given data and local clocks are mainly involved; whereas in order to conquer the inter-channel de-skew, a FIFO (First-In-First-Out) technique is widely used in the

downstream stages.

The above techniques are discussed from the angle of the phase relationship adjustment. According to the synchronization relationship between clocks used to sample data locally and clocks used to generate data at transmitters, the clocking strategies can also be classified into (1) system or global clocking [4, 6, 11], where the reference clock is shared by both sides; (2) source synchronous/forwarded clocking [3, 9, 10, 12, 13], where a clock is fed from transmitters along data channels; (3) embedded clocking [7, 8, 22], where a clock is embedded into data at the transmitter, and then is extracted at the receiver; (4) local clocking [20, 21, 24-34], where clocks are synthesized locally. (1) ~ (3) belong to synchronous, or mesochronous clocking strategies, which is applicable to applications A ~ C, and almost all of conventional CDR (clock and data recovery) techniques can be used; whereas (4) belongs to plesiochronous one, which is preferable to application C, and PI/PS (phase interpolation/phase selection) type and blind-oversampling (blind-oversampling) techniques are usually used [2, 35].

Clocking strategies are mainly realized by some special CDR-related techniques. A CDR consists basically of a CR (clock recovery) or CE (clock extraction), and a DR (data recovery). The latter can be further divided into data decision and phase alignment (or phase adjustment). As CDR techniques evolve and a lot of CDR-related techniques appear, the concept or connotation of a CDR is generalized, but the phase alignment is usually indispensable.

Table 2 lists several basic CDR-related techniques, including PLL(phase-locked loop), DLL(delay-locked loop), MPA (Manual Phase Alignment), FPA (Fixed Phase Alignment), PI/PS, and BOS. These techniques are then compared in terms of CE, APA (automatic phase alignment), MPA (manual phase alignment), ACI (Adjacent-Channel Interference), stability, complexity, power consumption, occupied area, and degree of integration. The FPA realizes phase alignment by means of fixed path (length and trace) matching layout and load balance techniques.

3. Proposed Novel Mixed Clocking Strategies

According to Table 1, from A to C, the function of the corresponding clocking strategies rise; however, their

Table 1. Clocking strategies for 3 kinds of application situations

App.	Situations	Clocking strategies	Complexity	Function	Reference
A	skew << UI; jitter << UI	clocking tree	low	low	[4] - [8]
B	skew ≈, or > UI; jitter << UI	(periodical) de-skew	moderate	moderate	[9] - [17]
C	jitter ≈, or >UI	automatic phase identification /tracking	high	high	[18] - [33]

Table 2. Comparison among several basic CDR-related techniques

	CE	APA	MPA	ACI	stability	complexity	power	area	integration
PLL	Y	Y	N	Y	poor	high	high	large	good
DLL	N	Y	N	N	fair	fair	fair	medium	good
MPA	N	N	Y	N	good	low	fair	medium	poor
FPA	N	N	N	N	good	low	low	small	good
PI/PS	N	Y	N	N	fair	high	high	large	good
BOS	N	Y	N	N	good	high	high	large	good

complexity also increases proportionally. Usually, from different levels, the application will take on different characteristics, so different CDR-related techniques belonging to different conventional clocking strategies can be mixed up for given applications. From another point of view, although Table 1 shows general clocking strategies for some typical parallel I/O application situations, actually, due to the existence of some limited factors, such as density, power, reliability, the freedom of choice over clocking strategies is restricted. Any single clocking strategy based on a single CDR-related technique is not sufficient, not to mention optimum, so mixed clocking strategies based on several CDR-related techniques are proposed to make a tradeoff to meet the special overall requirements, or to achieve maximum performance.

From Fig. 3, there exist three interfaces related to the parallel optical link or SERDES. Because interface III is responsible by the downstream CPU or other ICs, only both interfaces I and II are concentrated on in this paper. The specification comparison between the two target interfaces is shown in Table 3. No any reference clocks for the interface are provided by the system, and power consumption should be reduced as possible.

As for both interfaces I and II, because no any system/local reference clock is provided, the embedded

Table 3. Specification comparison between two target interfaces

Interfaces	Parallel electrical interface (Interface I)	Parallel optical interface (Interface II)
Transmission media	PCB, Cu, electrical	fiber, optical
Number of channels	24-channel	12-channel
speed	2.5Gb/s/ch	5G/s/ch
distance	short (~ 10 cm)	long (~ m)
Layout size requirement	< 125 $\mu\text{m}/\text{ch}$ (on average)	< 250 $\mu\text{m}/\text{ch}$ (on average)

clocking strategies must be employed. All the CDR-related techniques shown in Table 2 are able to recover the data, but only the PLL technique can extract clock information locally from the corresponding input data, so it must be required definitely. However, in consideration of die area, power, pulling-in effects between VCOs, and so on, it isn't wise that a PLL is used for each channel. The remaining techniques can work only with the help of external clocks, so, in other words, they can be employed here only accompanied by PLLs. Furthermore, the MPA is excluded because of the need of external tuning, and also, both PI/PS and BOS techniques are not preferred in view of die area, power and complexity, and so on. In conclusion, in terms of their advantages such as compactness, reliability, low power, low complexity, DLL and FPA techniques are considered here.

Specially, according to Table 3, the interface I exhibits the following characteristics: multi-channel (24 channels), high speed (2.5 Gb/s/ch), space-limited (<125 $\mu\text{m}/\text{ch}$), high temperature variation, serious crosstalk, short distance (~10 cm) and so on.

Since both ends of interface I reside on a PCB and the transmission distance is short, for those neighboring channels, the application occasion is similar to application A, where the inter-channel skew is shorter, jitter, esp. wander, inherent in them is highly correlative, so the PFA technique is preferred over the DLL one, due to its small size.

For those channels, where spaces between them are slightly further, and the inter-channel skews are slightly larger, so the FPA technique isn't applicable. However, due to the similar or consistent situations, e.g. power supply, temperature, and so on, the consistency between the jitter, esp. wander inherent in these channels remain higher, where the application surroundings are approaching

application B, so the DLL technique is more preferred. The DLL is used because it can possess the ability of APA.

Whereas for those channels where spaces between them are further, jitter (esp. wander) are almost irrelevant, which approaches application C, so the PLL technique is preferred. Here, the DLL is out of place, the reasons are as follows:

(1) Long-distance transfer will degrade clock signals, for example, to increase jitter, or incur distortion, and clock buffer chains will also help to crosstalk between channels.

(2) A long inter-channel wander will need an even longer VCDL (voltage-controlled delay line) chain, up to several, even more, UIs, which will increase power and die area sharply. The limited phase tuning range inherent in a DLL makes it unfit for the occasions where the relative wanders are large. Even though the control circuits exist here, every time that they work, the transient process, and then bit errors will appear. Therefore, the DLLs are preferred for de-skew stages, or occasions where the relative wander is not too large.

Compared to interface I, interface II possesses the following characteristics: Fewer channel (12 channels), higher speed (5 Gb/s/ch), larger pitch (250 $\mu\text{m}/\text{ch}$), longer distance (~m) and so on

Because of higher speed, longer distance, conversion between optical and electrical domains, and so on, the relative skew even between neighboring channels is hardly controlled, so the FPA technique is ill-suited. Except the FPA, the DLL and PLL can be used alternately because of the same reasons as that for interface I, and due to the smaller channel number, the space allows that only DLLs and PLLs are used.

Based on the above analysis, two novel mixed clocking strategies are proposed for interfaces I and II of the parallel SerDes application, respectively.

As for the proposed clocking strategies, shown in Fig. 5, the interface channels are divided into several identical groups. Within each group, different kinds of the above mentioned CDR-related techniques are combined to achieve the desired and comprehensive aims. Here, CH_{ij} indicates the j th channel of the i th group.

Within interface I, 4 channels are allocated for each group and 3 kinds of CDR-related techniques are designated for the 4 channels, a PLL for one, a DLL for

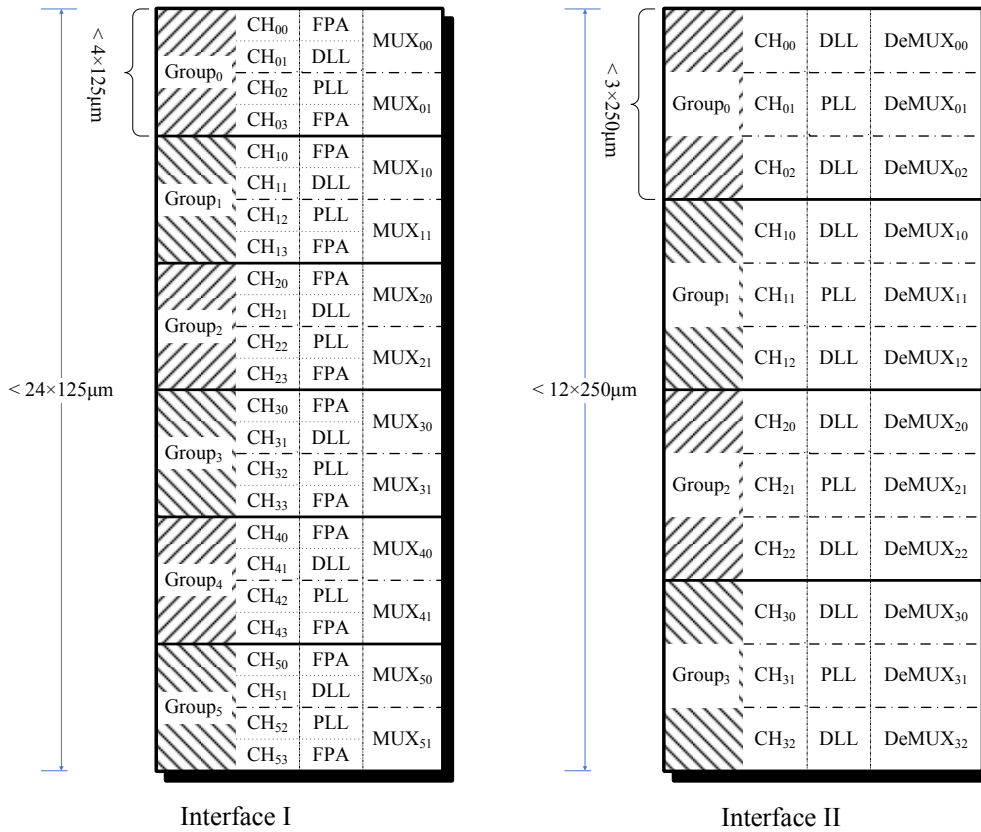


Fig. 5. The proposed mixed clocking strategies for interfaces I and II.

one, and two FPAs for the other two. For example, just as shown in Fig. 5, for the group₀, a PLL is for CH₀₂, a DLL for CH₀₁, and the two FPAs for CH₀₀ and CH₀₃.

The PLL is needed to extract a clock and realize the phase alignment locally, and the extracted clock is also fed into the DLL. At the same time, the two adjusted clocks from DLL and PLL are also provided to the other two channels by FPA.

Whereas within interface II, 3 channels are allocated for each group and 2 kinds of CDR-related techniques are designated for the 3 channels, a PLL for one, two DLL for the other two. For example, for the Group₀ of the interface II, a PLL is for CH₀₁, two DLL for CH₀₀ and CH₀₂, respectively.

Within both interfaces, PLLs and DLLs are placed shoulder to shoulder in order to facilitate the transfer of clock signals.

For each group, the clocking strategies are somewhat like the source synchronous one. Because of consistent temperature variation, crosstalk, and so on, the wander, even skew inherent in neighboring channels is similar.

Due to the low-pass characteristics of the PLL, the wander within the extracted clock is nearly same with the one inherent in the corresponding channel, and then also consistent with the one within neighboring channels, so DLL, even FPA can be used for the neighboring channels.

In order to reduce crosstalk by power supply, a separate power supply is preferred for each group, and it can also increase the wander, even jitter, consistency within each group.

IV. CIRCUIT DESIGN

Just as mentioned above, interfaces I and II, shown in Fig. 3, consist of several identical groups, respectively, so it's sufficient that only design for a group within each interface is focused on here. Owing to its superior performance, such as high speed, resistance to interference, the CML (current mode logic) is chosen [36, 37]. In addition to the core, input/output and inter-stage buffers are widely used to buffer, reshape and improve the circuit performance.

1. Circuit Design for Interface I

The block diagram of a group within interface I is shown in Fig. 6, from which the clocking strategy mentioned in the above section can be easily observed. Two 2:1 multiplexers (MUXs) are used to serialize 4-way input data into 2-way output data. The PLL, DLL, and FPA techniques are adopted to provide proper clocks for the two MUXs.

Fig. 7 shows the block diagram consisting mainly of a PLL and a MUX for interface I, which corresponds to the below two channels in Fig. 6. The PLL consists of a PFD (phase frequency detector), a V/I (voltage to current) convertor, a LF (loop filter) and an I/Q (in-phase/quadrature) VCO (voltage controlled oscillator). In consideration of PVT variation, the limited frequency acquisition range of a PD (phase detector) makes it

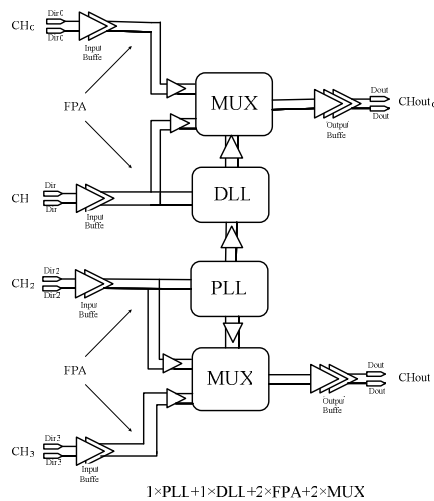


Fig. 6. Block diagram of a group within interface I.

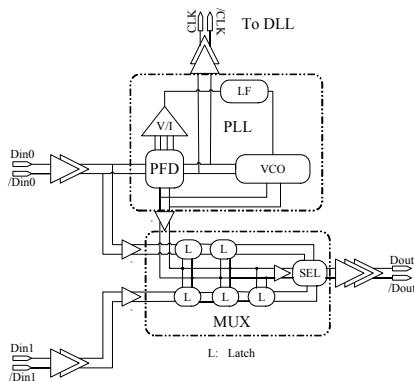


Fig. 7. Block diagram of a PLL and a MUX for interface I.

incapable of the reliable operation of the PLL, so a PFD is selected. Furthermore, a full-rate PFD is used instead of a fractional-rate one, because the clock with a frequency equivalent to the input data speed is required for the operation of the half-rate multiplexer. Finally, owing to its compact layout, a 4-stage inductorless ring VCO is adopted to generate I/Q clocks for the PFD. Here, it should be pointed out that, in this section, PD doesn't refer to a photodiode as in section II, but a phase detector.

As for the multiplexer, a half-rate one is chosen over its full-rate counterpart because of its low power consumption, small die area, and low complexity, and so on.

As shown in Fig. 8, the DLL (delay locked loop) for interface I mainly consists of a PD, a V/I convertor, a LF and a VCDL. Because the DLL needn't frequency acquisition, a full-rate PD is used. The VCDL should be long enough to provide sufficient varied phase shift range to allow for a large inter-channel wander, or to avoid dead lock.

The full-rate PD and full-rate PFD, which are used for the above mentioned DLL and PLL, respectively, are shown in Fig. 9. From this figure, it can be found that the full-rate PD is actually a double-edge-triggered flip-flop (DETFF), which consists of two latches and a conventional selector shown in Fig. 10(a) and (b), and the PFD [38] is composed of two identical DETFFs (or PDs) and a tri-state DETFF (Tri-DETFF) which is also called a frequency detector (FD). The main difference of the Tri-DETFF from the DETFF is that a tri-state selector shown in Fig. 10(c) is chosen over the conventional selector shown in Fig. 10(a).

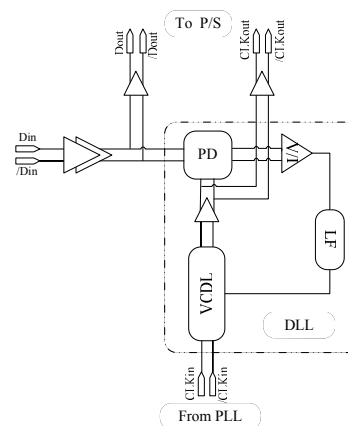


Fig. 8. Block diagram of a DLL for interface I.

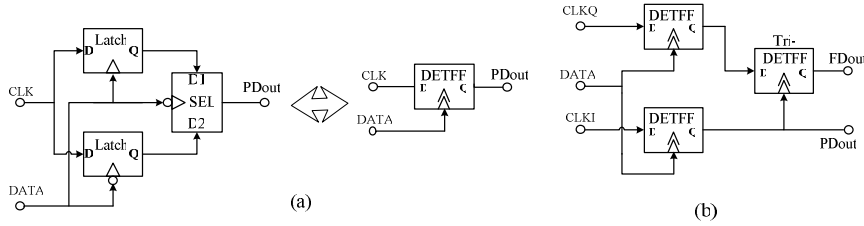


Fig. 9. Block diagrams of a full-rate PD (a) and a full-rate PFD (b).

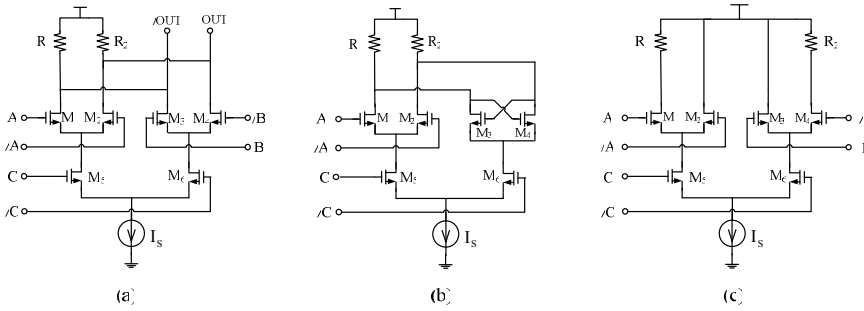


Fig. 10. Circuit diagrams of a conventional selector (a), a latch (b), a tri-state selector (c).

The timing diagrams for a group within interface I shown in Fig. 6 can be found in Fig. 11. $CHin_{i0}, CHin_{i1}, CHin_{i2},$ and $CHin_{i3}$ are the 4-way input data; $CHout_{i0}$ and $CHout_{i1}$ are the 2-way high-speed multiplexed output data. CLK_{i1} and CLK_{i2} are clocks extracted by the above mentioned DLL and PLL from $CHin_{i1}$ and $CHin_{i2},$ respectively, so, from Fig. 11, it can be seen that the rising edges of CLK_{i1} and CLK_{i2} are aligned with edges of $CHin_{i1}$ and $CHin_{i2},$ respectively.

From Fig. 11, there exists one quarter of a clock period ($T/4$) difference between the output data and their corresponding extracted clocks, which results from that, in order for an optimum phase relationship, a $T/4$ -phase-shifted clock is used for the selector within the half-rate MUX, shown in Fig. 7.

2. Circuit Design for Interface II

The block diagram of a group for interface II is indicated in Fig. 12, which is composed mainly of a PLL and two DLLs. The PLL is placed in between to facilitate the distribution of clock signals. Through the combination of a PLL and two DLLs within a group, 3-way input data can be deserialized into 6-way output data.

Fig. 13 shows the block diagrams of a PLL and a DLL for interface II. Contrary to the PLL and DLL for interface I, the half-rate PLL and DLL are used here. The

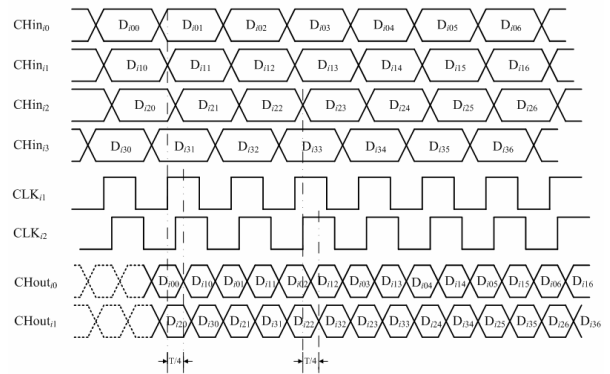


Fig. 11. Timing diagrams for a group within interface I shown in Fig. 6.

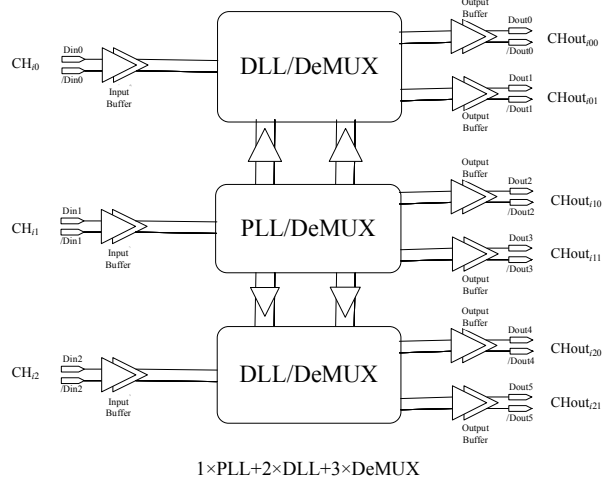


Fig. 12. Block diagram of a group within interface II.

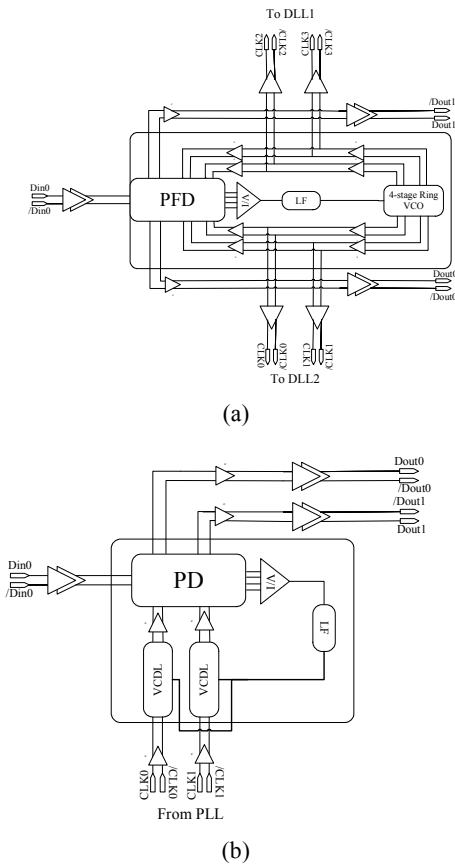


Fig. 13. Block diagram of a PLL (a) and a DLL, (b) for interface II.

advantages of the half-rate techniques are as follows: Firstly, no additional independent demultiplexers (DeMUXs) are needed, because the half-rate PFD or PD possesses the function of a 1:2 demultiplexer. Secondly, power consumption can be reduced largely because nearly all blocks can operate only at half a speed of the full-rate versions; finally, it's not easy for a multi-stage inductorless ring VCO to oscillate at 5 GHz reliably in standard 0.18 μm CMOS technology.

The PLL is composed of a half-rate PFD, a V/I converter, a LF and a ring VCO. The Savoj PFD [39] is chosen, shown in Fig. 14, which consists of two identical half-rate PD (IPD and QPD) and a FD. The FD is identical to the one used in the full-rate PFD for interface I. The basic building blocks, shown in Fig. 10, are also used for the PFD. From Fig. 14, 4-way differential clocks are needed for the PFD, so a 4-stage differential ring VCO is used. The VCO cell is given in Fig. 15, in which a current-folding technique [40] is used to

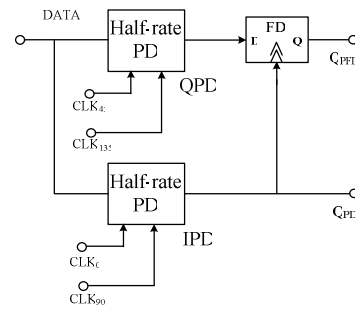


Fig. 14. Block diagram of a half-rate PFD.

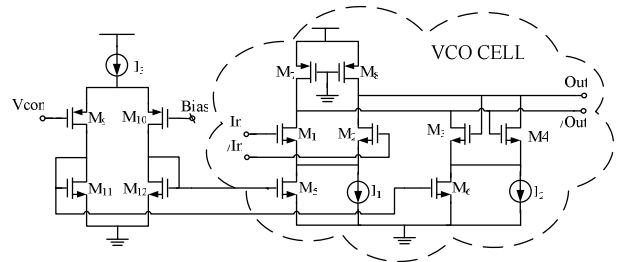


Fig. 15. Circuit diagram of a cell for the 4-stage ring VCO.

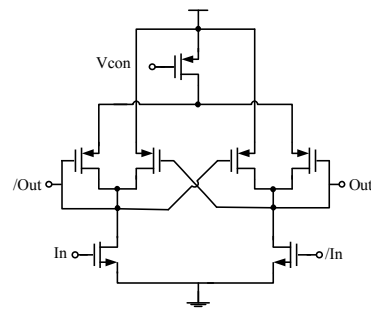


Fig. 16. Circuit diagram of a delay cell of the VCDL.

alleviate the conflict between the low voltage headroom and the sensitivity of the VCO.

The DLL consists of a half-rate PD, a V/I converter, a LF (loop filter) and 2-way VCDLs. The half-rate PD is identical to the one used in the half-rate PFD shown in Fig. 14. Because 2-way differential clocks are required for the half-rate PD, 2-way VCDLs are used. The circuit diagram of a delay cell of the VCDL is given in Fig. 15.

Fig. 17 shows the timing diagrams for a group within interface II shown in Fig. 12. From it, it can be found that 3-way high-speed data (CHin₀ ~ CHin₁) are demultiplexed into 6-way low-speed data (CHout₀ ~ CHin₂₁), and skews between channels can also be observed.

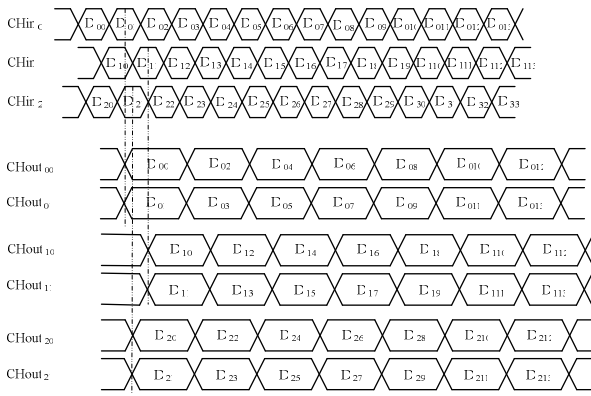


Fig. 17. Timing diagrams for a group within interface II shown in Fig. 12.

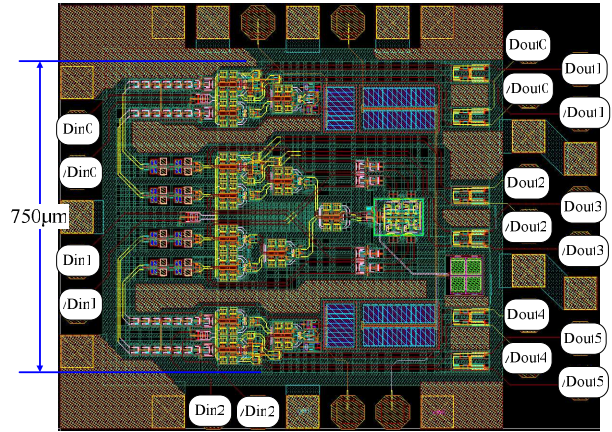


Fig. 19. Layout of a group for interface II.

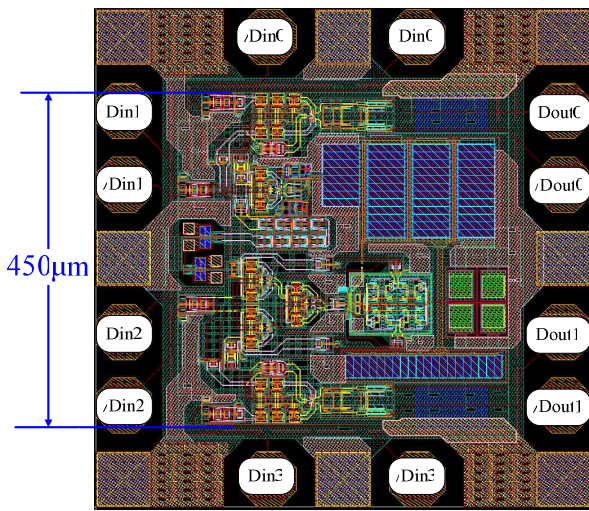


Fig. 18. Layout of a group for interface I.

V. LAYOUT DESIGN

In order to reduce the tape-out cost, only one group for each interface is designed and fabricated in a standard 0.18 μm CMOS technology. Compactness, isolation and match play a critical role in layout design in this work.

The layout of a group for interface I is shown in Fig. 18, which, including pads, occupies a die area of 673 $\mu\text{m} \times 667 \mu\text{m}$. The core width is only 450 μm , which is narrower than $4 \times 125 \mu\text{m}$, so the size specifications can be met. The arrangement of pads is just convenient for test and area reduction.

4-way 2.5 Gb/s differential data signals are fed into from the top, left and bottom sides, simultaneously, and 2-way 5Gb/s differential data are produced from the right side. Along the chip edges, ground and power pads are

interlaced with the ones for signals to reduce crosstalk and improve signal integrity.

No any pad is used for external tuning. The NMOS transistors instead of MIM capacitors are used for the large capacitor required by the PLL and DLLs. The layout be designed as compact as possible, and guarding strips or rings are placed between critical blocks or around the sensitive circuit blocks, e.g. VCO.

The layout of a group for interface II is shown in Fig. 19, which, including pads, occupies a die area of 1200 $\mu\text{m} \times 943 \mu\text{m}$. The core width is only 750 μm , which meet the size specification: 250 $\mu\text{m}/\text{ch}$. As indicated in Fig. 18, 3-way differential input data are fed into from the left side and the bottom side, and the 6-way differential input data are taken out from the two-column pads on the right side. All the layout design techniques mentioned above are also employed here.

VI. MEASUREMENT RESULTS

The fabricated IC for the interface I is measured after it is bonded on a microwave PCB, which is shown in Fig. 20. The high-speed differential traces on the PCB are strictly controlled to avoid imperfect issues, such as reflection, and their differential impedance are designed to 100 Ω .

Fig. 21 shows the measurement results of the IC for the interface I. The measured eye-diagram of one-channel data among the four-channel 2.5 Gb/s input data is shown in the upper half of Fig. 21(a). The measured two-channel 5 Gb/s output data eye-diagrams are shown in the lower half of Fig. 21(a) and Fig. 21(b), respectively.

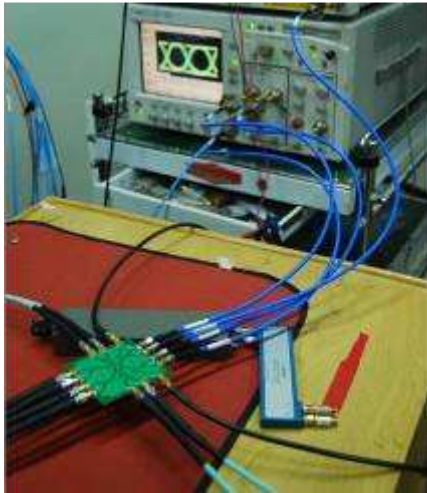


Fig. 20. The measurement setup for the fabricated IC for the interface I.

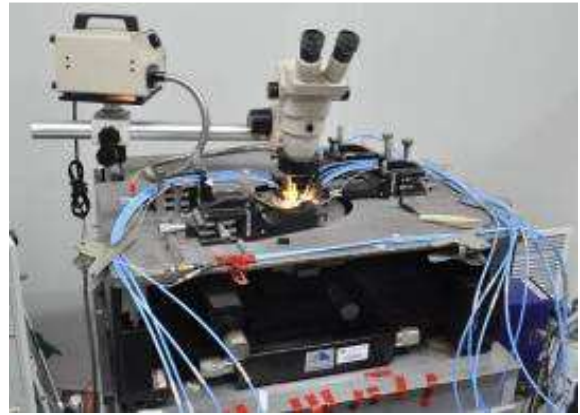
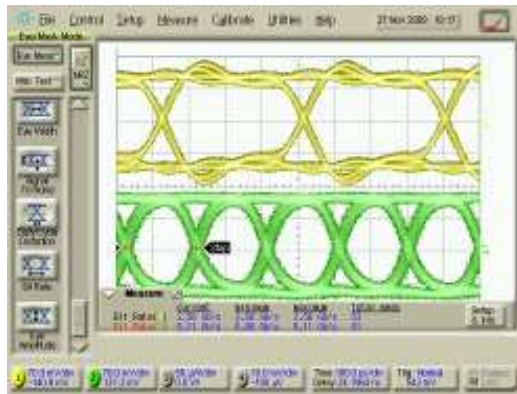
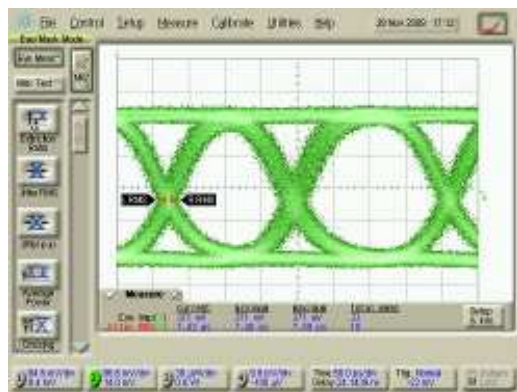


Fig. 22. The measurement setup for the fabricated IC for the interface II.



(a)



(b)

Fig. 21. Measured results of the IC for the interface I.

The former is derived from the MUX associated with a PLL, and the latter is from the one associated with a DLL.

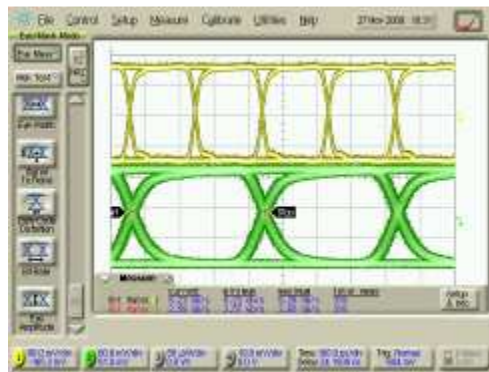
In order to avoid crosstalk between the two-column

bond-wires for the corresponding output pads, shown in Fig. 19, the measurement for the fabricated IC for the interface II is evaluated directly on a microwave probe station, which is shown in Fig. 22.

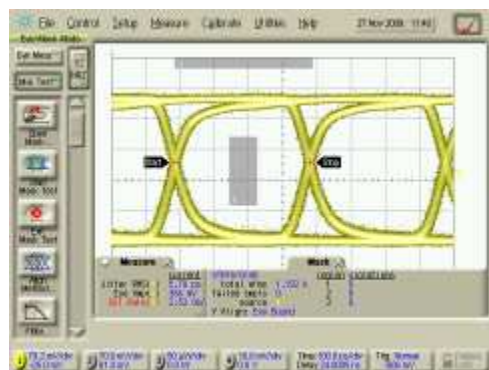
Fig. 23 shows the measurement results of the IC for the interface II. The measured eye-diagram of one-channel data among three-channel 5 Gb/s output data is shown in the upper half of Fig. 23(a). The measured eye-diagram of one-channel 2.5 Gb/s demultiplexed data from the PLL is shown in the lower half of Fig. 23(a). Fig. 23(b) and (c) show the measured one-channel output eye-diagrams from the other two DLLs, respectively.

VII. CONCLUSIONS

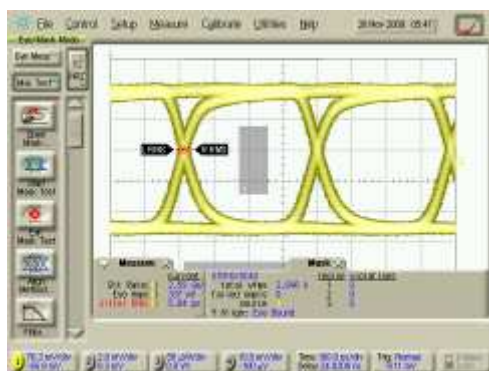
A high-speed multi-channel SERDES plays an important role in high-speed interconnect between ICs. In this paper, a 5 Gb/s/ch multi-channel SERDES is concentrated on, and based on extensive comparison and analysis, two novel clocking strategies are proposed for the SERDES. Both of the clocking strategies are based upon groups. The group within one strategy consists of a PLL, a DLL and two FPA techniques, and the group within the other strategy is composed of a PLL and two DLL. Each clocking strategy possesses distinct different characteristics for different application cases. Finally, two representative ICs for each group of SERDES are designed and fabricated in a standard 0.18 μm CMOS technology. Simulation and measurement results indicate that the two SERDES ICs can work properly accompanied with their corresponding clocking strategies.



(a)



(b)



(c)

Fig. 23. Measured results of the IC for the interface II.

ACKNOWLEDGMENTS

This work was supported by the China Postdoctoral Science Foundation (No. 2012M521126, 2012M521830), the National Natural Science Foundation of China (No. 61076073), the Scientific Research Funds of Nanjing University of Posts and Telecommunications, China (No. NY211016, NY211058), the Natural Science Foundation of Jiangsu Province (BK2012435) and State Key Laboratory of Millimeter Waves Open Research Program (K201223).

REFERENCES

- [1] Muller P, Leblebici Y. CMOS multichannel single-chip receivers for multi-gigabit optical data communications [M]. New York: Springer, 2007
- [2] Rabaey J M, Chandrakasan A, Nikolić B. Digital integrated circuits: a design perspective (second edition) [M]. London: Prentice Hall, 2003
- [3] Tao H, Shaeffer D K, Xu M, et al. 40-43-Gb/s OC-768 16:1 MUX/CMU chipset with SFI-5 compliance [J]. IEEE Journal of Solid-State Circuits, 2003, 38(12): 2169-2180
- [4] Kushiyama N, Ohshima S, Stark D, et al. A 500-Megabyte/s data-rate 4.5M DRAM [J]. IEEE Journal of Solid-State Circuits, 1993, 28(4): 490-498
- [5] Lau B, Chan Y F, Moncayo A, et al. A 2.6-GByte/s multipurpose chip-to-chip interface [J]. IEEE Journal of Solid-State Circuits, 1998, 33 (11): 1617-1626
- [6] Toshiro T, Takashi M, Yuji S, et al. 110-GB/s Simultaneous Bidirectional Transceiver Logic Synchronized with a System Clock [J]. IEEE Journal of Solid-State Circuits, 1999, 34(11): 1526-1533
- [7] Kim K, Choi J, Choi J. Design of 250Mb/s 10-channel CMOS optical receiver array for computer communication [C]. The first IEEE Asia Pacific Conference on ASICs, AP-ASIC'99, 1999: 29-32
- [8] Tang W, Plant D V. A 2.5-Gbps De-Skew Chip for Very Short Reach (VSR) Interconnects [C]. IEEE, LEOS, 2006: 823-824
- [9] Yeung E. Design of High-Performance and Low-Cost Parallel Links [D]: [A dissertation for Ph.D]. Stanford University, 2002
- [10] Chang K, Pamarti S, Kaviant K, et al. Clocking and circuit design for a parallel I/O on a first-generation CELL Processor [C]. IEEE ISSCC, 2005: 526-615
- [11] Sato T, Nishio Y, Sugano T, et al. A 5-GByte/s data-transfer scheme with bit-to-bit skew control for synchronous DRAM [J]. IEEE Journal of Solid-State Circuits, 1999, 34(5): 653-660
- [12] Yang K, Lin T, Ke Y. A scalable 32Gb/s parallel data transceiver with on-chip timing calibration circuits [C]. IEEE ISSCC Dig. Tech. Papers, 2000 (2): 258-259
- [13] Casper B, Jaussi J, Mahony F, et al. A 20Gb/s forwarded clock transceiver in 90nm CMOS [C].

- ISSCC Dig, Tech. Papers, 2006: 90-1
- [14] Casper B, Martin A, Jaussi J E, et al. An 8-Gb/s simultaneous bidirectional link with on-die waveform capture [J]. *IEEE Journal of Solid-State Circuits*, 2003, 38(12): 2111-2120
- [15] Tanahashi T, Kurisu K, Yamaguchi H, et al. A 2Gb/s 21CH low-latency transceiver circuit for inter-processor communication [C]. *IEEE ISSCC Dig. Tech., Papers*, 2001, (2): 60-61
- [16] Kohtaroh G, Hideki T, Hirotsuka T. A 2-byte parallel 1.25 Gb/s interconnect I/O interface with self-configurable link and plesiochronous clocking [J]. *FUJITSU Sci. Tech.*, 2000, 36(1): 82-90
- [17] Hossain M, Chan A. CMOS Oscillators for clock distribution and Injection-Locked Deskew [J]. *IEEE Journal of Solid-State Circuits*, 2009, 44(8): 2138-2153
- [18] Higashi H, Masaki S, Kibune M, et al. A 5-6.4-Gb/s 12-channel transceiver with pre-emphasis and equalization [J]. *IEEE Journal of Solid-State Circuits*, 2005, 40(4): 978-985
- [19] Kim J. A four-channel 3.125-Gb/s/ch CMOS serial/link transceiver with a mixed-mode adaptive equalizer [J]. *IEEE Journal of Solid-State Circuits*, 2005, 40(2): 462-471
- [20] Takauchi H. A CMOS multichannel 10-Gb/s transceiver [J]. *IEEE Journal of Solid-State Circuits*, 2003, 38(12): 2094-2100
- [21] Lee H R, Hwang M S, Lee B J, et al. A 1.2-V-only 900-mW 10 Gb Ethernet transceiver and XAUI Interface with robust VCO tuning technique [J]. *IEEE Journal of Solid-State Circuits*, 2005, 40(11): 2148-2158
- [22] Ishihara N, Fujita S, Togashi M, et al. 3.5-Gb/s×4-Ch Si bipolar LSI's for optical Interconnections [J]. *IEEE Journal of Solid-State Circuits*, 1995, 30(12): 1493-1501
- [23] Fukaishi M, Nakamura K, Heiuchi H, et al. A 20-Gb/s CMOS multichannel transmitter and receiver chip set for ultra-high-resolution digital displays [J]. *IEEE Journal of Solid-State Circuits*, 2000, 35(11):1611-1618
- [24] Tanaka K, Fukaishi M, Takeuchi M, et al. A 100Gb/s transceiver with GND-VDD common-mode receiver and flexible multi-channel aligner [C]. *IEEE Int. Solid-State Circuits Conf.* 2002, (2): 264-265
- [25] Landman P, Yee A L, Gu R, et al. A 62Gb/s backplane interconnect ASIC based on 3.1Gb/s serial-link technology [C]. *IEEE ISSCC Dig. Tech. Papers*, 2002, (2): 52-53
- [26] Miki Y. A 50-mW/ch 2.5/Gb/s/ch data recovery circuit for SFI-5 interface with digital eye-tracking [J]. *IEEE Journal of Solid-State Circuits*, 2004, 39(4): 613-621
- [27] Kromer C, Sialm G, Menolfi C, et al. A 25-Gb/s CDR in 90-nm CMOS for high-density interconnects [J]. *IEEE Journal of Solid-State Circuits*, 41(12): 2921-2929
- [28] Zhang D, Jin X, Cheung E, et al. A quad 3.125 Gb/s/channel transceiver with analog phase rotators [C]. *IEEE ISSCC Dig. Tech. Papers*, 2002, (2):70-71
- [29] Yang F, O'Neill J H, Inglis D, et al. A CMOS low-power multiple 2.5-3.125-Gb/s serial link macrocell for high IO bandwidth network ICs [J]. *IEEE Journal of Solid-State Circuits*, 2002, 37(12): 1813-1821
- [30] Yang F, O'Neil J, Larsson P, et al. A 1.5V 86mW/ch 8-Channel 622-3125Mb/s/ch CMOS SerDes Macrocell with selectable Mux/Demux Ratio [C]. *IEEE ISSCC, Dig. Tech. Papers*, 2002, 1: 68-69
- [31] Moon Y. A quad 0.6/3.2 Gb/s/channel interference-free CMOS transceiver for backplane serial link [J]. *IEEE Journal Solid-State Circuits*, 2004, 39(5): 795-803
- [32] Kaeriyama S, Mizuno M. A 10 Gb/s/ch 50 mW 120×120μm² clock and data recovery circuit [C]. *IEEE Int. Solid State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2003, (2): 70-71
- [33] Lee K H, Kim S J, Ahn G J, et al. A CMOS serial link for fully deplexed data communication [J]. *IEEE Journal of Solid-State Circuits*, 1995, 30(4): 353-364
- [34] Kim S, Lee K, Jeong D K, et al. An 800 Mbps multi-channel CMOS serial link with 3× oversampling [C]. *Proc. IEEE Custom Integrated Circuits Conf.*, 1995, (5): 451-454
- [35] David G M. Synchronization in digital system design [J]. *IEEE Journal of Selected Areas in Communications*, 1990, 8(8):1404-1419
- [36] Alioto M, Palumbo G. Model and Design of Bipolar and MOS Current-mode Logic: CML, ECL and SCL Digital Circuits [M]. The Netherlands:

Springer, 2005

- [37] Rein H M, Moller M. Design considerations for very-high-speed Si bipolar IC's operating up to 50 Gb/s [J]. *IEEE Journal of Solid-State Circuits*, 1996, 31(8):1076-1090
- [38] Pottbäcker A, Langman U, Schreiber H U. A Si bipolar phase and frequency detector IC for clock extraction up to 8 Gb/s [J]. *IEEE Journal of Solid-State Circuits*, 1992, 27(12): 1747-1751
- [39] Savoj J, Razavi B. A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase/frequency detector [J]. *IEEE Journal of Solid-State Circuits*, 2003, 38 (1): 13-21
- [40] Razavi B. *Design of integrated circuits for optical communications* [M]. New York: McGraw -Hill, 2003: 197-200



Changchun Zhang received the B.S. and M.S. degrees in communication engineering in Guilin University of Electronic Technology (GUET), Guilin, China, in 2003, and 2006, respectively, and Ph.D. degree in electrical engineering in Southeast

University, Nanjing, China, in 2010. Then, he worked as a post-doc researcher at Ewha Womans University, Seoul, South Korea. In December 2010, he joined Nanjing University of Posts and Telecommunications, Nanjing, China. Since February 2012, he has been working as a post-doc researcher in Nanjing Research Institute of Electronics Technology. His current research interests include IC designs on PON, RFID transceivers and other wireline transceivers.



Ming Li received the B.S. degree in Microwave Engineering from Chengdu Institute of Radio Engineering (now, University of Electronic Science and Technology of China), Chengdu, China, in 1982, the M.S. degree in Communications and Electronic

Systems from Nanjing Research Centre of Electronic Engineering in 1985. Since 1985, he has been involved in Signal Processing and IC Designs in Nanjing Research Institute of Electronics Technology, Nanjing, China, where he is currently a professorate senior engineer.



Zhi-Gong Wang was born in Henan, China. He received the M.-Eng. degree in radio engineering from Nanjing Institute of Technology (now, Southeast University), Nanjing, China, in 1981, and the Dr.-Ing.

degree in electronic engineering from Ruhr-University Bochum, Germany, in 1990. From 1977 to 1981, he worked on radio communication techniques and computer aided circuit designs in Nanjing Institute of Technology. During 1982-1984 he worked as a lecturer on semiconductor circuit techniques in Tongji-University, Shanghai. From 1985 to 1990, he worked on high-speed silicon bipolar circuit designs for multi-gigabit/s optic fiber communication in Ruhr-University Bochum, Germany. From Oct. 1990 to Sept. 1997, he has been with Fraunhofer-Institute of Applied Solid State Physics, Freiburg, Germany, working on high-speed GaAs ICs for optic-fiber data transmission and MMICs. Since Oct. 1997, he is full professor of Southeast University, Nanjing, China. He is the author or co-author of 20 books and more than 320 SCI/EI-cited papers, and inventor of 25 patents of China, Germany, Europe, USA, and Japan. He is Senior Member of IEEE since 1993, Chairman of the Advisory Committee of Electrical and Electronical Basic Courses of Chinese Universities. He is Guest Professor of more than 20 universities of China, Canada, and Australian. Recently, he is involving in IC design for optic-fiber transmission systems, for RF wireless, microwave, and millimeter-wave applications, and in micro-electronic systems for bio-medical applications.



Kuiyin Yin received the B.Sc. degree in 1999 and the Ph. D. degree in 2011, both from Xi'dian University, Xi'an China. She is currently a engineer with the signal Processing, Nanjing Research Institute of Electronics Technology. Her research

interests include image processing, SAR ATR. She has published over 30 research papers in these fields.



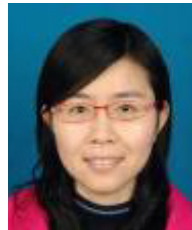
Qing Deng, male, 38, received Ph.D. from Southeast University, Nanjing, China. His current research interests include mixed-signal IC designs.



Yufeng Guo received the Ph.D. degree in Microelectronics from University of Electronic Science and Technology of China, Chengdu, China, in 2005, B.S. and M.S. degrees in material engineering from Sichuan University, Chengdu, China, in 1996 and 2001, respectively. From July 1996 to September 1998, he was an assistant engineer in Luoyang Ship Material Research Institute. He joined Nanjing University of Posts and Telecommunications, Nanjing, China, in 2005 where he is currently a Professor and Vice-Dean at the College of Electronic Science & Engineering, Director, and Center of Electrical & Electronic Experiment Teaching. He is also a consultant of Semiconductor Device Laboratory, Asia University, Taichung, Taiwan. He is currently leading a research group in power semiconductor devices, power integrated circuits and RF integrated circuits. His current research interests include the characterization, simulation and modeling of power semiconductor devices, RF devices, and Nano CMOS devices. He has published over 50 papers in technical journals and refereed conferences in the above areas.



Zhengjun Cao received the B.S. and M.S. degrees in electronic engineering from southeast university, Nanjing, China, in 2003 and 2006, respectively. From 2006 to 2008, he was with CR POWTECH where he worked on power management IC design. He worked as a hardware design engineer at HUAWEI Corporation in 2010. Since 2011, he has been with Magnichip Inc. and is focusing on high speed analog circuit design.



Leilei Liu received the Bachelor and PhD degrees in electromagnetic and microwave technology from Southeast University, Nanjing, P.R. China, in 2003 and 2009, respectively. She has been an Associate Professor at the Nanjing University of Posts and Communications since 2012. Her research interests are in the area of RF circuit and channel modeling.