A Spread Spectrum Clock Generator for DisplayPort 1.2 with a Hershey-Kiss Modulation Profile

Seung-Wook Oh*, Hyung-Min Park, Yong-Hwan Moon*, and Jin-Ku Kang***

Abstract—**This paper describes a spread spectrum clock generator (SSCG) circuit for DisplayPort 1.2 standard. A Hershey-Kiss modulation profile is generated by dual sigma-delta modulators. The structure generates various modulation slopes to shape a non-linear modulation profile. The proposed SSCG for DisplayPort 1.2 generates clock signals with 5000 ppm down spreading with a Hershey-Kiss modulation profile at three different clock frequencies, 540 MHz, 270 MHz and 162 MHz. The measured peak power reduction is about 15.6 dB at 540 MHz with the chip fabricated using a 0.13 μm CMOS technology.**

Index Terms—**SSCG, PLL, Hershey-Kiss modulation profile, sigma-delta modulator, DisplayPort**

I. INTRODUCTION

As the operation frequency of electronic devices increases, the electromagnetic interference (EMI) is generated and radiated to other devices. The spread spectrum clock generator (SSCG) is a PLL-based clock generator with an output frequency modulation to reduce the EMI. Amount of EMI reduction frequency varies on modulation profiles [1]. The linear modulation known as the triangular profile is commonly used because of its simplicity for implementation. With the triangular modulation profile, however, most of the harmonic energy is concentrated at the edges of the spectrum distribution. On the other hand, the Hershey-Kiss profile shows a non-linear modulation profile, but generates a more uniformed spectral spreading. Therefore a better EMI peak reduction could be achieved with Hershey-Kiss modulation profile [2]. Conventionally the Hershey-Kiss profile modulator is implemented by read-only-memory (ROM) [3]. In prior works the Hersey-Kiss profile or Hersey-Kiss-like profile was generated by look-up-table (LUT) [2], SRAM [3], piecewise linear modulation [4], and a Newton-Raphson method design [5]. Other various approaches are also reported [6-10].

This paper designed a SSCG for DisplayPort 1.2 with a non-linear Hershey-Kiss modulation profile. The modulation profile is generated using the dual sigma-delta modulators (SDM) [11]. Since the proposed modulators are based on the simple digital blocks, it can be modified to different applications and specifications. The DisplayPort 1.2 standard is a serial interface standard for display devices set by VESA. DisplayPort 1.2 serial interface should support three different data rates, which are 1.62 Gb/s, 2.7 Gb/s, and 5.4 Gb/s. Therefore the spread spectrum clock generator should support 162 MHz, 270 MHz, and 540 MHz clock modes for 10:1 multiplexing to a serial line. Also, the modulation frequency is defined as from 30 to 33 KHz with 0.5% down-spread frequency modulation [12].

The overview of the paper is as follows. Section II describes the main idea of the scheme and explains the design architecture of the proposed SSCG. Section III presents the circuit components in the SSCG. The measurement results are presented in Section IV and Section V concludes.

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* Inha University – Electronics, Incheon, Korea
** Hyundai-Autron, Seongnam, Gyeonggi-do, Korea
E-mail : jkang@inha.ac.kr

II. OPERATION AND ARCHITECTURE

1. Operation Principle

The Hershey-Kiss modulation profile generates a more uniform spectral spreading in SSCG application compared to a triangular profile. Fig. 1 shows a Hersey-Kiss modulation profile. The slope of the Hersey-Kiss modulation profile gradually changes from minimum to maximum value. Therefore, it is key point to make the gradual slope variation in order to generate Hershey-Kiss modulation profile. The underlying principle of this paper is to build a Hershey-Kiss modulation profile for DisplayPort 1.2 standard using the dual sigma-delta modulators. Fig. 2 shows a block diagram of the proposed SSCG circuit for DisplayPort 1.2. The modulators of proposed circuit for the Hersey-Kiss modulation profile consist of a slope modulator (SM) and a division modulator (DM). The slope of the Hershey-

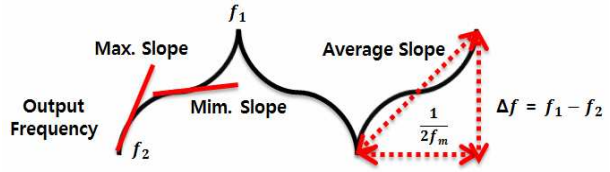


Fig. 1. Hershey-Kiss modulation profile with a slope change.

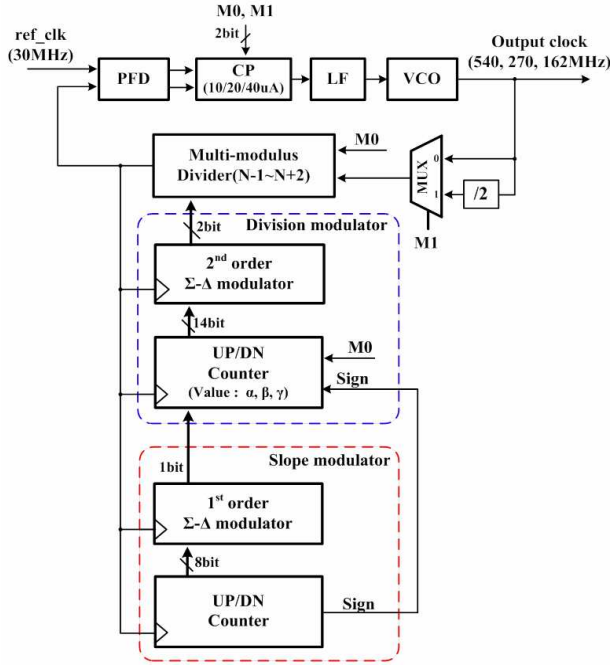


Fig. 2. The block diagram of the proposed SSCG.

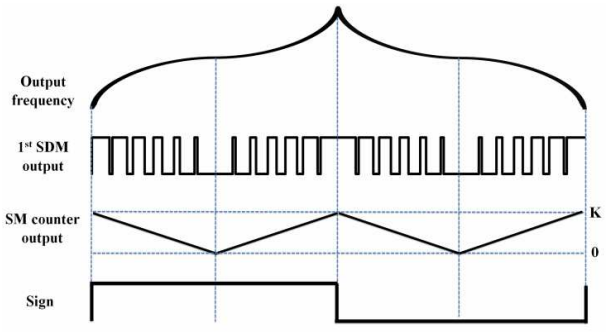


Fig. 3. The process of building the Hershey-Kiss modulation profile.

Kiss modulation profile repeats from the minimum and the maximum value, the derivative of its slope can be approximated to a triangular curve of SM counter output repeating itself with a twice of a modulation frequency. Fig. 3 shows the process of building the Hershey-Kiss modulation profile. The modulation profile has a very steep (maximum) slope at the 'K' value of SM counter output and a slow (minimum) slope at the '0' value of SM counter output. The 'K' is the largest number of the slope counter output will give the steepest slope. Though the Hershey-Kiss modulation profile is non-linear, the variation of its slope can be approximated and it has a periodicity as shown in Fig. 3. Therefore the Hershey-Kiss modulation profile can be generated by modulating its slope variation. The SM block provides gradual slope variation and sign (positive or negative) of profile slope to division modulator. The DM block provides a sigma-delta modulated division value for the PLL to multi-modulus divider (MMD). Therefore the final output of the dual sigma-delta modulators will give an approximated Hershey-Kiss profile as shown in the top of Fig. 3. Therefore the PLL has a Hershey-Kiss modulation profile on the VCO control voltage and the output clock of VCO is spectrum-spread.

2. ARCHITECTURE AND OPERATION

The proposed circuit has a fractional-N type PLL with a sigma-delta modulation. The circuit generates 540 MHz, 270 MHz, and 162 MHz clocks for DisplayPort 1.2 serial interface with a reference clock of 30 MHz. Each link symbol clock is controlled by external switch signals which are M1, M0. The M1 changes the PLL loop path. When the M1 and M0 are set at both '0', the

circuit operates in 162 MHz and when M0 is set at '1', it operates 270 MHz clock mode. When the M1 and M0 are set at both '1', the circuit operates in 540 MHz clock mode. At the 540 MHz clock mode, the output clock is divided by 2 before going into the loop. Each link symbol clock has different charge pump currents for its optimal loop bandwidth.

The SM block has a 1st order SDM and an 8-bit up/down counter. The SM block generates a 1-bit output (SM output) and a 'Sign' output. The 8-bit counter output represents the profile slope and the 'Sign' output indicates the sign of the profile slope (positive or negative). Since the 8-bit up/down counter (SM counter) is used, the slope variation resolution is the $1/2^8$. When the SSCG operates, the SM counter repetitively sweeps the output from 'K' to 0. Whenever the output value reaches at 'K', the 'Sign' signal switches its value from 0 to 1 and vice versa. The SM counter output shows a triangular profile as shown in Fig. 3. The SM block converts the counter value to a single bit randomized value. If the SM counter value goes up, the more 1's and the less 0's can be seen at the SM output. If the slope counter value goes down, the more 0's and the less 1's can be seen at the SM output. Therefore the average value of the SM output is equivalent to the SM counter output value or the absolute value of the profile slope. So, the average value of the SM output (AVS) can be expressed by Eq. (1) [11].

$$\mathrm{AVS} = \frac{\text{Output value of SM counter}}{2^8} \tag{1}$$

The half period of the triangular slope curve is a quarter of the modulation period as shown in Fig. 3. Therefore the modulation frequency (f_m) can be expressed by the reference clock frequency and the 'K' value as given in Eq. (2) [11].

$$f_m = \frac{\text{REF\_CLK frequency}}{4} \tag{2}$$

The DM block consists of a 2nd order sigma-delta modulator and a 14-bit up/down counter (DM counter). The DM block provides the division value for the PLL. The increment or the decrement of the DM counter output value is decided by the 'Sign' signal from the SM counter. And the counter step size is determined by 'M0' switch, which is related to the operating frequency range. When the 'Sign' output is '1', the DM counter goes up. And when the 'Sign' output is '0', the DM counter counts down. If the SM counter value goes to a upper value, the more number of '1' outputs from the SM are provided as the DM counter, which will have the large counting step size and translate to the more and more steep slope. If the SM counter value goes to a lower value, the more number of '0' outputs from the SM, which will have small counting step size and translate to the more and more gentle slope. When the output from the SM is '0', the output value of the DM counter is increased or decreased by α or β depending on the target output frequency. When the output value from the SM is '1', the output of the DM counter is increased or decreased by γ. Since the counting step size are set as $\gamma > \beta > \alpha$.

In our previous work [11], the counting step value of α and β is set 1 and 3 for proving the idea. In this work, we use three different counting steps as α, β and γ and their values are set to 0, 1 and 2, respectively. The reason using the three parameters in this paper is to meet the three target frequencies (540 MHz, 270 MHz, 162 MHz) for DisplayPort 1.2. Also, in order to make the smoother slope of Hershey-Kiss modulation profile and enhance the peak power reduction, the values of three counting step parameters are smaller than parameters in ref. [11].

When the M0 is set as '0', the DM is set for 162 MHz operation and the step size of the DM counter is derived from α and γ. As a result, the slope variation is related to the AVS, α and γ value when M0=0. The slope of the Hershey-Kiss profile can be expressed as

$$Slope\ of\ \ profile = (\gamma - \alpha) \times AVS + \alpha \quad \text{(M0=0)} \tag{3}$$

When the M0 is set as '1', the DM is set for 270 MHz or 540 MHz operation and the DM counter step values switch to β and γ. Thus the slope is given as

$$Slope\ of\ \ profile = (\gamma - \beta) \times AVS + \beta \quad \text{(M0=1)} \tag{4}$$

The average slope can be express as follows:

$$\text{Average slope} = \frac{D_{max} - D_{min}}{2 \times K} = \frac{\alpha + S_{max}}{2} \tag{5}$$

where K is the maximum value of the SM counter, and D_{max} and D_{min} are the maximum and minimum value of the DM counter output, respectively. And S_{max} is the maximum slope value and is given in Eq. (6) at each M0 value.

$$\begin{aligned} S_{max} &= (\gamma-\alpha)\times AVS_{max}+\alpha \\ &= (\gamma-\alpha)\times\frac{K}{2^8}+\alpha \quad (M0=0) \\ S_{max} &= (\gamma-\beta)\times AVS_{max}+\beta \\ &= (\gamma-\beta)\times\frac{K}{2^8}+\beta \quad (M0=1) \end{aligned} \tag{6}$$

The spread ratio (δ) can be expressed using the DM counter values as follows: [11]

$$\text{Spread ratio } (\delta) = \frac{D_{max}-D_{min}}{N\times 2^{14}+D_{max}} \tag{7}$$

Thus the spread ratio is controlled by the MMD and the DM counter. The values of N, D_{max}, and D_{min} can be determined by design parameters such as the reference clock, the targeted output frequency, and the spread ratio. Once the D_{max} and D_{min} are decided, the maximum value (K) of the SM counter can be derived from (3) to (5). For SSCG design of the three target frequencies, the maximum value of the SM counter is set as $248_{(10)}$. The values of N, D_{max} and D_{min} at 162 MHz mode are set as 5, $6554_{(10)}$ and $6111_{(10)}$, respectively, with a spread ratio of 5000 ppm with 30 MHz reference clock as defined in the DisplayPort 1.2 standard. When the modulator is set to 270 MHz clock mode, the DM counter operates based on β and γ values. And the values of N, D_{max} and D_{min} are set as 8, $16383_{(10)}$ and $15646_{(10)}$, respectively, at the 270 MHz. At the 540 MHz clock mode, N, D_{max} and D_{min} are set as same with 270 MHz clock mode except that 540 MHz output clock is divided by 2 before going into the loop.

III. CIRCUIT COMPONENTS

While the two sigma-delta modulators play the key role in realizing the Hershey-Kiss modulation profile, the design of a fractional-N PLL circuit is also very important. In this section, we describe circuit components for the proposed SSCG. Extra circuit design techniques to reduce spurious tones are not applied in the fractional-N PLL design [13]. In this paper a 3rd order loop filter was used for reducing spurious tones.

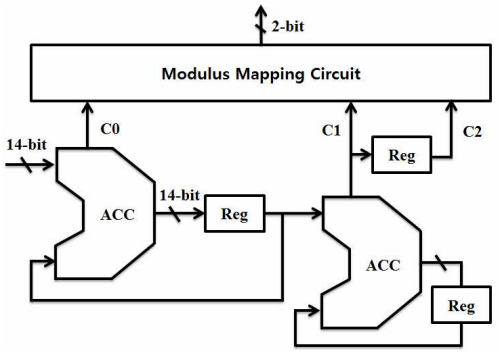


Fig. 4. Second-order MASH 1-1 sigma-delta modulator used in the division modulator.

1. Sigma-Delta Modulator

The proposed SSCG generates the Hershey-Kiss modulation profile with sigma-delta modulators. Using sigma-delta modulators, the number of control bits can be reduced while the quantization noise is pushed into the high frequency band. There is a trade-off between the order and the stability of the SDM. In this work, the MASH (multi-stage noise shaping) type SDM can be used to keep the stability regardless of the order. Fig. 4 shows the block diagram of the 2nd order MASH 1-1 sigma-delta modulator used in the proposed SSCG. It is formed by cascading two 1st order sigma-delta modulators.

2. PLL Blocks

The PLL circuit generates 540MHz, 270MHz, and 162 MHz clocks for the link symbol clock signals in the DisplayPort 1.2 serial interface. Fig. 5(a) shows the schematic of the VCO which consists of a 4-stage ring oscillator. The bias voltage generator can adjust V_{N_BIAS} dynamically by its own negative feedback loop to compensate the PVT variation. The self-biased technique can provide a wide frequency range and minimized supply /substrate noise. The delay cell of the VCO shown in Fig. 5(b) is a source-coupled pair with symmetric active loads for the better linearity of the VCO gain and wider swing [14].

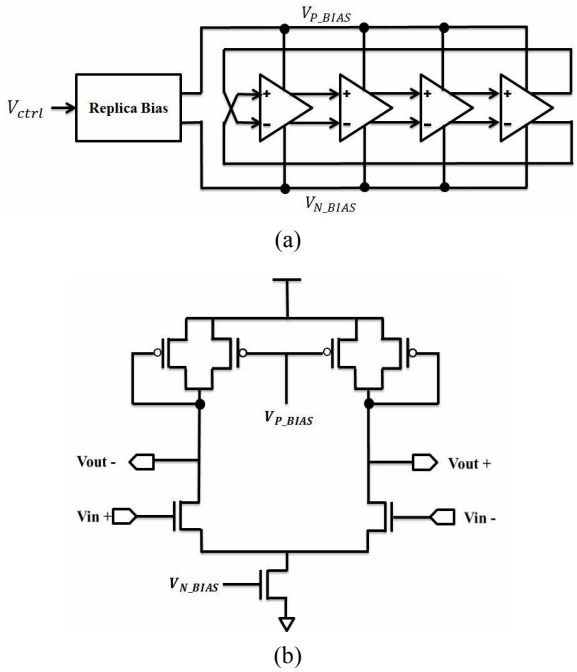


Fig. 5. Block diagram of the Voltage Controlled Oscillator (a) and its delay cell (b).

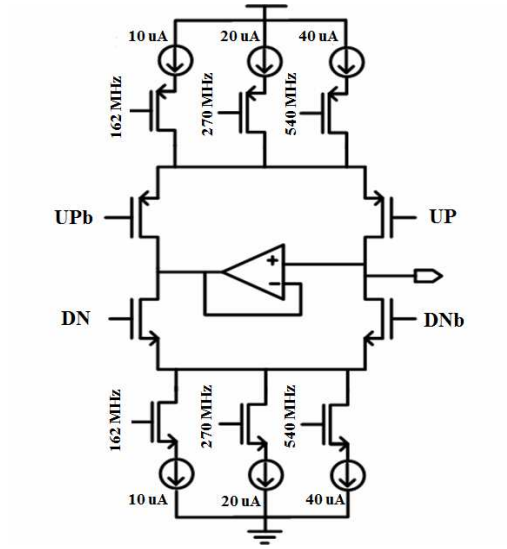


Fig. 6. Block diagram of the charge pump.

The schematic in Fig. 6 shows the charge pump circuit for the SSCG. A unity-gain buffer is used to clamp the terminal voltages of current sources during the zero-current pumping period. In this way, voltage glitches on the loop filter due to charge sharing can be eliminated [15]. Both the up and the down current can be either connected to the output or drained to a dummy reference voltage by the four switches. The relative timing of the charge pump switches is optimized to avoid glitches at the output node. And the proposed charge pump can switch to three current sources for 540 MHz, 270 MHz, and 162 MHz clocks. The reason we are using three different current source values is to meet the loop bandwidth because the N value of the MMD is difference according to the operating frequency. The loop bandwidth is set as 300 KHz to reduce the output jitter of the circuit.

The MMD block is designed by using Verilog coding and digital synthesis. The dividing ratio of the MMD is varied with N-1, N, N+1 and N+2. N value is to be decided for different clock frequencies. When the M0 signal is '0', the 'N' value is set to 5 for 162 MHz clock mode, thus the average division ratio is iterated between 5.373 and 5.4 according to output sequence of the DM. When the M0 signal is '1', the 'N' value of the MMD is set to 8 for 270 MHz and 540 MHz clock, and the average division ratio is iterated between 8.955 and 9.

IV. Measurement Results

The proposed SSCG with Hershey-Kiss modulation profile for DisplayPort 1.2 has been designed using CMOS 0.13-µm process. Fig. 7 shows the micrograph of the fabricated SSCG chip. Fig. 7(b) is the core layout of the proposed circuit. The area of the proposed circuit is 170 × 500 µm^2.

Fig. 8 shows the simulated modulation profile and the original Hershey-Kiss profile at 540 MHz clock mode with a PLL loop. It shows that the frequency of modulation profile has a frequency of 30.24 KHz. And the proposed scheme is well matched with the original Hershey-Kiss profile described in the Ref. [2]. We could not obtain the measured modulation profile since the pad for measuring the modulation profile was not drawn in

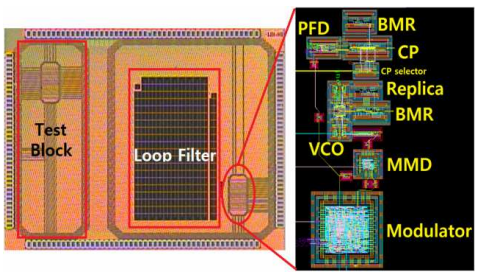


Fig. 7. (a) Chip microphoto, (b) the core blocks.

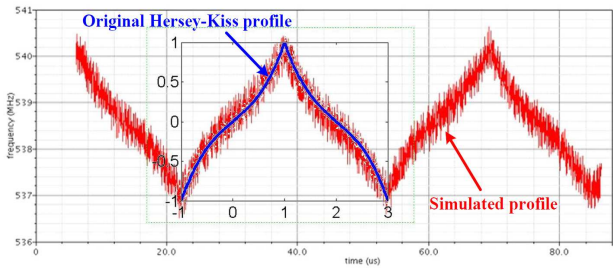
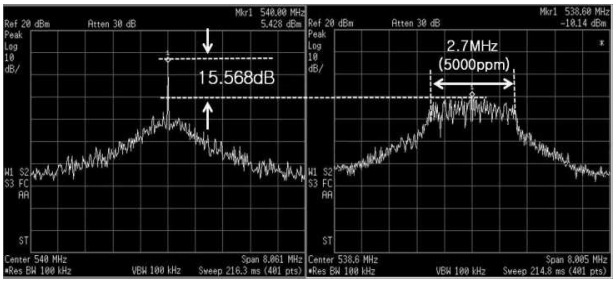
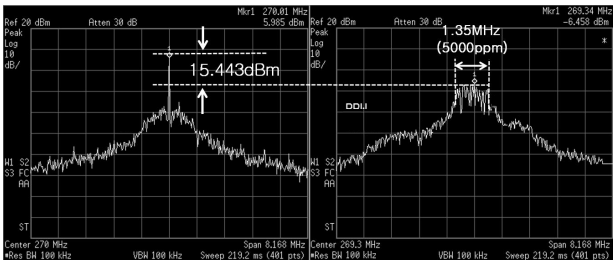


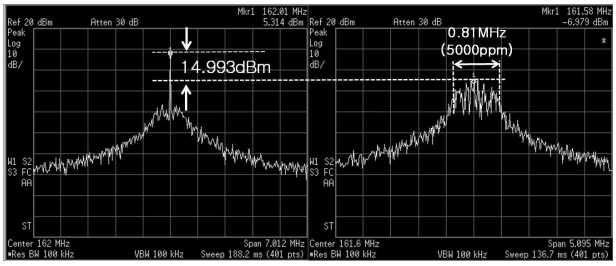
Fig. 8. Simulated modulation profile and the original Hershey-Kiss profile [2].



(a) 540 MHz



(b) 270 MHz

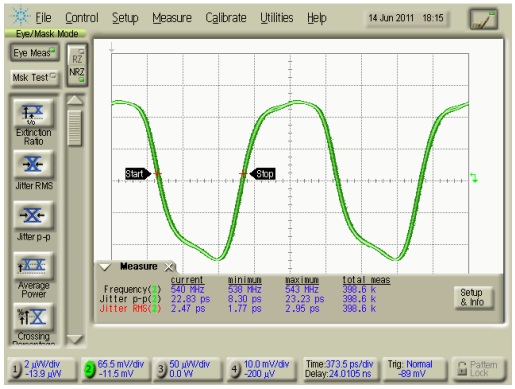


(c) 162 MHz

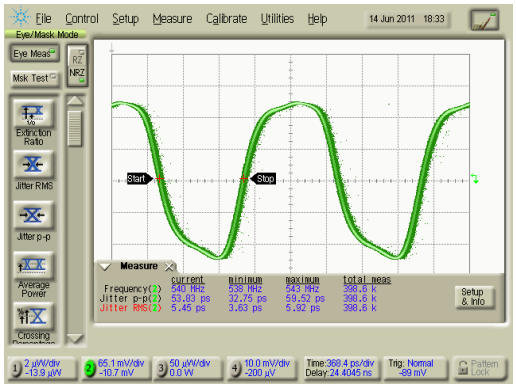
Fig. 9. Spectrum of SSC-off (left) and SSC-on (right) at three different rates.

the chip. However the modulation profile can be estimated indirectly from Fig. 9.

Fig. 9 shows the measured frequency spectrums at 540 MHz, 270 MHz, and 162 MHz output clock signals, respectively. The left measured spectrums are the single tone clock in the non-SSC mode and the right sides are the spectrum of the modulated output clock with the proposed profile. Fig. 9 is showing that the power



(a)



(b)

Fig. 10. Jitter Measurement of SSC-off (a) and SSC-on, (b) at 540 MHz.

reduction is about 15.6 dB measured with RBW (resolution bandwidth) of 100 KHz comparing to the non-SSC PLL, with 5000 ppm down spread ratio for 540 MHz clock mode. The power reduction of 15.4dB and 14.9 dB are achieved for 270 MHz and 162 MHz clock, respectively.

The jitter measurement of the circuit is shown Fig. 10. The maximum peak-to-peak jitter is 29.23 ps without SSC and 59.52 ps with SSC at 540 MHz. By using dual SDMs, the overlapped quantization noise shows up as output jitter. If the 3rd order SDM is used instead of 2nd SDM of division modulator, the output jitter characteristic could be improved.

Table 1 summarize the performance of the proposed SSCG. Table 2 shows the performance comparison with other designs. Our work has a lower maximum operating frequency of 540 MHz compared to other works operating typically 1.5 GHz. To substantiate our proposed approach with utilizing a Hershey-Kiss modulation profile in SSCG design, the most peak power reduction was achieved.

Table 1. SSCG performance summary

Process technology	0.13-μm CMOS
Supply voltage	1.2 V
Total chip area	1600 x 2000 μm^2 (w/ filter) 170 x 500 μm^2 (w/o filter)
Modulation profile	Hershey-Kiss Profile
Modulation frequency	30.24 KHz
Spreading ratio (down)	0.5 %
Output frequency	540 MHz / 270 MHz / 162 MHz
VCO gain	1.2 GHz/V
Loop bandwidth	300 KHz
Spectrum power reduction	15.6 dB (540 MHz) 15.4 dB (270 MHz) 14.9 dB (162 MHz)
Clock jitter (p-p) w/ SSC-on	59.5 ps (540 MHz) 62.4 ps (270 MHz) 63.9 ps (162 MHz)
Clock jitter (p-p) w/ SSC-off	23.2 ps (540 MHz) 25.2 ps (270 MHz) 24.4 ps(162 MHz)
Power consumption with output buffer	12.0 mW (540 MHz) 11.5 mW (270 MHz) 10.3 mW(162 MHz)

Table 2. SSCG performance comparison

	[3]	[4]	[6]	[16]	[17]	[18]	[19]	This Work
Process	65 nm	0.18 μm	0.18 μm	0.15 μn	0.15 μm	0.18 μm	0.13 μm	0.13 μm
*Operating frequency	1.25 GHz	1.5 GHz	1.5 GHz	1.5 GHz	1.05 GHz	1.5 GHz	3 GHz	0.54 GHz
Modulation Profile	Hershey-Kiss	Piecewise-linear	Tri-angular	Tri-angular	Tri-angular	Tri-angular	Chaotic PAM	Hershey-Kiss
Modulation Ratio	6 %	0.5 %	0.5 %	0.5 %	0.5 %	0.5 %	0.5 %	0.5 %
Modulation frequency	100 KHz	33 KHz	30.1 KHz	31.1 KHz	31.6 KHz	33 KHz	33 KHz	30.24 KHz
Peak Power Reduction (RBW = 100 KHz)	7.4 dB (RBW=1 MHz)	14.2 dB	9.8 dB	10 dB	5.43 dB	14.77 dB	14 dB	15.6 dB
Jitter (rms)	NA	**3.77 ps	3.2 ps	8.1 ps	NA	5.55	5.4 ps	5.92 ps
Jitter (peak-peak)	**93ps	**27.88ps	58.3 ps	NA	NA	34.2 ps	NA	59.6 ps
Power Consumption	44 mW	40 mW	NA	54 mW	NA	34.2mW	14.7 mW	12 mW
Chip-Area	0.044 mm^2	0.49 mm^2	1.645 mm^2	0.42 mm^2	5.72 mm^2	0.17 mm^2	0.21 mm^2	0.085 mm^2

*Measured frequency ** Measured with SSC-off

V. CONCLUSIONS

An SSCG circuit generating a Hershey-Kiss modulation profile using two sigma-delta modulators is designed for the DisplayPort 1.2 standard. Since the modulator is implemented by digital blocks, it can be modified upon different applications and spectrum spreading parameters. The circuit is implemented using 0.13 μm CMOS technology and the measured results show that the maximum peak power reduction of 15.6 dB at 540 MHz with 5000 ppm down spreading for the DisplayPort 1.2 standard.

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Seung-Wook Oh received the BS degree in electronics engineering from Inha University, Incheon, Ref. of Korea, in 2011 and is currently working toward the M.S. degree in electronic engineering. His research interests include high-speed interface IC, PLL, SSCG and analog/digital mixed circuit design.

Hyung-Min Park received the BS and MS in electronics engineering from Inha University, Incheon, Rep. of Korea, in 2009 and 2011, respectively. Since 2011, he has been with Hyundai Autron Co., Seongnam, Ref. of Korea. His research interests include high-speed clock generation and VLSI circuit design.

Yong-Hwan Moon received the BS and MS in electrical engineering in 2002 and 2004, respectively, from Inha University, Incheon, Rep. of Korea. He is currently working toward the PhD in the Department of Electrical and Engineering, Inha University. His research interests include high-speed interface and clock and data recovery circuits.

Jin-Ku Kang received his PhD in electrical engineering from North Carolina State University in 1996. From 1983 to 1988, he worked at Samsung Electronics, Inc., Korea. From 1996 to 1997, he was with Intel as a senior design engineer. Since 1997, he has been a professor in the School of Electronics Engineering, Inha University, Rep. of Korea. His research interests are high-speed CMOS VLSI design, mixed-mode IC design, and high speed serial interface design.