

Experimental Study on Conducted EMI Mitigation in SMPS using a Novel Spread Spectrum Technique

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Abstract

Switched mode power supplies (SMPS) are power electronic circuits extensively used in a wide range of applications. High frequency switching operation of SMPS causes electromagnetic emissions and has the potential to interfere with system operation, which in turn has an impact on system performance. This makes electromagnetic compatibility (EMC) an important concern. In this paper, a new and simple spread spectrum technique is proposed by modulating chaotic pulse position modulation (CPPM) and pulse width modulation (PWM). The resulting CPWM is implemented to reduce the conducted EMI in SMPS. The proposed method is found to be effective in reducing conduction EMI. The effectiveness and simplicity of the proposed method on spreading those dominating frequencies is compared to the EMI mitigation technique using an external chaotic generator. Finally, the levels of conductive EMI with standard PWM, CPWM with an external chaos generator and the proposed method are experimentally verified to comply with the CISPR 22A regulations. The results confirm the effectiveness of the proposed method.

Key words: Chaotic pulse position modulation, Chaotic pulse width modulation, EMC, EMI, External chaos generator, SMPS

I. INTRODUCTION

Switched mode power supplies (SMPS) are widely used in various sectors such as communications, control and military applications. In terms of electromagnetic interference (EMI), SMPS have always been a serious concern due to their unwanted radiations. The increased switching frequency, together with the increased current and voltage slew rates, di/dt and dv/dt , have detrimental effects on the electromagnetic compatibility (EMC) performance of these power supplies. Commercial power supplies cannot be put on the market until certain EMC regulations are met. In addition, SMPS must provide the desired electrical functionality, in order to meet the international standards of electromagnetic compatibility (EMC) by reducing conducted and radiated emissions [1].

The dc-dc conversion in switched mode converters is based on the pulse width modulation (PWM) technique. Under the steady state operation of SMPS, the constant switching frequency results in undesirable harmonics at multiples of the switching frequency in the power spectrum of the output

signal. These undesirable noises are often associated with conducted electromagnetic interference emissions [2]. There are several methods available in the literature for reducing EMI such as filter methods, soft switching methods, random modulation methods, chaotic modulation methods, etc [3]-[8]. With the random switching scheme, the harmonic power concentration in the frequency domain is reduced and the peak level of the power spectral density (PSD) becomes less than that of classical PWM. The discrete harmonics are significantly reduced and the harmonic power is spread over a continuous noise spectrum of insignificant magnitude [9].

On the other hand, operating a system in chaos, where the ripple waveform becomes aperiodic, has the effect of spectral spreading without any additional circuitry which can be effectively used in countering the EMI problem [10]. Two popular methods have been suggested in the literature to achieve the suppression of EMI by chaos technology [11]. The first method is the parameter-controlling method [12]-[15]. The switching converters are operated under the chaos state by controlling the various parameters of the system. The problem with this method is that it is difficult to achieve a satisfying design. The second method is the variable frequency modulation method [16]. It mainly utilizes the broadband nature of the clock signals generated by the chaotic system to reduce EMI. Some methods for spreading the spectrum through chaotic modulation have been proposed

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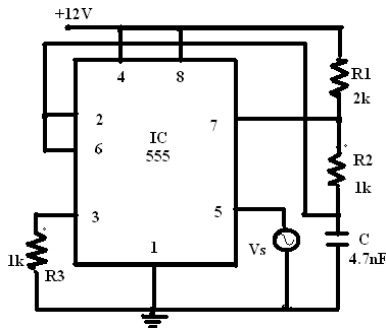
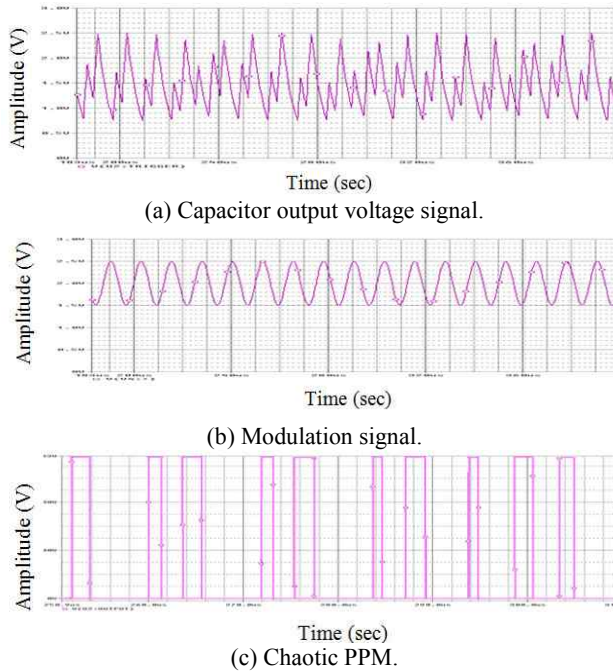


Fig. 1. CPPM generation.

Fig. 2. Generated chaotic PPM for $C=0.0047 \mu\text{F}$.

in [17]-[21].

Chua's circuit has been implemented as a chaos generator in [22], [23]. In these methods, chaos is incorporated into the circuit with an external chaos generator circuit. However, [24] reported some inherent shortcomings of chaos like reduced efficiency due to an increased ripple and a higher emission floor. A common limitation of all these methods is that once a converter has been designed for a particular EMC norm, it cannot be tuned to satisfy some other norm or have to be overdesigned [25]. Similar methods for spreading the spectrum through chaotic modulation have been proposed in [26], [27] but they use DSP boards to obtain chaotic waveforms through software programming.

This paper introduces a novel and easy approach for reducing the electromagnetic interference in SMPS using chaos, based on the approaches of [28]-[31]. In the proposed scheme, the converter is designed to work in a regular periodic regime, with a low ripple. The feedback PWM is then modulated with chaotic PPM (CPPM) produced by a

555 timer. This generates chaotic PWM that makes the converter switching chaotic, which results in spectrum spreading and a consequent reduction of the spectral peaks.

II. CHAOTIC PULSE POSITION MODULATION

Pulse position modulation (PPM) is a pulse modulation technique that uses pulses of uniform height and width but displaced in time from some base position according to the amplitude of the signal at the instant of sampling. In this study, an LM555 timer has been used to generate CPPM. The timer is connected for stable operation, as shown in Fig.1, with the modulating signal V_s applied to the control voltage terminal. The signal V_s is a sinusoidal voltage generated by a sinusoidal voltage generator. The pulse position varies with the modulating signal since the threshold voltage and hence the time delay is varied.

The capacitor value has been calculated as follows:

$$C = 1.44 / (R_1 + R_2)f_o \quad (1)$$

where f_o is the frequency of the oscillation. It has been found experimentally that when f_o is less than the frequency of the modulating signal, the output of the LM555 timer is a standard PPM signal. However, when f_o is equal to or greater than the frequency of the modulating signal, the PPM becomes chaotic. Hence by varying the capacitor value, a chaotic PPM is obtained. Here $C=0.0047 \mu\text{F}$ was chosen for generating the chaotic PPM.

Fig. 2 shows the waveforms generated for a sinusoidal wave modulation signal.

III. FORWARD CONVERTER

Forward converters are a popular SMPS used for producing isolated and controlled dc voltages from an unregulated dc supply.

A. Forward Converter with the Standard PWM Technique

Fig. 3 shows the block diagram of a voltage-mode controlled forward converter. In this circuit, the switch is controlled by load voltage feedback. In operation, the differential amplifier compares the voltage across the load resistor with the reference voltage. The output of this amplifier is compared with the ramp voltage (carrier), resulting in PWM pulses that determine the state of the switching action of the converter.

B. Forward Converter with CPWM Generated by An External Chaos Generator

Figure 4 shows a block diagram of a forward converter with an external chaotic generator added to it. The generator circuit chosen is Chua's oscillator [32].

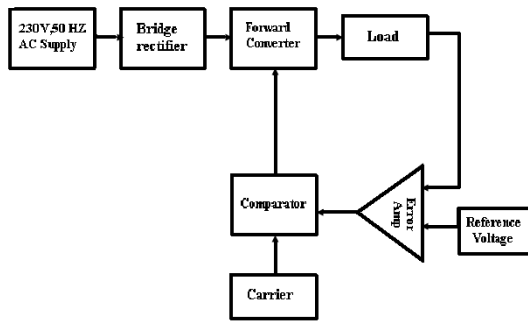


Fig. 3. Forward converter with conventional PWM technique.

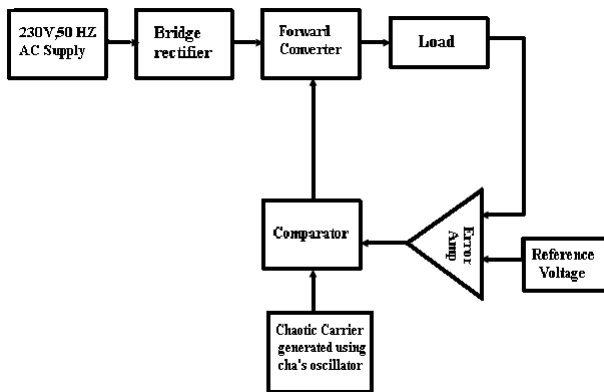


Fig. 4. Forward converter with CPWM generated by external chaotic generator.

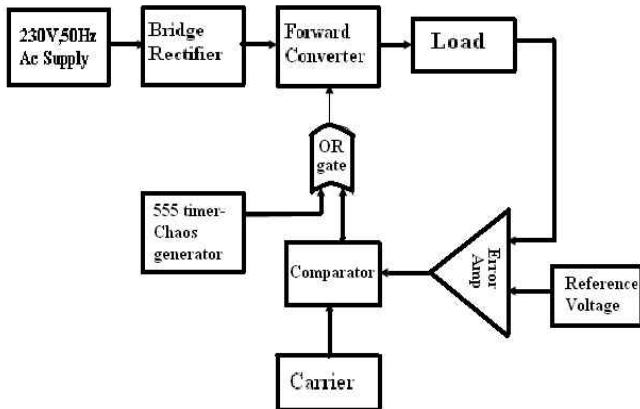


Fig. 5. Forward converter with proposed technique.

C. Forward Converter with CPWM Generated by the Proposed Method

To generate chaotic PWM for EMI reduction with the proposed method, a 555 timer and an OR gate are included in the conventional forward converter, as shown in Fig.5.

The output of the comparator is a PWM signal. This signal together with the chaotic PPM signal produced by the 555 timer are given as inputs to the OR gate. The output of the OR gate is a chaotic PWM pulse. This pulse in turn operates the converter chaotically. The PWM output of the comparator,

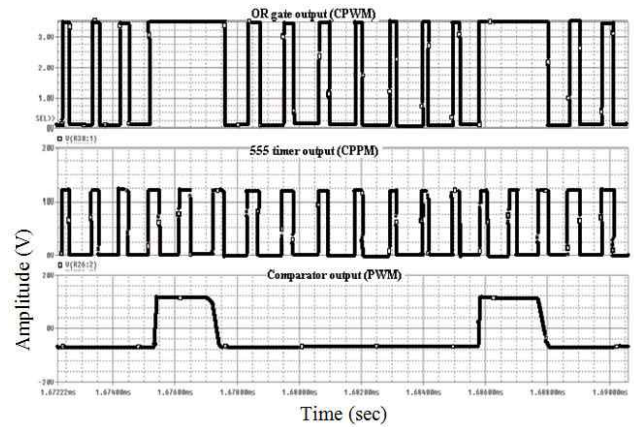


Fig. 6. Generation of chaotic PWM pulses.

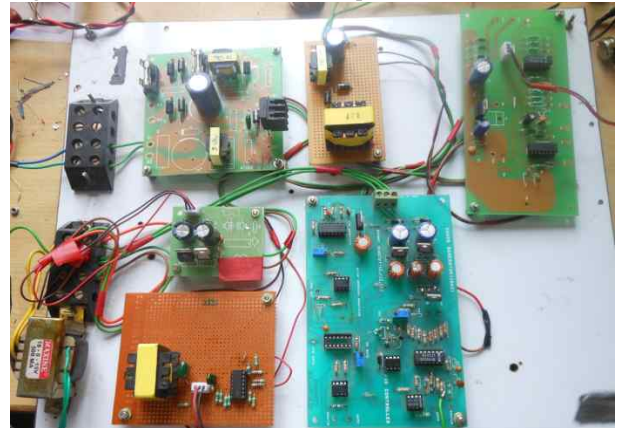


Fig. 7. Experimental prototype of forward converter with external chaos generator circuit.

the PPM output of the 555 timer and the chaotic PWM output of the OR gate are shown in Fig.6.

IV. MEASURED RESULTS - EMI REDUCTION IN SMPS

A forward converter has been designed, built and tested for chaos and EMI reduction. The power of the converter is 65W, the input ac voltage is 220V 50 Hz, the rectified dc input is 160 V, the dc output is 19.5V 3.5 A and the switching frequency is 100 kHz. The converter is designed to operate periodically under various system parameter disturbances. It has been found that the converter output is constantly periodic when the input voltage is varied from 140 V to 180 V.

Fig.7 shows an experimental prototype of a forward converter embedded with an external chaos generator. The converter is found to operate chaotically for an input voltage in the range of 140 V to 180 V.

Fig. 8 shows an experimental prototype of the forward converter with the implementation of the proposed CPWM method. With the proposed method for generating and applying chaotic PWM to the switch, the converter is found to operate chaotically for an input voltage in the range of 140 V to 180 V.

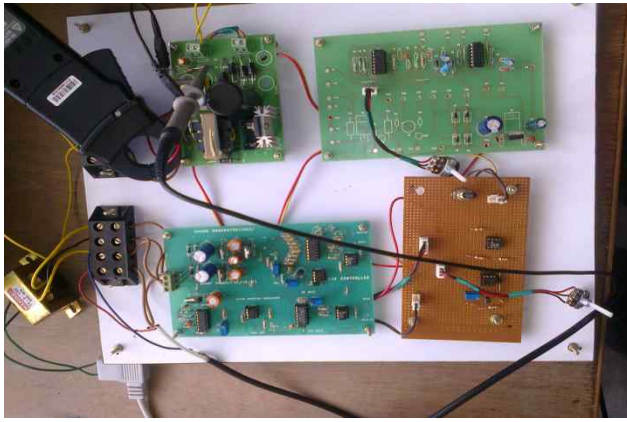
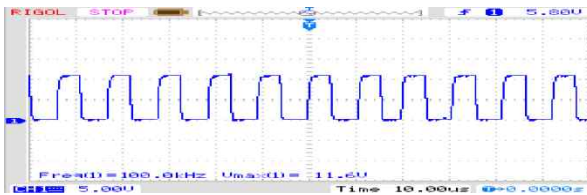
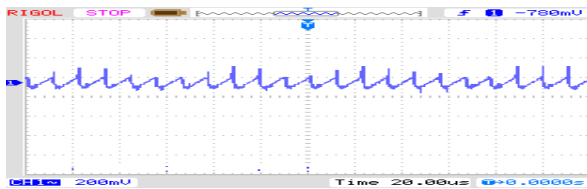


Fig. 8. Experimental prototype of forward converter with proposed CPWM.



(a) Gate pulse waveform.



(b) Capacitor voltage waveform.

Fig. 9. Measured waveforms (Periodic for both $V_{in} = 140V$ and $V_{in} = 180 V$) with PWM modulation.

A. Converter with PWM Modulation - Measured Results

The measured waveforms for the forward converter with the standard PWM method are obtained and the results are shown in Fig. 9.

It has been found that the gate pulses and the output voltage are periodic over an input voltage in the range of 140 V and 180 V.

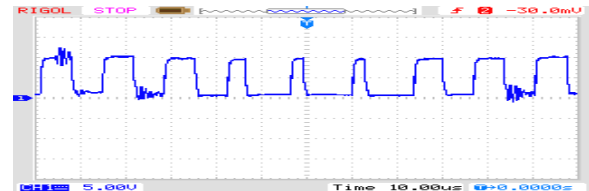
B. Converter with CPWM generated by an External Chaos Generator Circuit - Measured Results

The measured waveforms for the forward converter with the addition of an external chaotic generator circuit are shown in Fig. 10.

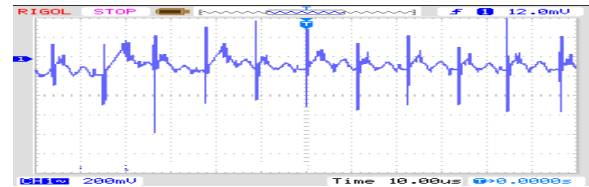
The gate pulses and the output voltage are chaotic over an input voltage in the range of 140 V and 180 V, with the CPWM generated by the external chaos generator, as shown in Fig. 10.

C. Converter with the Proposed Simple CPWM Generation Technique - Measured Results

Similarly, the measured waveforms for the forward

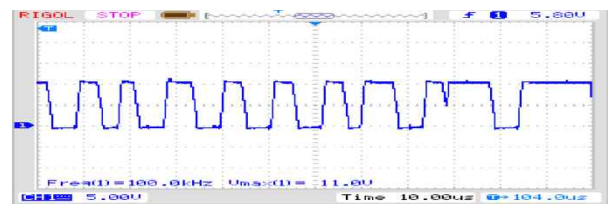


(a) Gate pulse waveform.

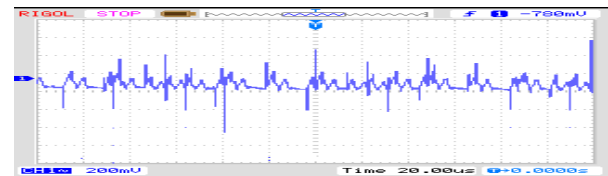


(b) Capacitor voltage waveform.

Fig. 10. Measured waveforms (chaotic for both $V_{in} = 140 V$ and $V_{in} = 180 V$) with CPWM generated by external chaos generator.



(a) Gate pulse waveform.



(b) Capacitor voltage waveform.

Fig. 11. Measured capacitor voltage waveform (chaotic for both $V_{in} = 140 V$ and $V_{in} = 180 V$) with CPWM generated by proposed method.

converter with the proposed simplified CPWM method are obtained and the results are as shown in Fig. 11.

It can be seen in Fig. 11, that the gate pulses and the output voltage are chaotic over an input voltage in the range of 140 V and 180 V, with the proposed method.

The power density spectrums of the output voltage under periodic operation of the converter with the standard PWM, the spectrum under chaotic operation of the converter (by parameter modulation) with the standard PWM and the spectrum under chaotic operation with the external chaos generator are compared in Fig. 12 and Fig. 13, respectively.

In Fig. 12, the periodic spectrum under PWM is compared with the chaotic spectrum under PWM. The chaotic spectrum in Fig. 12 is obtained by operating the converter in chaos, while varying the load resistance. It can be seen in Fig. 12 that, the height of the peaks is reduced to a considerable extent, when the converter is operated in the chaotic state rather than the periodic state. The power is densely concentrated at the fundamental frequency of 100 kHz and its harmonics during periodic operation whereas the spectrum is continuous and

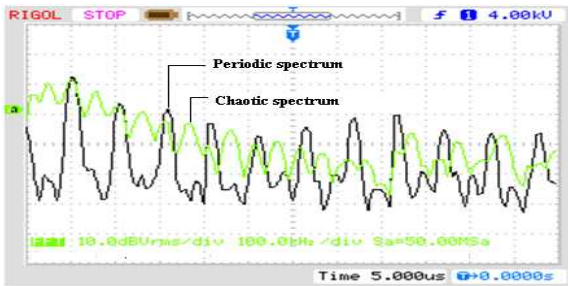


Fig. 12. Comparison of periodic and chaotic spectra under PWM modulation.

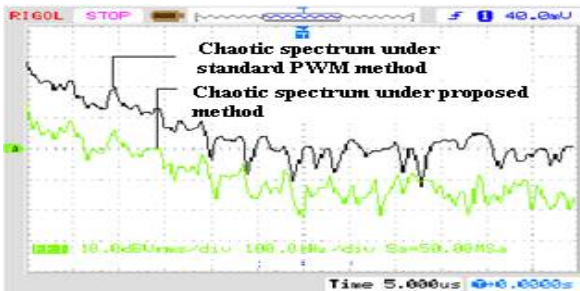


Fig. 13. Comparison of chaotic spectrum (with parameter modulation) under PWM and chaotic spectrum under CPWM generated by the proposed method.

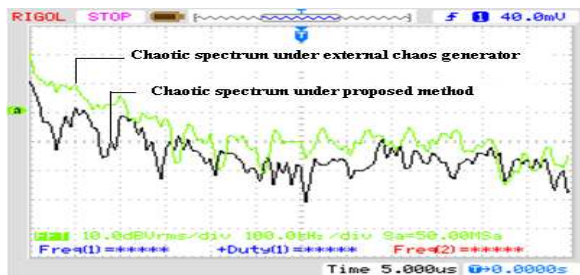


Fig. 14. Comparison of chaotic spectrum with external chaotic generator and chaotic spectrum with proposed method.

the amplitudes of the spectral peaks are reduced during chaotic operation. This is because the total emitted energy is spread over a wider frequency range thereby reducing the peak emissions. The plot shows that operating the system in chaotic mode is effective at lowering the peak levels of both fundamental and harmonic peaks.

Fig. 13 shows the comparison of the FFTs between the chaotic operation of the converter under the standard PWM method and the periodic and the chaotic operation of the converter with the proposed simplified CPWM method. It is found that the emission level for the proposed method is comparatively lower than that of the converter operating in chaos under the standard PWM method.

In addition, as seen in Fig.14, the level of the emission peaks with the proposed simple CPWM method is found to be comparatively lower than that of the peak emissions with the external chaos generator.

Hence it is experimentally verified from the spectral analysis that the proposed CPWM effectively suppresses the peaky EMI.

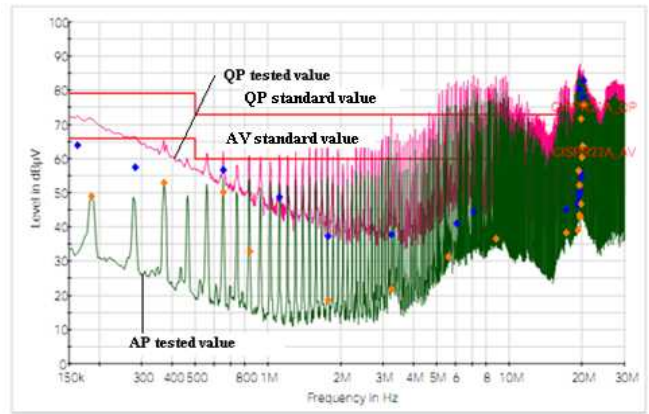


Fig. 15. Conduction EMI test results under standard PWM method.

V. EMI TEST ANALYSIS

The conducted EMI measurements are carried out with a 150 kHz to 30 MHz line impedance stabilization network (LISN) and an EMI analyzer. The EMI test criterion is CISPR 22A. Practical measurements of the conducted EMI of a 65W dc-dc forward converter are given in Fig.15, Fig.16 and Fig.17, respectively. The top standard line is the quasi-peak (QP) value limit and the bottom standard line is the average value (AV) limit. QP is used to quantify the annoyance factor of the signal by weighing its repetition rate in addition to its frequency and amplitude. It is measured by placing the signal in the EMI receiver and performing a remeasure using the detector.

The converter qualifies if the measured quasi-peak values are below the quasi-peak limit and the average limit, and the average values are below the average limit.

As seen in Fig.15, under the conventional PWM method, the noise energy exceeds the QP and AV limits after the 5M frequency point. The EMI test of the SMPS is disqualified under the constant PWM scheme.

In Fig.16, it can be seen that the noise energy gets reduced to below the QP and AV limits with the application of the external chaotic generator.

Under the proposed CPWM method, as shown in Fig.17, the noise energy is spread over a wide frequency range, and the peaky emissions are found to be a lot less when compared with Fig. 15 and Fig.16. The QP and AV tested values are all within their limits, and the SMPS is found to be qualified. A reduction of more than 20dB is noticed in the envelope of the spectrum. This demonstrates the effectiveness of using the proposed CPWM scheme in suppressing the EMI of the SMPS.

VI. CONCLUSION

A novel and simple method of CPWM generation and its implementation to SMPS for EMI reduction, is discussed in this paper. The method is compared with the CPWM

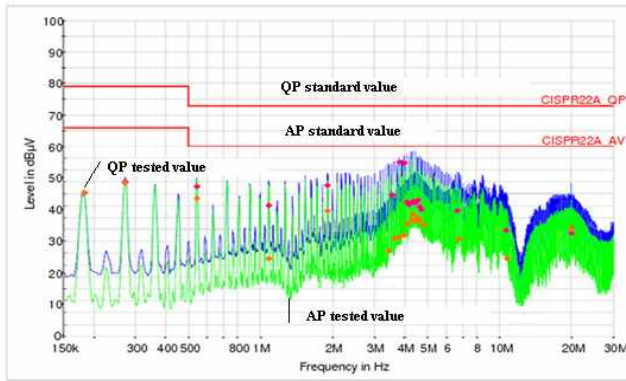


Fig. 16. Conduction EMI test results with external chaotic generator circuit.

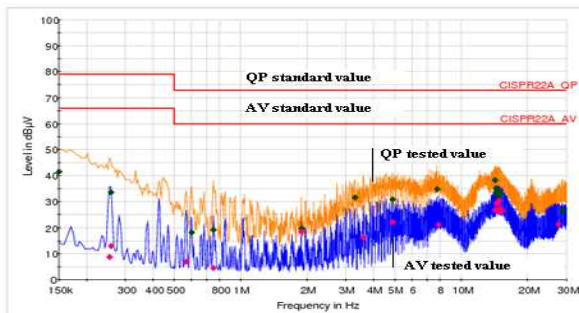


Fig. 17. Conduction EMI test results under the proposed method.

generated by an external chaos generator and it is found to have advantages like low cost, compactness and ease of design. The peaky emissions are found to be comparatively less with this approach. Measured results validate the suitability of the proposed method. Finally, the levels of conductive EMI for the SMPS are experimentally verified to comply with the CISPR 22A regulations and the results confirm the effectiveness of the proposed method.

APPENDIX

SMPS design specifications

Input voltage (min)	140 V DC
Input voltage (max)	180 V DC
Input voltage(nominal) V_{in}	160 V DC
Output voltage V_o	19.5 V DC
Output current I_o	3.5 A
Max output voltage ripple (1% of V_o)	0.195 V
Max output current ripple (20% of I_o)	0.7 A
Output power P_o	68.25 W
Peak input current ($1.2P_o / (V_{in} * \eta * D_{max})$)	1.42 A

Output resistance R_L	5.6 Ω
Switching frequency	100 kHz
Input current	0.53 A
Max. duty ratio D_{max}	0.45
Max.flux density	0.3 T
Change in flux density	0.3 T
Max.current density	450 A/cm ²
Winding factor due to isolation	0.5
Winding factor between primary and secondary	0.4
Inductor winding factor	0.7

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power quality.

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