

Effects of Mesh Planes on Signal Integrity in Glass Ceramic Packages for High-Performance Servers

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Abstract

This paper discusses effects of mesh planes on signal integrity in high-speed glass ceramic packages. One of serious signal integrity issues in high-speed glass ceramic packages is high far-end (FE) noise coupling between signal interconnects. Based on signal integrity analysis, a methodology is presented for reducing far-end noise coupling between signal interconnects in high-speed glass ceramic modules. This methodology employing power/ground mesh planes with alternating spacing and a via-connected coplanar-type shield (VCS) structure is suggested to minimize far-end noise coupling between signal lines in high-speed glass ceramic packages. Optimized interconnect structure based on this methodology has demonstrated that the saturated far-end noise coupling of a typical interconnect structure in glass ceramic modules could be reduced significantly by 73.3 %.

I. Introduction

Over the last two decades, the scaling of the CMOS transistor has enabled the design of microprocessors operating at multigigahertz frequencies. This trend, based on the International Technology Roadmap on Semiconductors (ITRS), is expected to continue over many years for desktop and mobile computers [1]. Because of this trend, many serious signal integrity

issues have already aroused and will arise in high-speed packages and printed circuit boards (PCB).

Glass ceramic based single-chip module (SCM) and multi-chip module (MCM) carriers have been used for IBM's high-performance server applications since the early 1980s [2]. This is because glass ceramic based carrier can provide very high wiring and power densities and therefore high-performance [3]. In addition to that, glass-ceramic material provides much lower dielectric loss than typical printed circuit board material such as FR4 and therefore dielectric dispersion is very small and can be neglected [4]. The IBM's POWER and z-series high-performance server systems have been built using this technology because of the high-data rates that can be sustained and the high wiring capacity. However, as signal speeds and the number of those signal IOs increase rapidly in recent applications of ASICs, signal integrity issues arises. Among them, the most serious signal integrity issue is high noise coupling between signal interconnects and has become the most critical concern in glass ceramic packages and severely limited its application at high-speed data rates. Especially, high far-end (FE) noise coupling between signal interconnects in glass ceramic packages has been a serious bottleneck for high-performance systems. Hence, reduction of FE noise coupling between signal interconnects in high-speed glass ceramic packages has become a critical issue.

To reduce noise coupling in signal interconnects in glass ceramic modules, the method in [5] was recently reported. In this method, metal fillings were inserted in mesh planes to reduce noise coupling in ceramic packages. However, the use of this method is limited in real glass ceramic module applications since there is a limit for metal loading for each metal layer in glass ceramic packages and the use of metal fillings in mesh planes significantly increases metal amount in the layer, which is not cost-effective and also violates a limit for metal loading. Hence, it is necessary to develop a novel and efficient method which reduces FE noise coupling and does not violate limit for metal loading in glass ceramic packages.

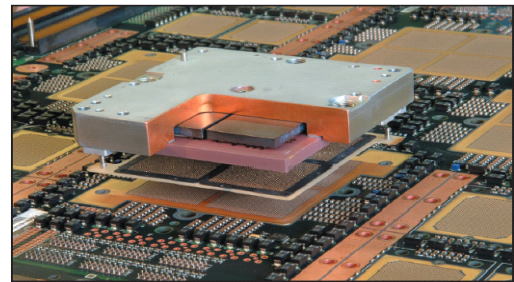
This paper is organized as follows. In Section II, issues related to mesh planes in glass ceramic packages are described. In Section III, modeling and simulation methodology for interconnect structures in glass ceramic modules are shown. This is followed by signal integrity analysis in Section IV. In Section V, transient simulation is performed to quantify noise coupling between interconnects in glass ceramic packages. Noise coupling reduction methodology employing power/ground mesh planes with alternating orthogonal lines and a via-connected coplanar-type shield (VCS) structure and eye diagram simulation results are presented in Section VI. Finally, the conclusion is provided in Section VII.

II. Mesh planes in Glass Ceramic Packages

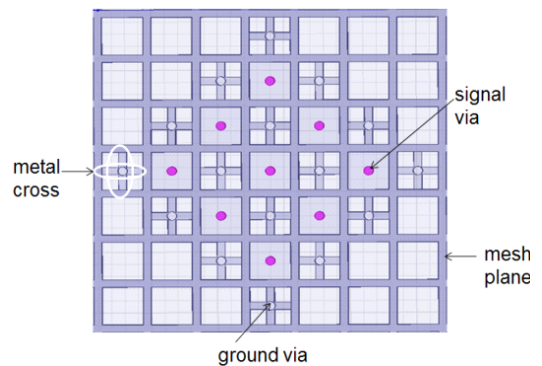
Mesh planes normally have been used as reference planes for signal lines in glass ceramic packages while solid planes have been used as ground/power planes in organic packages and PCBs. For glass ceramic packages, conductors are screened on individual ceramic sheets

that are laminated and sintered at higher than 900 °C. This type of processing imposes restrictions on the type of transmission line designs. [Fig. 1] (a) shows a cut-away view of IBM multi-chip module (MCM) showing a copper hat, the silicon carbide (SiC) heat spreaders, IBM high-performance glass-ceramic substrate, the LGA spring connector, the IBM advanced board and precision alignment pins for assembly [6]. Most ground planes in glass ceramic modules are hollow meshes that allow punched vias go through [3], which is shown in [Fig. 1] (b).

In fact, these mesh planes perturb the propagation characteristics of the interconnects from the values they would have if the reference planes were solid planes



(a) Cutaway view of IBM multi-chip module (MCM)



(b) Top view of mesh plane in glass ceramic modules

[Fig. 1] Glass ceramic package for high-performance servers.

[7]. It was reported that far-end noise coupling was substantially higher for mesh plane structures than that for solid plane structures [5], [8]. It is known that signal integrity is mostly affected by distortions caused by hollow mesh reference planes and orthogonal lines in mesh planes. Hence, it is important to study effects of orthogonal lines in mesh planes on noise coupling between interconnects. In Section IV, the effects of orthogonal lines in mesh planes on near-end and far-end noise coupling will be shown and, based on this result, methodology to reduce far-end noise coupling will be presented in Section VI.

III. Modeling and Simulation

3-1 Modeling and Simulation Methodology

Commercial 3-D full-wave EM (electromagnetic) solvers based on FEM (Finite Element Method) provides accurate simulation results. However, using a FEM tool for modeling of the complex interconnect structure in multi-layer ceramic SCM and MCM requires unaffordable CPU runtime and computational resources. Therefore, a better efficient modeling approach with reasonable accuracy and fast CPU runtime is required for modeling glass ceramic packages. In addition to this, it should be noted that non-optimized modeling conditions in 3-D full-wave EM solvers based on FEM such as ANSYS HFSS (High Frequency Structure Simulator) could result in deviating the simulation results from correct ones [9].

In this paper, a hybrid modeling approach is shown to speed up simulation and to use less memory for modeling complex interconnect structures in glass ceramic packages. The hybrid modeling method consists of CZ2D tool and EMITPKG tool, which are IBM's internal

tools. CZ2D is a highly accurate 2-D quasi-static tool which is based on method of moment (MoM) algorithm and computes the R, L, G, and C parameters for 2-D structures [10]. The CZ2D handles resistive losses, lossy and frequency dependent dielectrics and has facilities to assure physical consistency such as causality. In addition to this, CZ2D has a powerful auto gridding facility that accounts for proximity effect, edge effect, and skin effect to assure high accuracy [11], [12]. EMITPKG is based on a full-wave analysis method based on MoM [13] to calculate the Y parameters seen between two appropriately chosen reference planes, which are called as port planes and the per-unit-length $RLGC$ parameters are computed from Y parameters. Using scalar and vector potentials, in a standard moment-method procedure, a matrix equation is generated having the following form

$$\mathbf{Z}\mathbf{I} = \mathbf{V} \quad (1)$$

where \mathbf{Z} is an impedance matrix, \mathbf{I} is a column vector of current coefficients, and \mathbf{V} is a column vector of test voltages. The equation is solved for the unknown currents, from which the EM field distribution can be calculated. The matrix element in row β and column α is represented as follows [13];

$$Z_{\beta\alpha} = \int_{u_{1\beta}}^{u_{2\beta}} [\mathbf{E}^s(x, y, z) - R_{s\alpha} R'_\alpha(x, y, z) \mathbf{e}_{u\alpha}] \cdot \mathbf{e}_{u\beta} du \quad (2)$$

where $\mathbf{E}^s = -j\omega\mathbf{A} - \nabla\Phi$ is the electric field produced by volume current density. $u_{1\beta}$ and $u_{2\beta}$ are interval end variables defined in [13]. $R_{s\alpha}$ is surface impedance, depending on the orientation of rooftop α , $R_{s\alpha}$ could be either R_{sx} , R_{sy} , or R_{sz} . \mathbf{A} is the vector potential, given by

$$\mathbf{A} = \frac{\mu_0}{4\pi} \iiint \frac{J e^{-jkr(x-x', y-y', z-z')}}{r(x-x', y-y', z-z')} dx' dy' dz' \quad (3)$$

and Φ is the scalar potential, given by

$$\Phi = \frac{1}{4\pi\epsilon_0} \iiint \frac{\rho e^{-jkr(x-x', y-y', z-z')}}{r(x-x', y-y', z-z')} dx' dy' dz' \quad (4)$$

where \mathbf{J} is volume current density can be expressed by

$$\mathbf{J} = \sum_{\alpha=1}^{P'} R_{\alpha}(x, y, z) I_{\alpha} \mathbf{e}_{u\alpha} \quad (5)$$

where $R_{\alpha}(x, y, z)$ is the rooftop function centered at $x = x_{\alpha}$, $y = y_{\alpha}$, $z = z_{\alpha}$. I_{α} is the corresponding current coefficient, P' is the total number of rooftop functions, $\mathbf{e}_{u\alpha}$ is unit vector along the direction of current flow. $R'_{\alpha}(x, y, z)$ is defined as follows [13];

$$R'_{\alpha}(x, y, z) = \begin{cases} q_{\tau\mu\alpha}(u - u_{\alpha}), & \text{if } w = w_{\alpha} \\ 0, & \text{if } w \neq w_{\alpha} \end{cases} \quad (6)$$

where $q_{\tau\mu\alpha}(u - u_{\alpha})$ is a triangular function defined in [13]. And the elements of \mathbf{V} are given by

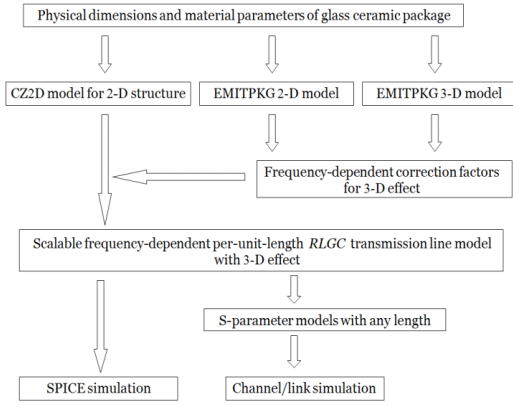
$$V_{\beta} = - \int_{u_{1\beta}}^{u_{2\beta}} \mathbf{E}^i(x, y, z) \cdot \mathbf{e}_{u\beta} du \quad (7)$$

where $\mathbf{E}^i(x, y, z)$ is the incident electric field.

The modeling procedure using EMITPKG involves setting up a signal interconnect structure that is driven by sources at sufficiently far distances from the port planes [14], which makes source effect on the EM field between the port planes is negligible, which means the end effects are effectively stripped off and the results correspond to the effective transmission line parameters of the structure. In other words, the calculation of Y

parameters involves voltages and currents on the port planes, the effects of the regions outside the port planes are removed, which is a unique feature of the EMITPKG and is different from other FEM based 3-D EM solvers that cannot exclude the end effects. In addition to this, relatively smaller structure is required in EMITPKG than in other FEM based 3-D EM solvers. This is because glass ceramic structures are periodic and EMITPKG only requires some periodic areas rather than the whole structure to extract the per-unit-length *RLGC* parameters. Once the per-unit-length *RLGC* parameters are extracted, a scalable per-unit-length *RLGC* transmission model is generated. With the scalable per-unit-length *RLGC* transmission model, it is possible to run any length of transmission lines in PowersPICE and it is also possible to generate S-parameter models with any length for channel simulator. Therefore, EMITPKG provides an accurate and unique method to extract the *RLGC* parameters of structures that resemble 2-D uniform transmission lines but also include 3-D effects.

[Fig. 2] shows modeling and simulation methodology flow chart for analyzing interconnect structures in glass ceramic modules. From the given physical dimension and material parameters of the glass ceramic packages, CZ2D model for the 2-D structure is built with 23 frequency points which ranges from DC to 100 GHz. And then, EMITPKG 3-D and 2-D models are made at the same frequency points. The correction factors for 3-D effect like mesh planes, vias, and metal crosses can be extracted from the EMITPKG 3-D and 2-D models. The same modeling conditions such as the same sub-sectional grid are used for both structures to remove any errors due to different modeling conditions in EMITPKG. So, accurate correction factors for 3-D effects can be generated as offsets between 3-D EMITPKG results and



[Fig. 2] Modeling and simulation methodology.

2-D EMITPKG results, as shown below.

$$\begin{aligned}
 R_{3-D_effects}(f) &= R_{EMITPKG_3-D}(f) - R_{EMITPKG_2-D}(f) \\
 L_{3-D_effects}(f) &= L_{EMITPKG_3-D}(f) - L_{EMITPKG_2-D}(f) \\
 G_{3-D_effects}(f) &= G_{EMITPKG_3-D}(f) - G_{EMITPKG_2-D}(f) \\
 C_{3-D_effects}(f) &= C_{EMITPKG_3-D}(f) - C_{EMITPKG_2-D}(f) \quad (8)
 \end{aligned}$$

where f represents selected group of frequency points or a selected single frequency point. It should be noted that a single frequency can be used for faster results while multiple frequencies can be used for better accuracy.

Then, these frequency-dependent correction factors for 3-D effect are applied to $RLGC$ parameters calculated from CZ2D, which results in the final $R(f)$, $L(f)$, $G(f)$, and $C(f)$ parameters, as shown below.

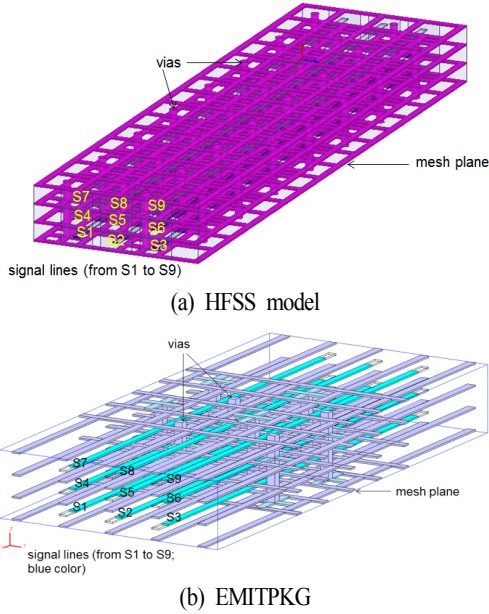
$$\begin{aligned}
 R(f) &= R_{CZ2D}(f) + R_{3-D_effects}(f) \\
 L(f) &= L_{CZ2D}(f) + L_{3-D_effects}(f) \\
 G(f) &= G_{CZ2D}(f) + G_{3-D_effects}(f) \\
 C(f) &= C_{CZ2D}(f) + C_{3-D_effects}(f) \quad (9)
 \end{aligned}$$

This hybrid modeling sequence results in a scalable frequency-dependent per-unit-length $RLGC$ transmission

line model for the given interconnect structure in glass ceramic packages. For transient simulation results, this transmission line model can be run in SPICE for any length and, for eye opening results, S-parameter with any length can be extracted from the scalable frequency dependent per-unit-length $RLGC$ transmission line model and is used as an input for any channel/link simulator.

3-2 Validation of Hybrid Modeling Approach

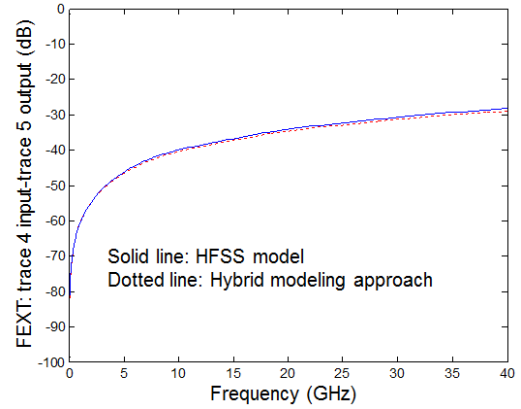
In this section, hybrid modeling approach was verified through HFSS which is one of the well-known commercial 3-D EM solvers based on FEM. The same interconnect structure in glass ceramic package was generated for hybrid modeling method and HFSS. [Fig. 3] (a) shows 3-D view of HFSS model while [Fig. 3] (b) shows 3-D view of EMITPKG model. In HFSS model, length of trace was 5.629 mm and wave ports were employed. In [Fig. 3], 4 mesh planes and 9 signal lines are shown. In these models, a horizontal grid is 371.2 μm and a vertical grid is 83 μm . The signal line width is 59 μm and signal height is 11.25 μm . The ground line width in mesh planes is 61 μm and power/ground line height in mesh planes is 15 μm . The dielectric constant of a dielectric material is 5.15 and loss tangent of the dielectric material, $\tan\delta$, is 0.0005. The mesh pitch is 371.2 μm and via diameter is 71 μm . In typical mesh plane structures, the wave is non-TEM [15] and hence, wave ports in HFSS were chosen since wave ports in HFSS were made to capture non-TEM wave characteristics. In EMITPKG model, the first port plane was located in the middle of the second mesh and the second port plane was located in the middle of the third mesh. It is important to place the port planes at such locations that EM field between them is uniform, i.e., that the current flow is nearly two dimensional. It should



[Fig. 3] Two 3-D interconnect models in glass ceramic packages model for hybrid modeling approach.

be noted that the whole structure is not required for EMITPKG model, which is one of the main advantages of EMITPKG tool since a compact EMITPKG structure reduces CPU runtime significantly. For both models, 20 MHz is chosen as a starting frequency, 40 GHz is chosen as a stop frequency, and 20 MHz is used as a frequency step. In S-parameter models, odd numbers are used for input ports of the signal lines and even numbers are used for output ports of the signal lines. [Fig. 4] shows comparison of S-parameters from the HFSS model and hybrid modeling approach.

Because far-end noise coupling or far-end crosstalk (FEXT) is an important parameter in glass ceramic modules, FEXT between input of trace 4 (i.e., a signal line 4; S4) and output of trace 5 (i.e., a signal line 5; S5) was chosen for comparison. As can be observed, there is a good correlation between HFSS model and



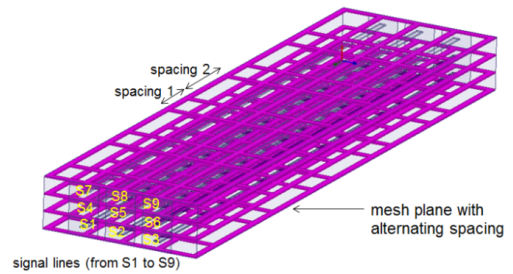
[Fig. 4] Comparison of S-parameters from HFSS model and hybrid modeling approach.

hybrid modeling approach (i.e., EMITPKG and CZ2D) over entire frequency range (i.e., from 20 MHz to 40 GHz).

IV. Signal Integrity Analysis

4-1 Impact of Orthogonal Lines in Mesh Planes on Impedance

To investigate impact of orthogonal lines in mesh planes on impedance, two HFSS models were generated. One model has orthogonal lines with constant spacing in mesh planes like in [Fig. 3] (a) while the

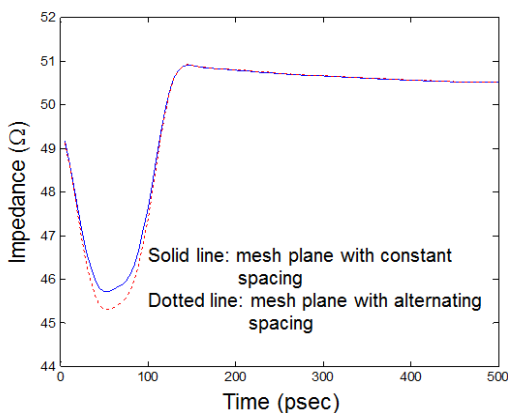


[Fig. 5] 3-D view of HFSS model with alternating spacing in mesh planes.

other model has orthogonal lines with alternating spacing like in [Fig. 5]. To remove any effects due to vias on the results, vias and their metal crosses were not included in these models.

[Fig. 6] shows impedance plots for both models by TDR (time domain reflectometer). For TDR simulation, a step input with rise time of 41.66 psec was applied at the input of trace 5 (i.e., signal line 5; S5) to obtain impedance plots of both models. From [Fig. 6], impedance of a signal line 5 with mesh planes with constant spacing is $45.7\ \Omega$ while impedance of the signal line 5 with the mesh planes with alternating spacing is $45.3\ \Omega$. It is obvious that impedance for both structures were very close, which indicates that effect of orthogonal lines with different spacing in mesh planes on impedance was not significant.

In other words, the mesh planes with alternating spacing could be used as reference planes for signal lines without making any issue related to deviation from target impedance in an original design.



[Fig. 6] TDR simulation results for the structures with mesh planes with constant spacing and with alternating spacing.

4-2 Impact of Orthogonal Lines in Mesh Planes on Noise Coupling between Signal Interconnects

Noise coupling between interconnects in glass ceramic modules has become a major bottleneck for system performance as a clock speed has increased. Especially, far-end noise coupling has been a critical issue in glass ceramic modules since mesh planes have been used as reference planes for signal lines and it was reported that higher far-end noise coupling was observed in mesh plane environment than in solid plane environment [5], [8]. Therefore, it's important to see effects of mesh planes on noise coupling. Preliminary studies on effects of mesh planes on noise coupling were shown in [16].

The same two HFSS models in section 4-1 were used for this purpose. That is, one model has orthogonal lines with constant spacing in mesh planes while the other model has orthogonal lines with alternating spacing in mesh planes. First, near-end noise coupling or near-end crosstalk (NEXT) was investigated for both cases. [Fig. 7] (a) shows NEXT between input of trace 4 and input of trace 5 for both cases. As can be observed, less NEXT was observed for the model with constant spacing in mesh planes than the model with alternating spacing in mesh planes. So, it is desirable to employ mesh planes with orthogonal lines with constant spacing for locations where near-end noise coupling should be minimized. Second, far-end noise coupling or far-end crosstalk (FEXT) was tested for both cases. [Fig. 7] (b) shows FEXT between input of trace 4 and output of trace 5. It is observed that the model with alternating spacing in mesh planes produced less FEXT than the model with constant spacing in mesh planes. This observation is very important since FEXT is a critical issue in glass ceramic packages and this result

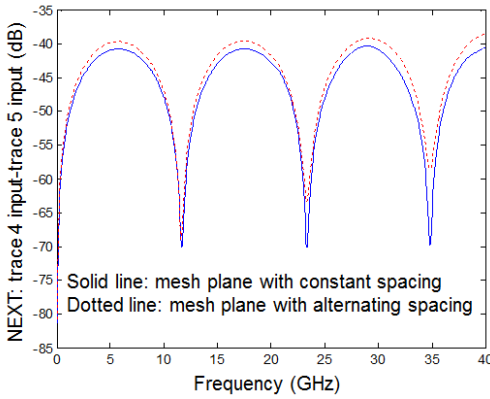
indicates that the FEXT can be reduced using only mesh planes with alternating spacing. Normally shield lines are inserted between signal lines to reduce FEXT or metal fillings are inserted in mesh planes to reduce FEXT [5]. Through these methods, mutual inductance and conductance that are main causes of noise coupling can be reduced but these methods require extra costs due to additional metals needed. Also the method using metal fillings cannot be used sometimes due to limit for metal loading in each metal layer. Hence, it is great to minimize FEXT using only mesh planes with alternating spacing, which does not require extra metal and

actually requires less metal rather than regular mesh planes with constant spacing.

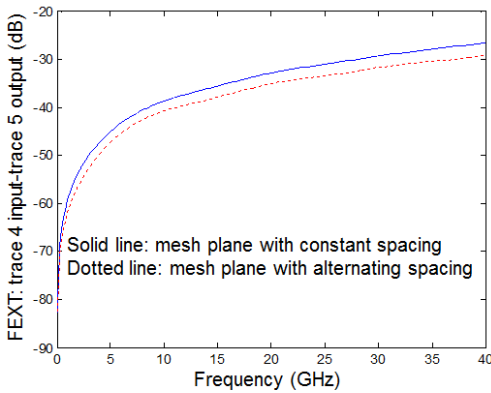
V. Transient Simulation

In this section, transient simulation was performed in PowerSPICE, which is an internal IBM SPICE simulator, to quantify NEXT and FEXT due to all 8 aggressors around a victim (S5) in Fig. 3 (b). The hybrid modeling approach was used to generate a scalable frequency dependent per-unit-length *RLGC* transmission line model. Then, this transmission line model was run in PowerSPICE to see near-end (NE) and far-end (FE) noise coupling between a victim and aggressors. To quantify NEXT and FEXT due to 8 aggressors, which is the worst case scenario, the signal line S5 was chosen as a victim (i.e., a passive line) and the other signal lines were chosen as aggressors (i.e., active lines). The 1 V step input whose rise time (t_r) is 41.66 psec was applied to inputs of signal lines S1, S2, S3, S4, S6, S7, S8, and S9 for the worst case crosstalk and all signal lines were terminated with $50\ \Omega$ resistor at input and output. Due to hollows in the mesh ground planes, a quiet line (i.e., a victim) receives coupled noise from all the surrounding aggressors. For the glass ceramic interconnect structure in [Fig. 3] (b), the signal lines S2 and S8 are the biggest noise contributors to a victim line S5 among aggressors since the vertical grid ($83\ \mu\text{m}$) is much shorter than the horizontal grid ($371.2\ \mu\text{m}$), which means that vertical coupling is much stronger than horizontal coupling for the interconnect structure in [Fig. 3] (b).

[Fig. 8] shows near-end and far-end noise waveforms on the victim line (S5) due to 8 aggressors when the trace length was chosen as 2 cm in PowerSPICE simu-

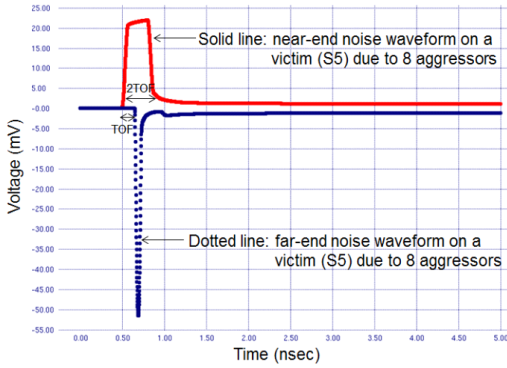


(a) NEXT results.



(b) FEXT results.

[Fig. 7] Noise coupling comparison for two cases.



[Fig. 8] Near-end and far-end noise waveforms on a victim (S_5) due to 8 aggressors in transient simulation.

lation, which are typical noise waveforms for glass ceramic interconnect structures. The noise waveforms are reasonable since the width of the near-end noise waveform is around 2TOF (time of flight) and the far-end noise waveform started at TOF and its width is close to the rise time of 1 V step on aggressors [17].

The saturated near-end noise V_N and far-end noise V_F can be expressed as follows when signal lines are terminated with 50Ω resistor at input and output and aggressors are with step excitation [17], [18]:

$$V_N = \frac{1}{4} \left(\frac{C_m}{C} + \frac{L_m}{L} \right) V_s$$

$$V_F = \frac{1}{2} \left(\frac{C_m}{C} - \frac{L_m}{L} \right) \frac{l \sqrt{LC}}{t_r} V_s \quad (10)$$

where C_m and C are the mutual capacitance per unit length and the self-capacitance per unit length, respectively, and L_m and L are the mutual inductance per unit length and the self-inductance per unit length, respectively. V_s is the voltage amplitude on the active line,

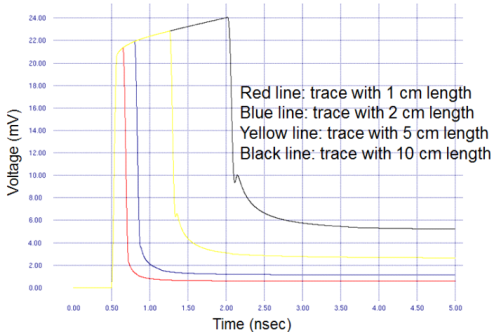
l is the coupling length, and t_r is the input step rise time. It is clear that the saturated near-end noise is always positive but the saturated far-end noise can be negative or positive depending on magnitude of C_m , C , L_m and L . In other words, near-end noise coupling always exists since cancellation is not possible but far-end noise coupling can be eliminated when the following condition is met:

$$\frac{C_m}{C} - \frac{L_m}{L} = 0 \quad (11)$$

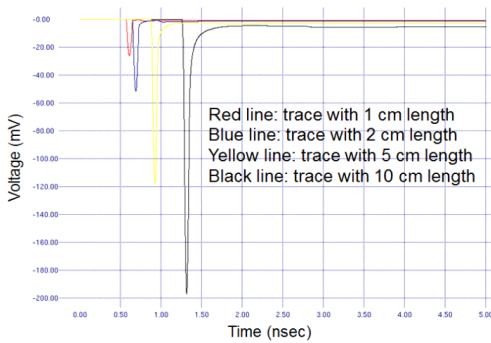
It should be noted that the condition in equation (11) indicates that it is possible to eliminate far-end noise coupling completely if the signal interconnect structure in glass ceramic packages can be designed to satisfy the condition in equation (11). However, it is practically extremely difficult to eliminate far-end noise coupling completely in glass ceramic packages.

To investigate the relationship between a trace length and noise coupling, 4 traces with 1 cm, 2 cm, 5 cm, and 10 cm were chosen. Then, these 4 traces were run in PowerSPICE to see near-end and far-end noise waveforms on the victim line (S_5) due to 8 aggressors. [Fig. 9] (a) shows near-end noise waveforms on the victim line (S_5) for 4 traces with different length. It is observed that the saturated or maximum near-end noise is increased slightly as the length of trace increases from 1 cm to 10 cm.

However, this tendency is not the same for far-end noise coupling. Fig. 9 (b) shows far-end noise waveforms on the victim line (S_5) for 4 traces with different length. As can be shown, far-end noise coupling increases dramatically as the length of trace increases, which is a serious signal integrity issue in glass ceramic pac-



(a) Near-end noise waveforms on the victim (S_5) due to 8 aggressors for traces with different length



(b) Far-end noise waveforms on the victim (S_5) due to 8 aggressors for traces with different length

[Fig. 9] Relationship between trace length and noise coupling in glass ceramic packages.

<Table 1> Saturated near-end and far-end noises vs. trace length in glass ceramic packages.

Trace\Saturated noise	Saturated near-end noise (mV)	Saturated far-end noise (mV)
Trace with 1 cm length	21.35	-26.25
Trace with 2 cm length	21.93	-51.54
Trace with 5 cm length	22.85	-117.70
Trace with 10 cm length	24.06	-196.95

kages. In <Table 1>, saturated near-end and far-end noises for traces with different length are summarized.

VI. Noise Coupling Reduction Methodology

6-1 Methodology

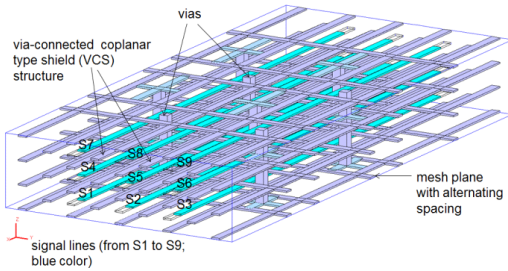
In this section, efficient methodology for reducing far-end noise coupling in glass ceramic packages is suggested. Then, transient simulations are performed to show how efficient this methodology is. Finally, channel simulation results are shown for comparison of eye openings.

There are well-known methods for reducing far-end noise coupling in packages and printed circuit boards. First, decreasing the coupling length between a victim line and active lines reduces far-end noise coupling [19] since far-end noise coupling is proportional to the coupling length, l , which is shown in equation (10). However, this cannot be easily achieved due to complex high-speed signal routing in glass ceramic packages. Second, increasing the distance between a victim line and active lines can reduce far-end noise coupling. But this method cannot be employed practically. This is because current tendency for high-speed modules requires more signal lines in a smaller area in glass ceramic packages. Therefore, an efficient methodology for reducing far-end noise coupling in glass ceramic modules is critical for better system performance.

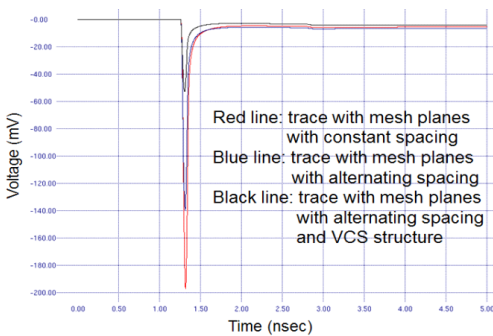
In section IV, it was shown that the interconnect structure with mesh planes with alternating spacing produced less far-end noise coupling than the interconnect structure with mesh planes with constant spacing. This indicates that the orthogonal lines in mesh planes are sources to increase far-end noise coupling between interconnects. Hence, it is critical to employ mesh planes with alternating spacing to reduce far-end noise coupling. To reduce far-end noise coupling further, the interconnect structure with via-connected coplanar-type

shield (VCS) structure [5], [20] should be also employed. [Fig. 10] shows 3-D view of optimized interconnect structure with mesh planes with alternating spacing and via-connected coplanar-type shield (VCS) structure [21].

The following three cases were chosen for comparison of far-end noise coupling; (i) interconnect with mesh planes with constant spacing, (ii) interconnect with mesh planes with alternating spacing, and (iii) interconnect with mesh planes with alternating spacing and via-connected coplanar-type shield (VCS) structure. These



[Fig. 10] 3-D view of optimized interconnect structure with mesh planes with alternating spacing and via-connected coplanar-type shield (VCS) structure to minimize far-end noise coupling in glass ceramic modules.



[Fig. 11] Far-end noise coupling comparison for three cases.

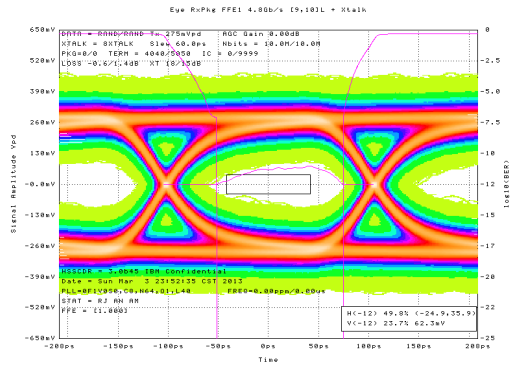
<Table 2> Saturated far-end noises for three cases.

Interconnect\far-end noise	Saturated far-end noise (mV)
Interconnect with mesh planes with constant spacing	-196.95
Interconnect with mesh planes with alternating spacing	-139.30
Interconnect with mesh planes with alternating spacing and VCS structure	-52.49

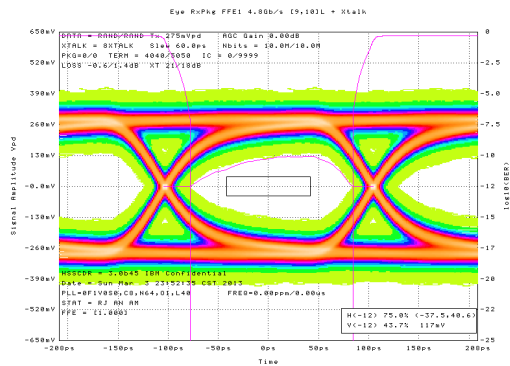
three interconnect structures were generated by hybrid modeling approach. The trace length of 10 cm was selected and three cases were run in PowerSPICE to evaluate far-end noise coupling. [Fig. 11] shows far-end noise waveforms on a victim (S5) due to 8 aggressors for the three cases when the trace length is 10 cm. It is clear that the case (iii) shows the least saturated far-end noise among three cases and the case (ii) produces less saturated far-end noise than that of the case (i). In summary, with the optimized interconnect structure in the case (iii), the saturated far-end noise was reduced by 73.3 % compared with that of the case (i) which is the interconnect with mesh planes with a regular constant spacing. In <Table 2>, saturated far-end noises for these three cases are summarized.

6-2 Eye Diagram Simulation

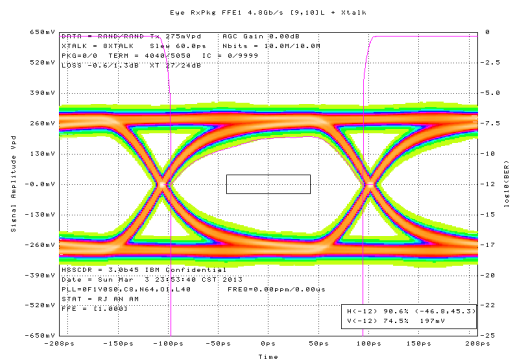
In high-speed digital systems, an eye diagram has become a common indicator of the quality of signals in a channel. To get the eye diagrams of the three cases in section 6-1, HSSCDR (High Speed SerDes/Clock Data Recovery) simulations were performed from a chip (driver side) to a chip (receiver side) at 4.8 Gbps. HSSCDR is an internal IBM channel simulator for system-level channel simulations. [Fig. 12] shows the



(a) Interconnect with mesh planes with constant spacing



(b) Interconnect with mesh planes with alternating spacing



(c) Interconnect with mesh planes with alternating spacing

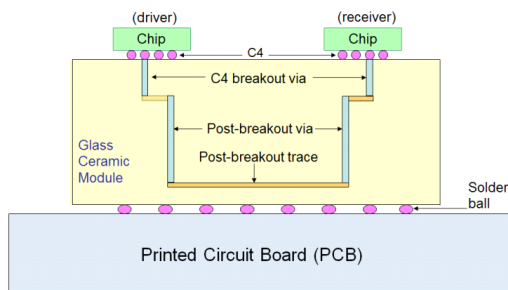
[Fig. 12] Eye diagram simulation results for three cases at 4.8 Gbps and via-connected coplanar-type shield (VCS) structure.

eye diagram simulation results for the three interconnect cases. In these eye diagrams, x-axis is time in psec and y-axis is signal amplitude in mV. The eye opening in eye diagrams was monitored at a receiver. Since vertical eye opening is closely associated with noise coupling, vertical eye opening in eye diagrams should be monitored carefully. As can be observed, the interconnect with mesh planes with alternating spacing shows a bigger eye opening than the interconnect with mesh planes with constant spacing. Similarly, the eye opening for the interconnect with mesh planes with alternating spacing and via-connected coplanar-type shield (VCS) structure is much bigger than that of the interconnect with mesh planes with alternating spacing, which is consistent with far-end noise coupling results shown in [Fig. 11]. In <Table 3>, vertical eye opening results (from 0 mV to peak value in mV) for three interconnect cases are summarized.

Next, full module-level channel simulations including several models were performed in HSSCDR to see effects on eye opening at a receiver due to different interconnect structures. For a full module-level channel analysis in typical ceramic modules, two C4 breakout via models with 1.9 mm length, two post-breakout via models with 6 mm length, one of interconnect models

<Table 3> Vertical eye opening results for three interconnect cases.

Interconnect/eye opening	Vertical eye opening (mV)
Interconnect with mesh planes with constant spacing	62.3
Interconnect with mesh planes with alternating spacing	117
Interconnect with mesh planes with alternating spacing and VCS structure	197



[Fig. 13] Module-level channel simulation for eye diagrams.

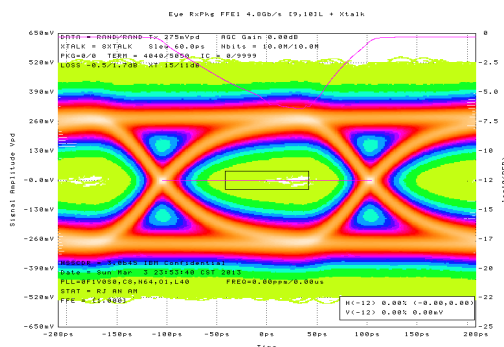
with 10 cm length (i.e., post-breakout trace) among three interconnects in section 6-1 were included for simulation, as shown in [Fig. 13].

[Fig. 14] shows the eye opening results for the full module-level channel cases. The eye in an eye diagram is closed for the channel with the interconnect with mesh planes with constant spacing, as shown in [Fig. 14] (a). But it is observed that there is an improvement in eye opening when the interconnect with alternating spacing is used in module-level simulation, as shown in [Fig. 14] (b).

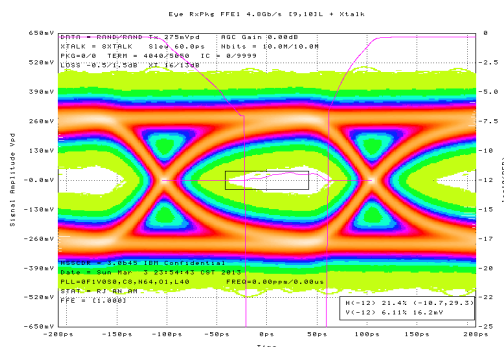
Finally, with the optimized interconnect with mesh planes with alternating spacing and via-connected coplanar-type shield (VCS) structure, there is a significant improvement in eye opening, which clearly demonstrates noise coupling reduction capability of the optimized interconnect with alternating spacing and via-connected coplanar-type shield (VCS) structure in high-speed multi-layer glass ceramic modules. In <Table 4>, vertical eye opening results (from 0 mV to peak value in mV) for the three channel cases are summarized.

VII. Conclusion

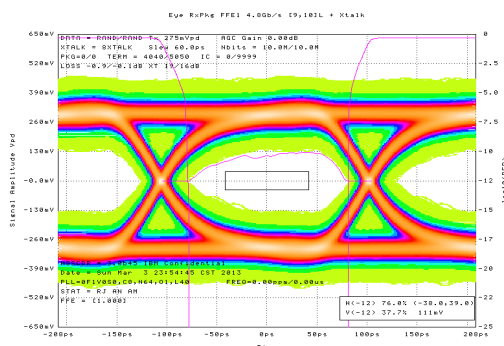
In this paper, signal integrity issues related to mesh planes in high-speed glass ceramic packages have been



(a) Channel with the interconnect with mesh planes with constant spacing



(b) Channel with the interconnect with mesh planes with alternating spacing



(c) Channel with the interconnect with mesh planes with alternating spacing

[Fig. 14] Eye diagram simulation results for full module-level channels at 4.8 Gbps and via-connected coplanar-type shield (VCS) structure.

〈Table 4〉 Vertical eye opening results for three channel cases.

Channel/eye opening	Vertical eye opening (mV)
Channel with interconnect with mesh planes with constant spacing	0
Channel with interconnect with mesh planes with alternating spacing	16.2
Channel with interconnect with mesh planes with alternating spacing and VCS structure	111

discussed. Then, an efficient methodology for reducing far-end noise coupling in high-speed ceramic modules has been presented. This methodology employs mesh planes with alternating spacing and via-connected coplanar-type shield (VCS) structure to minimize far-end noise coupling between signal interconnects in glass ceramic packages. It has been shown that, with the optimized interconnect structure based on this methodology, the saturated far-end noise coupling of a typical interconnect structure in glass ceramic modules could be reduced significantly by 73.3 %. Finally, eye diagram simulation results also demonstrate that the eye opening has been improved significantly with the optimized interconnect structure.

References

- [1] J. Choi, S. Min, J. Kim, M. Swaminathan, W. Beyene, and C. Yuan, "Modeling and analysis of power distribution networks for gigabit applications", *IEEE Trans. on Mobile Computing*, vol. 2, no. 4, pp. 299-313, Oct.-Dec. 2003.
- [2] R. R. Tummala et al., "Packaging technology for IBM's latest mainframe computers", *Proc. EIA /CPMT 41st Electronic Components and Technology Conf*, Atlanta, GA, pp. 682-688, May 1991.
- [3] A. Deutsch, "Electrical characteristics of interconnections for high performance systems", *Proc. of the IEEE*, vol. 86, no. 2, pp. 335-337, 1998.
- [4] R. R. Tummala, Rymaszewski, *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York, 1989.
- [5] J. Choi, R. Weekly, A. Haridass, and T. Zhou, "Methodology for minimizing far-end noise coupling between interconnects in high-speed ceramic modules", *IEEE 59th Electronic Components and Technology Conference (ECTC)*, San Diego, California, pp. 1227-1233, May 2009.
- [6] J. U. Knickerbocker et al., "An advanced multichip module (MCM) for high-performance UNIX servers", *IBM J. Res. & Dev.* vol. 46, no. 6, pp. 779-804, Nov. 2002.
- [7] A. C. Cangellaris et al., "Electrical characteristics of multichip module interconnects with perforated reference planes", *IEEE Trans-CPMT*, vol. 16, no. 1, pp. 113-118, 1993.
- [8] B. J. Rubin, "Comparison of mesh and solid planes for use in electrical packaging", *IEEE Proc 5th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 217-219, Oct. 1996.
- [9] J. Choi, Z. Chen, D. W. Becker, J. Morsey and B. Rubin, "Constructing 3D package component broadband electrical models with correct DC values.", *IEEE 20th Topical Meeting of Electrical Performance of Electronic Packaging and Systems (EPEPS)*, Austin, Texas, pp. 253-256, Oct. 2010.
- [10] W. T. Weeks, "Calculation of coefficients of capacitance of multiconductor transmission lines in the presence of a dielectric interface", *IEEE Trans-MTT*, vol. MTT-18, pp. 35-43, 1970.

- [11] W. T. Weeks, et al., "Resistive and inductive skin effect in rectangular conductors", *IBM J. Res. Develop.*, vol. 23, no. 6, pp. 652-660, 1979.
- [12] A. E. Ruehli et al., "Method for generating an electrical circuit comprising dielectrics", U.S. Patent #6192507, May 1998.
- [13] B. Rubin et al., "Radiation and scattering from structures involving finite-size dielectric regions", *IEEE Trans-Antennas Propagat.*, vol. 38, pp. 1863-1873, 1990.
- [14] B. Rubin et al., "Calculation of multi-port parameters of electronic packages", *IEEE Proc 2nd Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 37-39, Oct. 1993.
- [15] B. Rubin, "The propagation characteristics of signal lines in a mesh-plane environment", *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-31, no. 5, pp. 522-531, May 1984.
- [16] J. Choi, W. D. Becker, and T. Zhou, "High-speed ceramic modules with hybrid referencing scheme for improved performance and reduced cost", U.S. Patent #8339803, Dec. 2012.
- [17] B. Young, *Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages*, Prentice-Hall, New York, pp. 98-104, 2001.
- [18] E. Bogatin, *Signal Integrity-Simplified*, Prentice-Hall, New Jersey, pp.401-469, 2004.
- [19] J. Choi, B. Krauter, A. Haridass, R. Weekly, D. Douriet, and S. Chun, "Crosstalk analysis between interconnects in high-speed server packages", *IEEE 57th Electronic Components and Technology Conference (ECTC)*, Reno, Nevada, pp. 333-338, May 2007.
- [20] J. Choi, S. Chun, A. Haridass, and R. Weekly, "Noise coupling reduction and impedance discontinuity control in high speed ceramic modules", U.S. Patent #8288657, Oct. 2012.
- [21] J. Choi, "Mesh planes with alternating spaces for multi-layered ceramic packages", U.S. Patent Applications # 820110319, Nov. 2011.

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