Optimized Design of Low-power Adiabatic Dynamic CMOS Logic Digital 3-bit PWM for SSL Dimming System

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***Abstract*:** The size and power consumption of digital circuits including the dimming circuit part will increase for high-performance solid state lighting (SSL) systems in the future. This study examined the low-power consumption of adiabatic dynamic CMOS logic (ADCL) due to the principles of adiabatic charging. Furthermore, the designed low-power ADCL digital pulse width modulation (PWM) was optimized for SSL dimming systems. For this purpose, an ADCL digital 3-bit PWM was optimized in two steps. In the first step, the architecture of the ADCL digital 3-bit PWM was miniaturized. In the second step, the clock cut-off circuit was designed and added to the ADCL PWM. As a result, compared to the original configuration, 60 transistors and 15 capacitors of ADCL digital 3-bit PWM were reduced for miniaturization. Moreover, the clock cut-off circuit, which controls wake-up and sleep mode of ADCL D-FFs, was designed. The power consumption of an optimized ADCL digital PWM for all bit patterns decreased by 54 %.

***Keywords*:** clock cut-off circuit, miniaturization, adiabatic dynamic CMOS logic, digital PWM, SSL dimming system, low-power design

1. Introduction

Green information technology (IT) has attracted significant attention for the low-power consumption of electronic devices, as well as applications to the smart grid, solar cell system, and hybrid electric vehicle. Furthermore, energy savings and the development of eco-friendly technologies are needed for general lighting systems.

There is a growing trend toward not using incandescent lamps because of their low-efficiency. In addition, the use of fluorescent lights that contain harmful materials, such as lead and mercury etc, is being reduced by regulating the use of heavy metals, waste electrical and electronic equipment (WEEE), and restriction of hazardous substances (RoHS) [1, 2]. Therefore, the development of the solid-state lighting (SSL) containing light emitting diodes (LEDs), organic light emitting diodes (OLEDs) and polymer light emitting diodes (PLEDs) is expanding due to the necessity of new eco-friendly lighting sources. Currently, the SSL has formed a broad market from the display to general lighting. Lighting manufacturers are conducting considerable research on low-cost and high efficiency operation systems of SSL to pre-empt the market of the next generation SSL systems [3, 4].

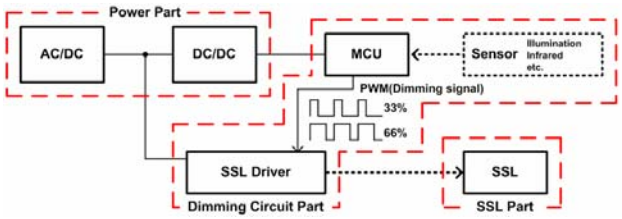


Fig. 1. SSL system.

Presently, the SSL system consists of a power part, dimming circuit part and SSL part, as shown in Fig. 1. Although power consumption of the dimming circuit part is the lowest, size and power consumption of the digital circuit, including the dimming circuit part will increase for

high-performance SSL systems in the future. Therefore, a low-power design of the dimming circuit part is required for low-power SSL systems. The pulse width modulation (PWM) is normally used for the dimming circuit [5-7].

The adiabatic dynamic CMOS logic (ADCL) was studied to reduce the power loss in a conventional CMOS logic for the low-power design of a logic circuit [8-14]. Power loss occurs by a sudden change in voltage from high to low and from low to high in CMOS logic with a direct current (DC) power supply. On the other hand, this power loss is reduced by slowly increasing and decreasing the power supply voltage in ADCL with the alternate current (AC) that is synchronized with for a change to high or low.

The SSL dimming circuit part was designed using the ADCL in Ref. [14]. On the other hand, the architecture has not been optimized. Furthermore, the power consumption is increased by the unnecessary operation of the ADCL D-flipflops (D-ffs) in ADCL digital 3-bit PWM at both dimming 0 % and 100 % of the PWM output. In this study, the low-power SSL dimming system was designed. ADCL digital 3-bit PWM was miniaturized. Moreover, the clock cut-off circuit, which controls the wake-up and sleep mode of the ADCL D-ffs, is proposed.

The remainder of this paper is organized as follows. Section 2 describes the adiabatic charging, and standard operation of adiabatic logic. A low-power ADCL digital 3-bit PWM was designed and optimized for a SSL dimming system in section 3. Section 4 reports the simulation results of designed circuits using a 1.2 μm standard CMOS technology. Finally, section 5 concludes the paper.

$$v_I(t)=\frac{V_I}{\tau}(t+\phi)\left[u(t)-u\left(t-(\tau-\phi)\right)\right]+V_I\left[u\left(t-(\tau-\phi)\right)\right] \tag{1}$$

$$v_R(t)=\frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-(\tau-\phi)}{CR}}\right)u\left(t-(\tau-\phi)\right)\right]+\frac{V_I\phi}{\tau}e^{-\frac{t}{CR}} \tag{2}$$

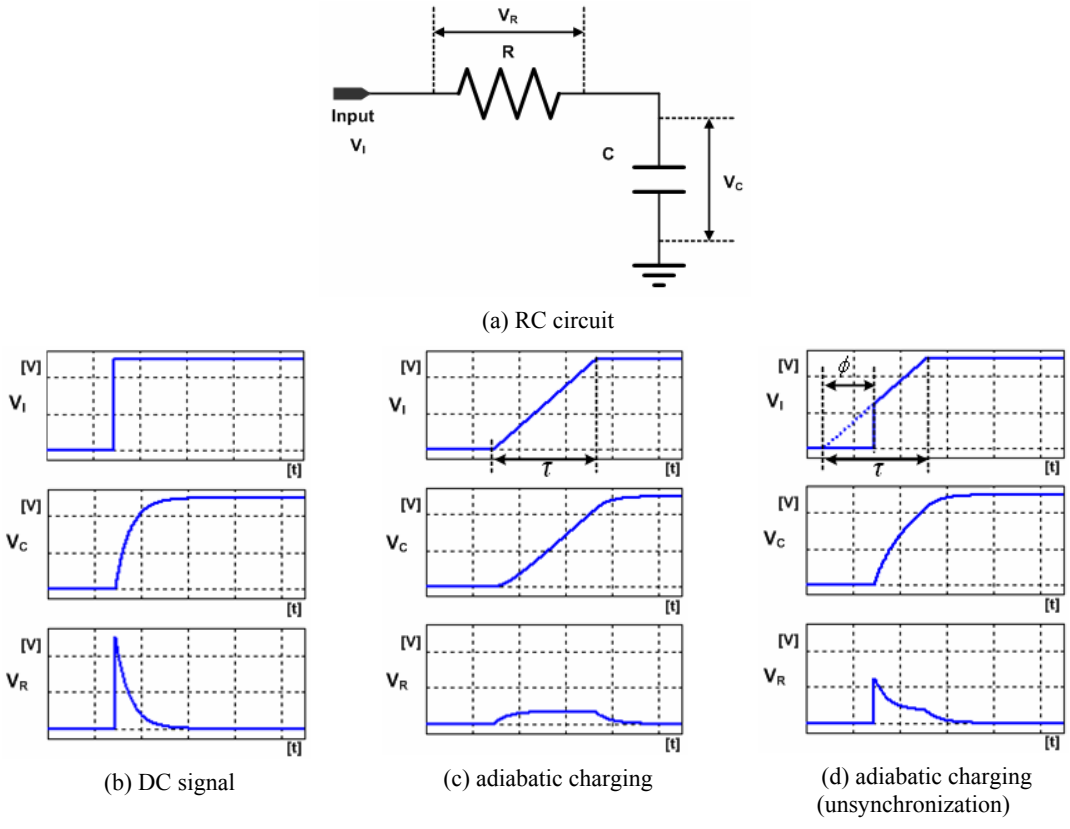
$$P_R(t)=R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-(\tau-\phi)}{CR}}\right)u\left(t-(\tau-\phi)\right)\right]+\frac{V_I\phi}{\tau R}e^{-\frac{t}{CR}}\right]^2 \tag{3}$$

2. Adiabatic Logic

2.1 Adiabatic Charging

During a sudden transition between high and low levels of the input voltage, a load capacitor cannot be charged and discharged immediately. Power dissipation occurs by the resistive component of the logic circuit in the conventional CMOS logic because this logic circuit uses a constant voltage; DC power supply. To minimize the power dissipation, adiabatic charging is one of the promising candidates with AC power, which has a slower rising/falling time than charge/discharge time constant [8-11].

Fig. 2 shows the operations at a normal RC circuit with a DC signal, adiabatic charging, and unsynchronization.



(a) RC circuit

(b) DC signal

(c) adiabatic charging

(d) adiabatic charging (unsynchronization)

Fig. 2. Operation of the RC circuit.

The input signal $v_I(t)$, voltage drop of the resistance $v_R(t)$ and power dissipation $P_R(t)$ in Fig. 2(a) are expressed in Eqs. (1)-(3), respectively, where τ is the rising time of input, ϕ is unsynchronized period and $u(t)$ is the unit step function [11-15].

In the case of the DC signal ($\tau = \phi$) at the input signal, the energy dissipation occurred at the load R until the end of charging at the load C, as shown in Fig. 2(b). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ at Fig. 2(a) are

$$v_I(t) = V_I\left[u(t)\right], \tag{4}$$

$$v_R(t) = V_I e^{-\frac{t}{CR}}, \tag{5}$$

$$P_R(t) = \frac{V_I^2}{R} e^{-\frac{2t}{CR}}. \tag{6}$$

On the other hand, in the case of the AC signal ($\phi = 0$) as the input signal, adiabatic charging and little power dissipation are shown in Fig. 2(c). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ are

$$v_I(t) = \frac{V_I}{\tau} t\left[u(t) - u(t-\tau)\right] + V_I\left[u(t-\tau)\right], \tag{7}$$

$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1 - e^{-\frac{t}{CR}}\right) - \left(1 - e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right], \tag{8}$$

$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1 - e^{-\frac{t}{CR}}\right) - \left(1 - e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right]\right]^2. \tag{9}$$

The region of adiabatic charging decreased with increasing ϕ of the AC signal, as shown in Fig. 2(d). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ are expressed as equation (1), (2), and (3) respectively [15].

2.2 Adiabatic Dynamic CMOS Logic (ADCL)

The ADCL consists of the CMOS logic, AC power and two diodes for the adiabatic charging as it is applied to the CMOS logic. Fig. 3 shows an ADCL inverter gate. In this circuit, because the output voltage of the ADCL gate is synchronized with the power supply, V_{phi}, the operating speed of the ADCL circuits is determined by the frequency of V_{phi}. Figs. 3(a) and (b) show the principle of the ADCL inverter [12-15].

Principle (I) input: high → low

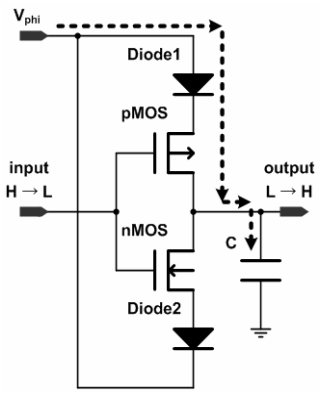
In Fig. 3(a), pMOS and nMOS are on and off, respectively. In this case, the supply current path is generated and the load capacitor C is charged adiabatically by V_{phi}. The high level is then kept with diode1.

Principle (II) input: low → high

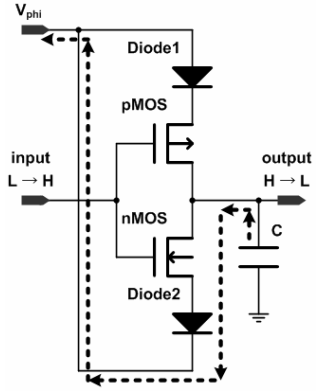
Under this condition, pMOS and nMOS are off and on, respectively. In this case, the current path is generated, as shown in Fig. 3(b) and the charge in C is discharged adiabatically into V_{phi}.

Consequently, the ADCL inverter works in the adiabatic mode, as shown in Fig. 3(c). On the other hand, if the difference between V_{phi} and the voltage across C is large, adiabatic operation will not be established and power will be largely dissipated.

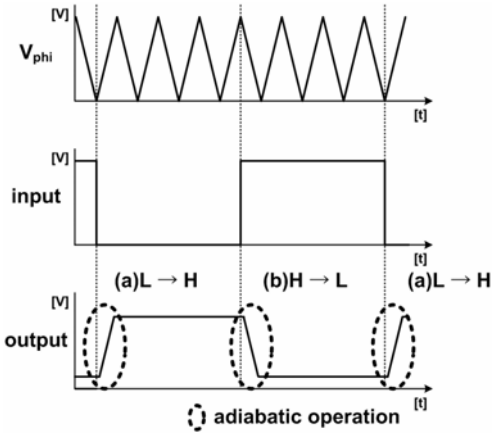
The ADCL operates the adiabatic charging whenever logic level of the output is changed from high level to low and vice versa. Furthermore, the charge can be reused because the charge reverts to the power source at the discharge of load C.



(a) input: H → L



(b) input: L → H



(c) operation waveforms

Fig. 3. Principles of ADCL inverter.

3. Optimized ADCL Digital 3-bit PWM

Low-power PWM of the SSL dimming system was optimized in two steps, as shown in Fig. 4. In the first step, the unnecessary gates at designed ADCL digital 3-bit PWM in Ref. [14] were reduced for miniaturization and the low-power consumption of the SSL dimming system. In the second step, the clock cut-off circuit is proposed, which pauses the ADCL D-ffs to incur power consumption by unnecessary operation at both dimming 0 % and 100 % of the PWM output.

3.1 Digital 3-bit PWM

The PWM is normally used for the dimming circuit. Fig. 5 shows the timing chart of digital 3-bit PWM. The PWM is reset, if the load is at a high level. The LD0, LD1, and LD2 can control the output pulse width. For example the output pulse width will be 33.3 % if LD0 = L, LD1 = L and LD2 = H (001), and the output pulse width will be 66.6% if LD0 = L, LD1 = H and LD2 = H (011). This output pulse width of the PWM can control the dimming of SSL. The SSL dimming circuit part was designed using ADCL in Ref. [14]. On the other hand, the architecture has not been optimized. Furthermore, power consumption occurs by the unnecessary operation of ADCL D-ffs in ADCL digital 3-bit PWM at both dimming 0 % and 100 % of the PWM output.

3.2 Miniaturization of ADCL Digital 3-bit PWM

To miniaturize ADCL digital 3-bit PWM, block (a) in Fig. 6, setting PWM pulse width by input-bit, was changed from 2 AND gates and OR gate to 3 NAND gates. The D-ffs to decrease the number of logic gates were used. Table 1 lists the elements and Fig. 6 shows the miniaturized ADCL digital 3-bit PWM. Compared to the original configuration, 60 transistors and 15 capacitors were reduced.

3.3 Design of the Clock Cut-off Circuit

Unnecessary operation at both dimming 0 % and 100 % of PWM output results in power consumption. The designed clock cut-off circuit pauses the D-ffs after cutting off the clock at both input-bit 000 (0 %) and 111 (100 %), and performs normal operation of the D-FFs at other case.

Fig. 7 shows the designed control block of the clock cut-off circuit. Table 2 lists the truth table of the proposed control block. The up-level D-latch was used to output the logic level of the SW and PO by the input-bit if the load is reset but to remain at the logic level of the pre-state if the load is set.

4. Simulation Results

The optimized ADCL digital 3-bit PWM system was

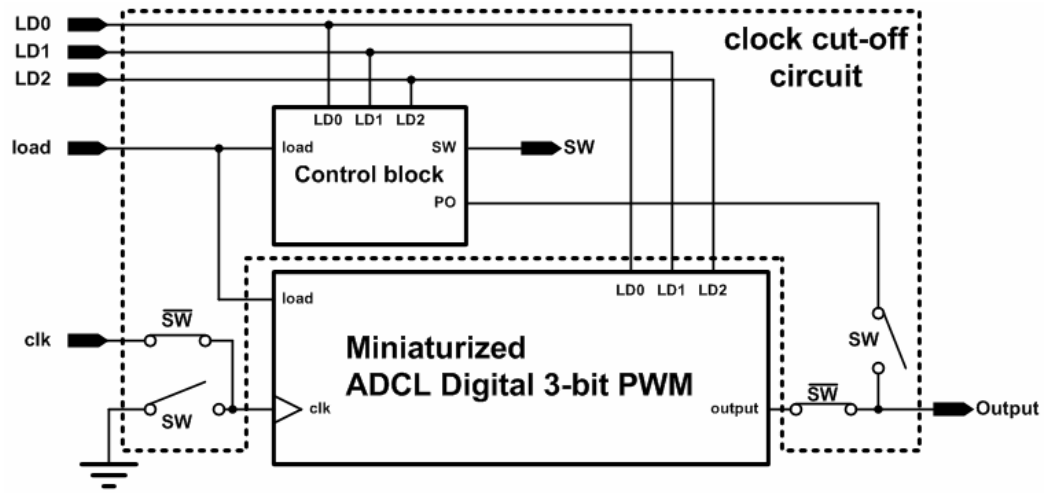


Fig. 4. Designed low-power ADCL PWM.

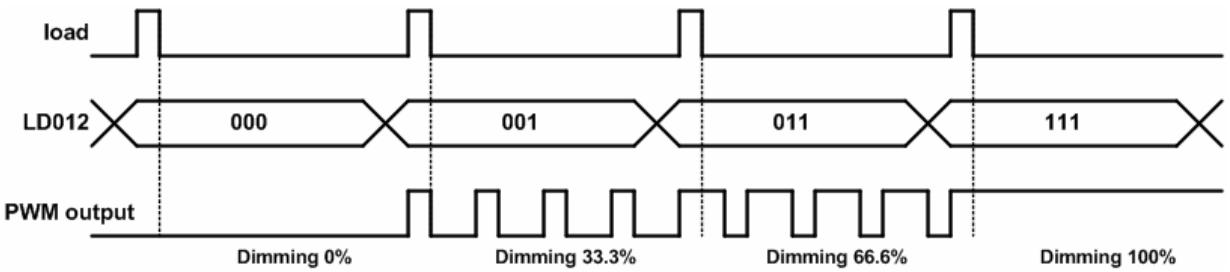


Fig. 5. Timing chart of the digital 3-bit PWM.

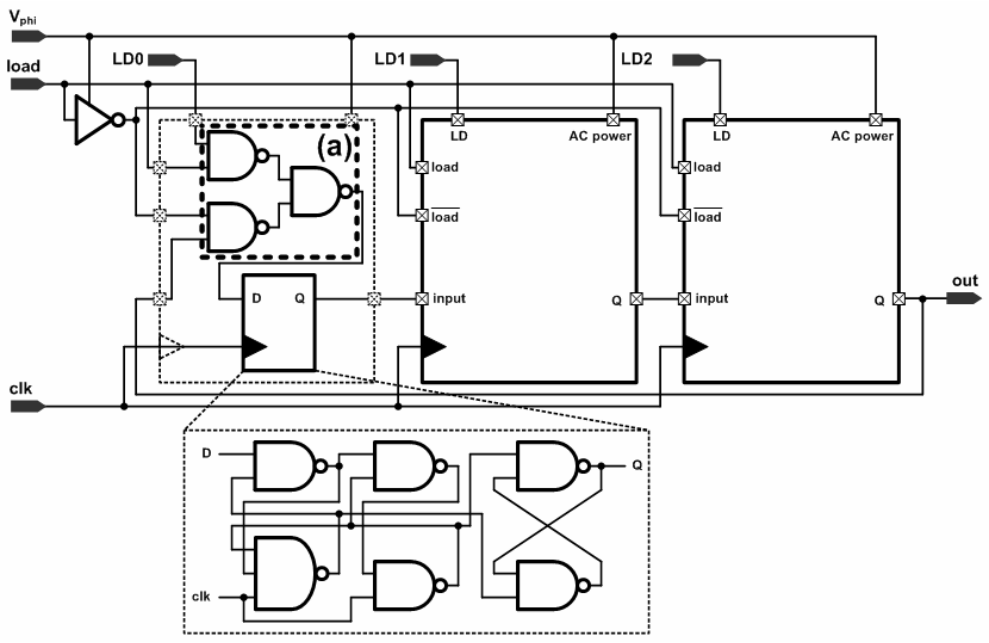


Fig. 6. Miniaturized ADCL digital 3-bit PWM.

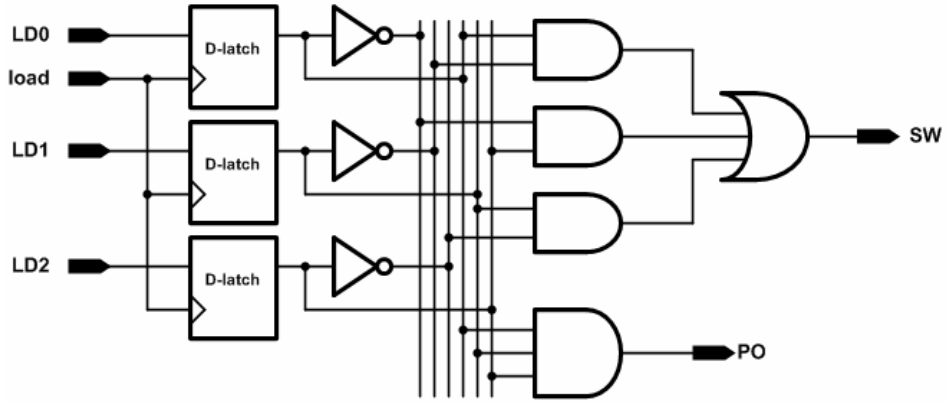


Fig. 7. Control block of the clock cut-off circuit.

Table 1. Comparison of the elements.

	Ref. [3]			This paper		
	No.	Tr.	Cap.	No.	Tr.	Cap.
AND	6	60	12	0	0	0
OR	3	30	6	0	0	0
NAND	0	0	0	9	54	9
D-FF	3	138	24	3	114	18
sum	12	228	42	12	168	27

Table 2. Truth table of proposed control block.

load	LD0	LD1	LD2	SW	PO
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	1	1	0
1	1	1	1	0	1
0	Don't care	Don't care	Don't care	X_{n-1}	X_{n-1}

simulated using PSpice OrCAD 10.3 with 1.2 μm standard MOS level-3. The DC power, AC power and clock were 5 V, 33 kHz sinewave, 3 kHz respectively. Fig. 8 shows the simulation results. The simulation confirmed that the input clock of the ADCL D-ffs is cut off because the SW is high at both input-bits 000 and 111. Moreover, the pulse width of the PWM output becomes 100 % because the PO is a high level at input-bit 111.

The power consumption of the ADCL digital PWM in Ref. [14] and optimized ADCL digital PWM with the proposed clock cut-off circuit in this paper were compared, as shown in Table 3 and Fig. 9. The power consumption of the optimized ADCL digital 3-bit PWM was less than 3 nW at both dimming 0 % and 100 % of the PWM output. Moreover, the power consumption of the optimized ADCL digital PWM for all bit patterns decreased by 54 % compared to that of the ADCL PWM of Ref. [14].

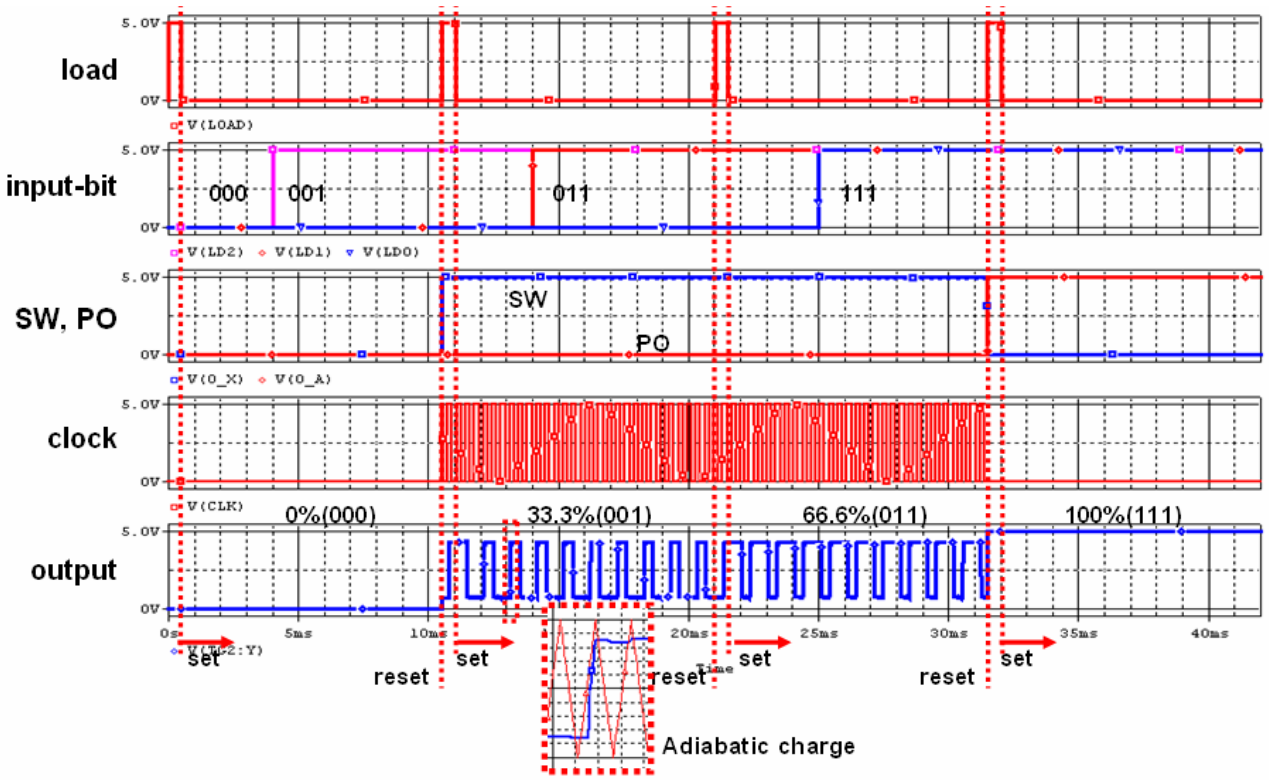


Fig. 8. Simulation results.

Table 3. Comparison of the power consumption.

[nW]

	000	001	011	111
ADCL Digital PWM [14]	243.5	410.8	351.4	81.9
Miniaturized ADCL Digital PWM	78.0	247.0	246.2	78.0
Optimized ADCL Digital PWM	2.6	245.9	248.2	2.8

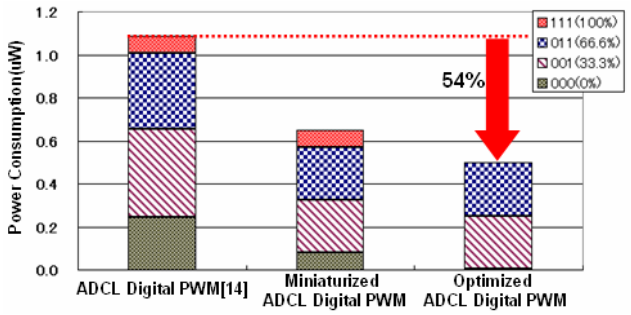


Fig. 9. Comparison of the power consumption.

5. Conclusion

An optimized low-power ADCL digital PWM was designed in two steps for a SSL dimming system. In the first step, the architecture of the ADCL digital 3-bit PWM was miniaturized. In the second step, the clock cut-off circuit, which pauses the ADCL D-ffs to incur power consumption by unnecessary operation at both dimming 0 % and 100 % of PWM output, was designed and added to the ADCL PWM.

Compared to the original configuration, 60 transistors and 15 capacitors of ADCL digital 3-bit PWM were reduced for miniaturization. Furthermore, the power consumption of the optimized ADCL digital PWM was 54 % lower than that of the ADCL digital PWM of Ref. [14] in the simulation because the clock cut-off circuit was used to reduce the unnecessary operations and miniaturized ADCL. This shows the potential of the optimized ADCL PWM in future low-power SSL dimming systems.

References

[1] Wang Feng, J. Huisman, K. Balde, and A. Stevels, "A systematic and compatible classification of WEEE," in Proc. Electronics Goes Green (EGG) 2012, pp1-6, Berlin, Germany, Sept. 2012. Article (CrossRef Link)

[2] O. Deubzer, N.F. Nissen, and K.-D. Lang, "Overview of RoHS 2.0 and status of exemptions," in Proc. Electronics Goes Green (EGG) 2012, pp1-6, Berlin, Germany, Sept. 2012. Article (CrossRef Link)

[3] S. Tarashioon, S.W Koh, W.D van Driel, G.Q. Zhang, "Temperature dependency in performance of solid state lighting drivers," in Proc. 12th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-

electronics and Microsystems, pp1-3, April, 2011. Article (CrossRef Link)
[4] J.Y. Tsao, M.E. Coltrin, Mary H. Crawford, J. A. Simmons, "Solid-State Lighting: An Integrated Human Factors, Technology, and Economic Perspective," Proceeding of the IEEE, vol. 98, no. 7, pp. 1162-1179, July, 2010. Article (CrossRef Link)
[5] B.J. Huang, M.S. Wu, P.C. Hsu, J.W. Chen, K.Y. Chen, "Development of high-performance solar LED lighting system", Energy Conversion and Management, pp1669-1675, vol. 51, no. 8, Aug. 2010. Article (CrossRef Link)
[6] D. Gacio, J.M. Alonso, J. Garcia, L. Campa, M. Crespo and M. Rico-Secades, "High Frequency PWM Dimming Technique for High Power Factor Converters in LED Lighting", in Proc. Applied Power Electronics Conference and Exposition (APEC) 2010, pp743-749, Feb. 2010. Article (CrossRef Link)
[7] Huang-Jen Chiu, Yu-Kang Lo, Jun-Ting Chen, Shih-Jen Cheng, Chung-Yi Lin and Shann-Chyi Mou, "A High-Efficiency Dimmable LED Driver for Low-Power Lighting Applications", IEEE Trans. Ind. Electron., vol. 57, no. 2, pp735-743, Feb. 2010. Article (CrossRef Link)
[8] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzains, and E. Y.-C. Chou, "Low-power digital systems based on adiabatic-switching principles," IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol. 2, no. 4, pp. 398-407, Dec. 1994. Article (CrossRef Link)
[9] A. G. Dickinson and J. S. Dencker, "Adiabatic dynamic logic", IEEE J. Solid-States Circuits., vol. 30, no. 3, pp. 311-315, April 1995. Article (CrossRef Link)
[10] Y. Takahashi, S. Nagano, N.Anuar, T. Sekine, and M.Yokoyama, "On chip LC resonator circuit using an active inductor for adiabatic logic," in Proc. 52nd IEEE International Midwest Symposium on Circuits System. pp.1171-1174, Cancun, Mexico Aug. 2009. Article (CrossRef Link)
[11] N. Anuar, Y. Takahashi, and T. Sekine, "4x4-bit array two phase clock adiabatic static CMOS logic multiplier with new XOR," in Proc. 18th IEEE/IFIP VLSI System on Chip Conference (VLSI-SoC), Madrid, Spain, pp.364-368, Sept. 2010. Article (CrossRef Link)
[12] Y. Takahashi, K. Konta, K. Takahashi, K. Shouno, M. Yokoyama, and M. Mizunuma, "Carry propagation free adder/subtracter using adiabatic dynamic CMOS logic circuit technology", IEICE Trans. Fundamentals., vol. E86-A, no. 6, pp.1437.1444, June 2003. Article (CrossRef Link)
[13] S.-I. Cho, T. Harada, and M. Yokoyama "Design of the ultra low-power synchronizer using ADCL buffer for adiabatic logic," IEICE Electronics Express, vol. 9 No. 20, pp1576-1585, Oct. 2012. Article (CrossRef Link)
[14] S.-I. Cho and M. Yokoyama "Design of low-power PWM for dimming system of the SSL using Adiabatic Dynamic CMOS Logic," in Proc. 2nd Int. Symp. GCSS2012, Kitakyushu, Japan, pp27-30, Apr. 2012. Article (CrossRef Link)
[15] S.-I. Cho, S.-K. Kim, T. Harada, and M. Yokoyama "Design of low-power clock generator synvhronized with AC power for adiabatic dynamic CMOS logic," IEICE Electronics Express, vol. 10 No. 20, pp1-9, Oct. 2013. Article (CrossRef Link)

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