Efficient Multi-site Testing Using ATE Channel Sharing

Kyoung-woon Eom, Dong-kwan Han, Yong Lee, Hak-song Kim, and Sungho Kang

Abstract—**Multi-site testing is considered as a solution to reduce test costs. This paper presents a new channel sharing architecture that enables I/O pins to share automatic test equipment (ATE) channels using simple circuitry such as tri-state buffers, AND gates, and multiple-input signature registers (MISR). The main advantage of the proposed architecture is that it is implemented on probe cards and does not require any additional circuitry on a target device under test (DUT). In addition, the proposed architecture can perform DC parametric testing of the DUT such as leakage testing, even if the different DUTs share the same ATE channels. The simulation results show that the proposed architecture is very efficient and is applicable to both wafer testing and package testing.**

Index Terms—**Multi-site test, channel sharing, probe card, automatic test equipment**

I. INTRODUCTION

The cost of manufacturing testing has steadily increased [1] due to the increased number of transistors on a single die. In addition, enlarging wafer size from 200 mm to 300 mm increases testing costs, even though wafer fabrication time is largely unchanged. When wafer size increases to 450 mm [2], the proportion of test costs to overall manufacturing costs will increase even further.

Multi-site testing is a solution for reducing test costs that reduces the wafer test time by simultaneously testing multiple DUTs [3]. In the traditional multi-site test, all pins of all DUTs are simultaneously connected to each channel. Due to the high pin cost and the restrictions of ATE structures, ATE channels have limited capability. Therefore several approaches have been proposed.

In burn-in test compaction (BITCOM) [4], the MISR is used as a compactor and 64 pin data are transmitted to the ATE. However, BITCOM is not suitable for I/O pins, and cannot handle unspecified bits. Test stimuli broadcasting [5] and the comparator sharing method [6] were proposed but only for dedicated input pins or dedicated output pins. However, most of the pins in integrated circuits (ICs) are I/O pins, so it is inefficient except for the low pin count ICs. In addition, these methods are not suitable for DC parametric testing such as leakage testing. Moreover, it requires additional wafer testing time.

In order to overcome these drawbacks and to maximize the number of multi-sites, a new channel sharing approach is proposed which considers only logic testing and can share I/O pins. It is configured on a probe card and does not require additional circuits on a test target chip.

II. PROPOSED ARCHITECTURE

A block diagram of the proposed ATE channel sharing architecture is shown in Fig. 1. This architecture is composed of a tri-state buffer block, an MISR, and an X-masking block. C-BIT is a control bit that is used for the relay control, and the ATE has equal numbers of channels and C-BITs. P*nm* refers to the *m*-th pin of the *n*-th DUT, while P*m* refers to the *m*-th pin. The test stimuli travel from the ATE to the DUTs through a tri-state buffer block, and the test responses of the DUTs travel to the ATE either directly or indirectly through the MISR and the X-masking block due to the operation of the C-BITs.

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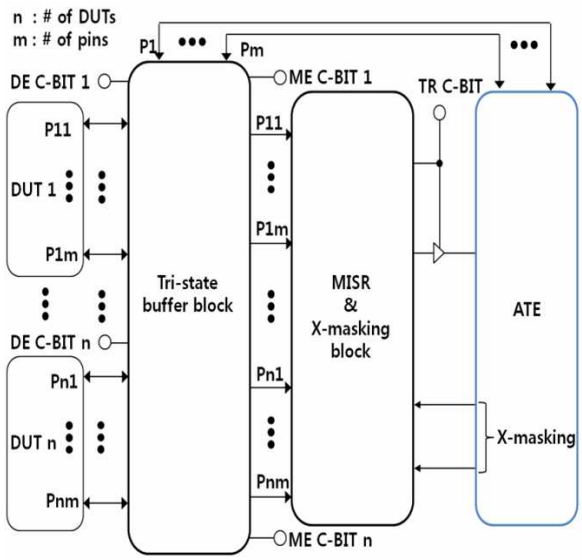


Fig. 1. Block diagram of ATE channel sharing architecture.

1. Tri-state Buffer Block

Fig. 2 shows the tri-state buffer block in detail. A single DUT Enable C-BIT (DE C-BIT) is connected to the active low tri-state buffers of each DUT. The primary function of the tri-state buffers is to disconnect DUTs that fails the manufacturing test. The DC parametric test is performed serially, and can effectively disconnect the failed DUT in order to reduce the wafer test time when the yield is low. The secondary function of the buffers is to create an indirect path for the test responses of the DUT. A single ATE channel can broadcast the test stimuli to multiple pins; however, because of signal-mixing, a single ATE channel cannot simultaneously accept multiple responses. Tri-state buffers prevent the test response from traveling directly to the ATE channel.

The MISR Enable C-BIT (ME C-BIT) is connected to both active high and active low tri-state buffers. Only one of the two tri-state buffers can be activated during testing. When the active low tri-state buffers are turned on, the test response can be transmitted to the MISR for compaction. In this mode, the active high tri-state buffers separate each DUT. If there is not an active high tri-state buffer, unwanted test responses from other DUTs become noise. In addition, active high tri-state buffers are used for directly transmitting the test responses to the ATE. In this mode, the DC parametric values can be tested by parametric management unit (PMU) of the ATE. A Shmoo plot can also be acquired in this mode.

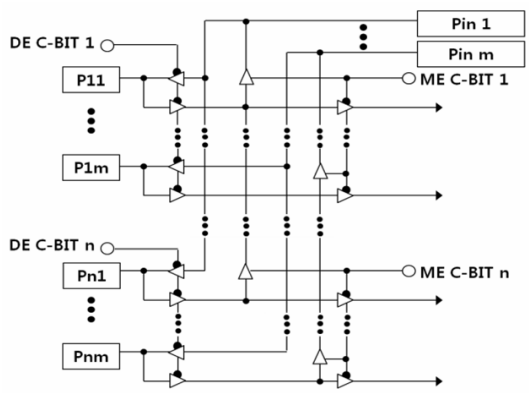


Fig. 2. Tri-state buffer block.

However, because a shared ATE channel can test only one DUT at a time, other DUTs should be disconnected.

2. X-masking

A normal ATE test pattern consists of 1, 0, H, L, and X. In the logic test, many unspecified bits are included in the test responses. The unspecified bit might occur during the transition of the test response. The test signal travels through several connections, and the impedance of each connection is marginally different between test systems. If the test response of the DUT varies with the ATE or test conditions, a stable manufacturing test cannot be performed. To address this problem, X is used. To perform data compaction, unspecified bits should be changed to specified bits. X-masking is used to change the unspecified values from the DUT to specified values.

3. MISR Block

In the proposed architecture, each DUT has a single MISR, and each MISR is serially connected to reduce the transmitting channel count. All of the serially-connected MISRs forward the compaction data to the ATE, and only a single ATE channel is required for transmitting the compaction data.

4. Power Management

The number of power supplies is tens to hundreds depending on the ATE type. If the number of power supplies is insufficient for the proposed architecture, the power dividing method or regulator power can deal with

the power shortage.

III. PERFORMANCE EVALUATION

Eq. (1) shows the wafer test time *TW* for a traditional multi-site test, where *TFC* is the functional test time of a single chip, and T_{DC} is the DC parametric test time of a single chip. N_S is the number of shots (the number of wafer contacts with the probe card) during wafer testing, and T_I is the index time required to move the probe card onto the next DUT. T_C is the time needed for cleaning the probe card tips.

$$TW = (TFC + TDC) \times NS + TI \times NS + TC \quad (1)$$

The wafer test time of the single test set T_{WS} is shown in Eq. (2) where N_C is the number of chips to be tested.

$$TWS = TFC \times NS + TDC \times NC + TI \times NS + TC \quad (2)$$

To perform DC parametric tests on all DUTs simultaneously, a multi-set architecture is used which is the combination of several structures. Wafer test time of the multi set T_{WM} is shown in Eq. (3), where the DC parametric test time T_{MDC} is T_{DC} divided by the number of test sets to reduce the DC parametric test time.

$$TWM = TFC \times NS + TMDC \times NC + TI \times NS + TC \quad (3)$$

To evaluate the wafer test time, the required conditions are assumed as listed below.

(1) The functional test time T_{FC} is 4.6 sec, the DC parametric test time T_{DC} is 0.4 sec, and the index time T_I is 0.7 sec.

(2) The ATE has 256 channels.

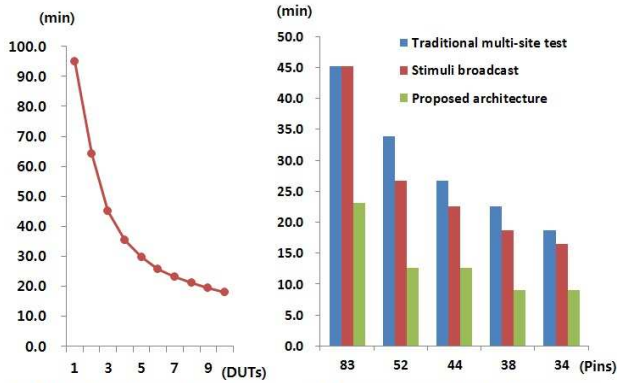
(3) The tip cleaning time T_C is 1 minute for each cleaning shot and the tip cleaning is performed every 100 chips.

(4) The number of pins does not affect the chip test time.

(5) Since the wafer is round, this paper assumes that a multi-site test has 30% more shots than with a rectangular wafer.

(6) The total number of chips on a wafer is 1,000.

(7) The total number of input pins is 3 (test, reset, clock).The others are all I/O pins.



(a) Water test time of single set (b) Comparison of water test times

Fig. 3. Performance evaluation.

Fig. 3(a) shows the wafer test time as a function of the number of DUTs connected to a single test set. The wafer test time of a single set is saturated at close to 8 DUTs. A test set of eight DUTs is adopted in this paper based on the current driving performance of the ATE channel and the test time trend. Fig. 3(b) shows the comparison of wafer test times. The proposed architecture demonstrates a more than 40% reduction in test time compared with the traditional multi-site test architecture, whereas there is not a large difference in test time between the traditional multi-site test and the stimuli broadcasting method.

IV. CONCLUSIONS

In this paper, a new channel sharing architecture is proposed for multi-site testing in order to decrease the wafer test time. The proposed architecture consists of several simple blocks, and shows a superior reduction in test time as compared to the traditional multi-site test. Future works will address implementation and calibration issues in order to allow for easy adaption in the field.

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