JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.13, NO.3, JUNE, 2013 http://dx.doi.org/10.5573/JSTS.2013.13.3.245

The Optimal Design of Junctionless Transistors with Double-Gate Structure for reducing the Effect of Band-to-Band Tunneling

Meile Wu*, Xiaoshi Jin*, Hyuck-In Kwon*, Rongyan Chuai*, Xi Liu*, and Jong-Ho Lee****

***Abstract*—The effect of band-to-band tunneling (BTBT) leads to an obvious increase of the leakage current of junctionless (JL) transistors in the OFF state. In this paper, we propose an effective method to decline the influence of BTBT with the example of n-type double gate (DG) JL metal-oxide-semiconductor field-effect transistors (MOSFETs). The leakage current is restrained by changing the geometrical shape and the physical dimension of the gate of the device. The optimal design of the JL MOSFET is indicated for reducing the effect of BTBT through simulation and analysis.**

***Index Terms*—Band-to-band tunneling (BTBT), double-gate (DG), junctionless field-effect transistor (JL FET), device simulation, optimal design**

I. INTRODUCTION

Multi-gate structure which contains double-gate (DG), surrounding-gate and Tri-gate is considered to be a formidable candidate when metal-oxide-semiconductor field-effect transistors (MOSFETs) dimensions are scaled down extremely due to its inhibition of the serious influence of short channel effect (SCE). However, classical transistors with multi-gates still have to face the challenge of ultrasharp doping profile. Recently, junctionless (JL) MOSFETs which have no doping concentration gradient between source / drain (S / D) region and body region are proposed. The JL MOSFET contains a silicon nanowire which needs a high doping concentration to realize amount of current flowing in the ON state [1]. The channel of the JL MOSFET is depleted by piping out the electrons (n-channel) or holes (p-channel) from the body region at lower gate bias, which causes low current in the OFF state. With the increase of gate bias, the depletion is reduced gradually. When the channel region under the gate becomes electrically neutral, an accumulation of carriers appear at the interface between the silicon nanowire and oxide near the gate electrode with further rise of gate bias. While, take an n-type JL MOSFET as an example; the valence and conduction bands of electrons in the silicon nanowire under the gate are higher than source and drain regions due to the depletion in the channel of the device. The exacerbation of the depletion creates an overlap between the valence and conduction bands in the channel and the drain separately, which results in a tunneling of electrons between the two bands. This is the effect of band-to-band tunneling (BTBT) that leads to a significant leakage current in the OFF state [2]. It means that the higher doping concentration of silicon nanowire triggers larger effect of BTBT.

At present, some research groups have already studied the JL MOSFETs with multi-gate structures systematically and detailedly. The theoretical foundations of JL FETs with double-gate [3], analysis of turned on characteristics of JL nanowire FET at different drain

Manuscript received Dec. 3, 2012; accepted Jan. 28, 2013.
* School of Information Science and Engineering, Shenyang University of Technology, Shenyang 110870, China
** School of EECS Eng. and ISRC (Inter-University Semiconductor Research Center), Seoul National University, Shinlim-Dong, Kwanak-Gu, Seoul 151-742, Korea
*** School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 156-756, Korea
E-mail : xsjin@live.cn

voltages and the potential under various operating conditions [4], discrete doping-induced variability in junctionless nanowire MOSFETs using dissipative quantum transport simulations [5], the impact of random dopant fluctuation for several JL FinFET [6], et al can be searched. Furthermore, some modeling results such as theoretical model of the JL silicon-on-insulator (SOI) FET [7] and a charge-based model of DG MOSFETs [8] have been reported. Some groups studied the OFF-state behavior of JLTs, and showed the effect of BTBT on JLT operating in volume depletion in OFF state [2]. In consideration of the significant influence of BTBT, it is necessary to propose an effective way to decrease it. In this paper, we present a method which includes the change of the geometrical shape and the physical dimension of the gate of the device with the example of n-type DG MOSFETs. The method is explored and demonstrated through TCAD simulations with Band-Band (standard) model picking from band-to-band models by SILVACO [9].

II. Description and Simulation Setup

The 2D schematic view of the reference DG JL FET is shown as Fig. 1(a). Here, L and t_b are the length and body thickness of the device separately, t_{ox} is the gate oxide thickness and t_{sp} represents the vertical distance between gate sidewall and source/drain contacts. Fig. 1(b) shows the modified structure of the DG JL FET. In the Fig., the values of t_l and t_h are the change of t_{sp} and t_{ox}. Through these modifies, the value of t_{sp} and t_{ox} are increased to t_{sp}' and t_{ox}', which decline the exhaustion of the channel in the body under the modified part of the gate. Then the energy band distributions of the carriers in the silicon nanowire near the gate sidewall are changed. It slows down the reduction of energy band in the body from the gate region to the drain and source regions of the device, then lessen the overlap between the valence and conduction bands in the channel and the drain separately to reduce the effect of BTBT. The simulation parameters of the DG JL devices are listed in Table 1.

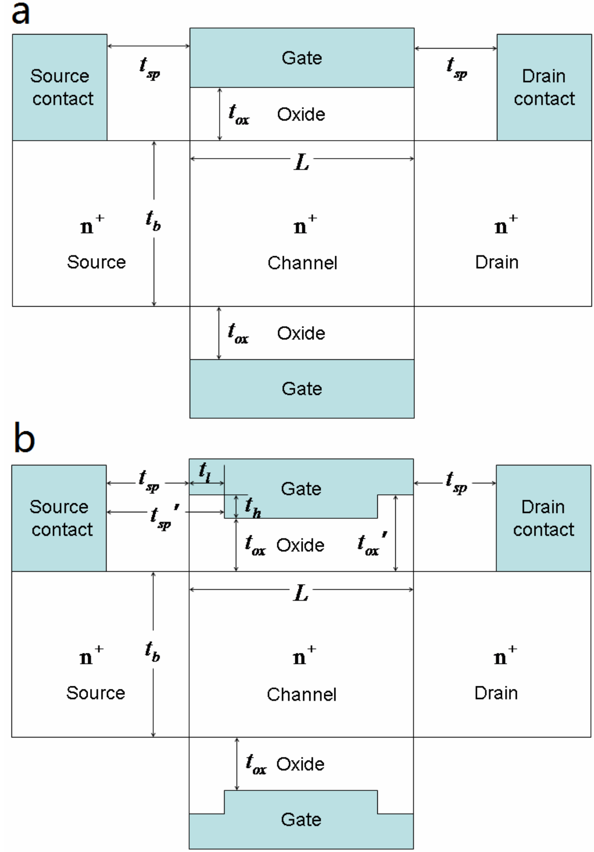

Fig. 1. The 2D schematic view of the reference (a) and the modified, (b) DG JL FETs. L and t_b are the length and body thickness of the devices separately, t_{ox} is the gate oxide thickness and t_{sp} represents the vertical distance between gate sidewall and source/drain contacts. t_l and t_h are the height and length of the thickly formed gate oxide near the both edges of the gate, t_{sp} and t_{ox} are increased to t_{sp}' and t_{ox}', respectively.

Table 1. Parameters Used for Simulated DG JL FETs

parameters	values
Channel length (L);	15 nm
Body thickness (t_b);	10 nm
Doping concentration (N_d);	10^{19} cm^{-3}
Reference oxide thickness (t_{ox});	0.8 nm
Reference vertical distance between gate sidewall and source/drain contacts (t_{sp});	5 nm
Height of the thickly formed gate oxide near both edges of the gate (t_h);	From 0.2 nm to 1.4 nm with a step of 0.2 nm
Length of the thickly formed gate oxide near both edges of the gate (t_l);	From 0.5 nm to 4.5 nm with a step of 0.5 nm
Modified oxide thickness (t_{ox}');	From 1.0 nm to 2.2 nm with a step of 0.2 nm
Modified vertical distance between gate sidewall and source/drain contacts (t_{sp}');	From 5.5 nm to 9.5 nm with a step of 0.5 nm

III. SIMULATIONS AND ANALYSES

Fig. 2 shows the conduction and valence bands of reference DG JL FET at different V_{DS} and V_{GS}. In the OFF state (V_{GS}=-1.5 V), the effect of BTBT is apparently observed especially at higher V_{DS} (V_{DS}=1.0 V) according to the simulation results. However, the influence of BTBT can be reduced by making the gate oxide thickness near both edges of the gate relatively thick as shown in Fig. 1(b), since the thick edge oxide makes the band bending relatively slow. The values of t_l and t_h are the height and length of the thickly formed gate oxide near the both edges of the gate. By changing the two values, the energy bands of carriers in the silicon near the gate edge can be changed.

Firstly, the t_h is set to be 0.7 nm (t_{ox}=0.8 nm, t_{ox}'=1.5 nm in total gate oxide thickness near the gate edge) and the value of t_l is increased from 0.5 nm to 4.5 nm with a step of 0.5 nm. The simulated energy band diagrams of the DG JL FETs biased at V_{DS}=0.2 V and V_{GS}=-1.5 V are shown in Fig. 3(a).

Fig. 3(b) represents the valence band of the channel in a part of the band bending between the channel and the drain region. From Fig. 3(b), we can clearly see that from the channel edge region to the drain region, the band bending is obviously decreased by the rise of t_l, which will cause a lower possibility of the tunneling of electrons from the valence band of the channel to the conduction band of the drain. When t_l is increased to 2.0 nm, the decrease of the band bending is insignificant

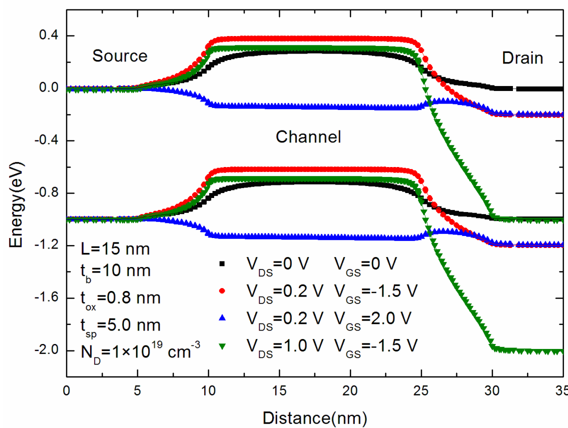

Fig. 2. Conduction and valence bands of reference DG JL FET with L=15 nm, t_b =10nm, N_d =10^{19} cm $^{-3}$, t_{sp} =5 nm and t_{ox} =0.8 nm at different V_{DS} and V_{GS}.

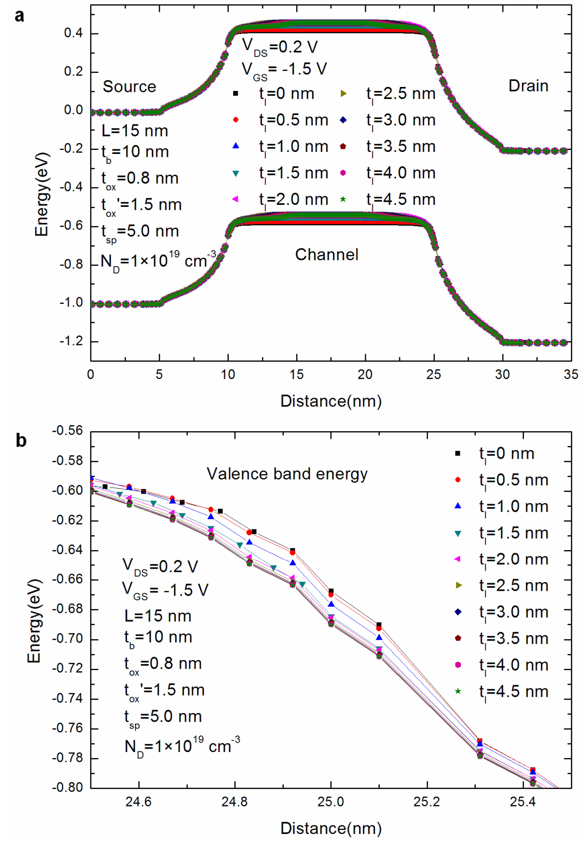

Fig. 3. (a) Energy bands of the DG JL FETs with t_{ox}=0.8 nm, t_{ox}'=1.5 nm, t_{sp}=5 nm and t_l ranging between 0nm and 4.5 nm biased at V_{DS}=0.2V and V_{GS}=-1.5V, (b) Valence band of the channel in the part of the band bending between the channel and the drain region.

with the further rising of t_l. Fig. 4(a) illustrates the I-V characteristics of 15 nm DG JL FETs biased at a fixed V_{DS} of 0.2 V. The curves in ON and OFF states are plotted in Fig. 4(b) and (c), respectively. Overall, the increase of t_l reduces the leakage current in the OFF state and conduction current in the ON state concurrently. It can be seen that the diminution of leakage current is inconspicuous after t_l reaches 2.0 nm while the conduction current still keeps dropping from Fig. 4(a) and (b). Note the current in ON state decreases much slowly compared to that of the current OFF state. We calculate the threshold voltage difference (ΔV_{TH}) between the V_{TH} of the modified DG JL FETs with t_l=0.5 nm to 4.5 nm and the one of the reference DG JL FET. The ΔV_{TH}-t_l is shown in Fig. 5(a) and ΔV_{TH} decreases with the increase of t_l. Simultaneously, the Subthreshold slope (SS) increases with the increase of t_l according to the curve of SS-t_l which is plotted in Fig.

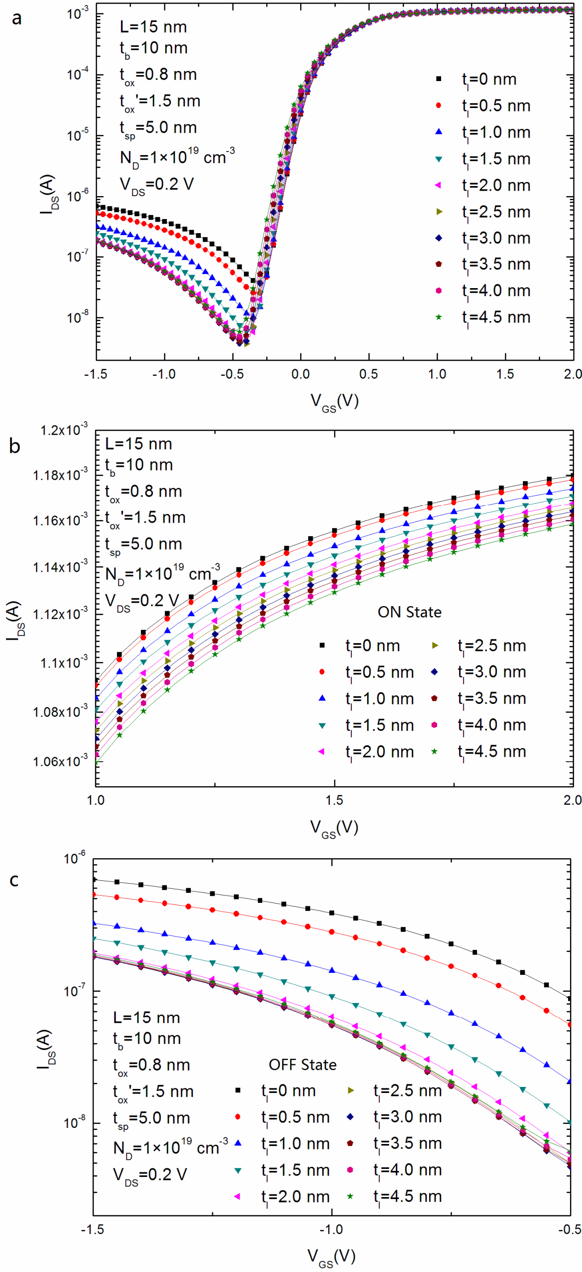

Fig. 4. (a) I-V characteristics of the DG JL FETs with t_{ox} =0.8 nm, t_{ox}'=1.5 nm, t_{sp} =5 nm and t_l ranging between 0nm and 4.5 nm biased at V_{DS}=0.2V, (b) Curves of the current in the ON state, (c) Curves of the current in the OFF state. The increase of t_l reduces the leakage current in the OFF state and conduction current in the ON state. The diminution of leakage current is inconspicuous after t_l reaches 2.0 nm while the conduction current still keeps dropping.

5(b). All the above aspects considered, t_l =2.0 nm (t_{sp}'=7 nm) is the appropriate choice with a certain t_{ox} for DG JL FETs to restrain the impact of BTBT. As the t_l increases, the gate oxide thickness from both edges of the gate increases, which is inferior to suppress the

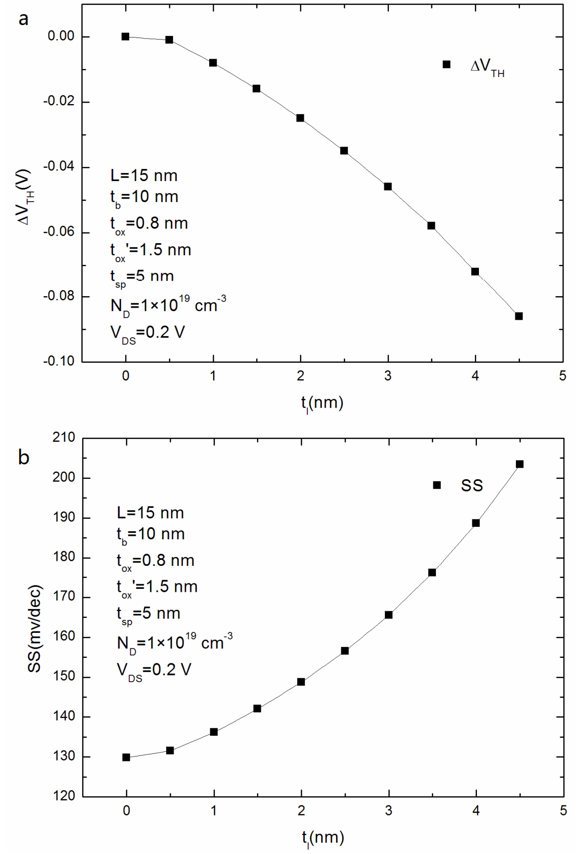

Fig. 5. (a) Curve of ΔV_{TH} - t_h . ΔV_{TH} is the difference between V_{TH} of the modified DG JL FETs with t_l =0.5nm to 4.5nm and the one of the reference DG JL FET, (b) Curve of SS- t_l . With the increase of t_l , ΔV_{TH} decreases and SS increases.

electric field penetration to the source. Therefore, short channel effect is increased, resulting in the decrease of V_{TH} and the increase of SS with increasing t_l .

Now t_l is set to 2.0 nm and change the value of t_h to find an optimum one through the same method. Fig. 6(a) shows simulated energy bands of the DG JL FETs biased at V_{GS}=-1.5 V and V_{DS}=0.2 V by changing t_h from 0 nm to 1.4 nm. The band bending between the channel and the drain region of the eight DG JL FETs are plotted in Fig. 6(b), respectively. The band bending in this area is decreased by the rising of t_h. Hence the suppression of the BTBT is more evident with the higher value of t_h . The I-V characteristics of these DG JL FETs at V_{DS}=0.2 V are represented in Fig. 7(a), which shows that the conduction current in the ON state and the leakage current in the OFF state are both decreased with increasing t_h . In the Fig. 7(b) and (c) which illustrate

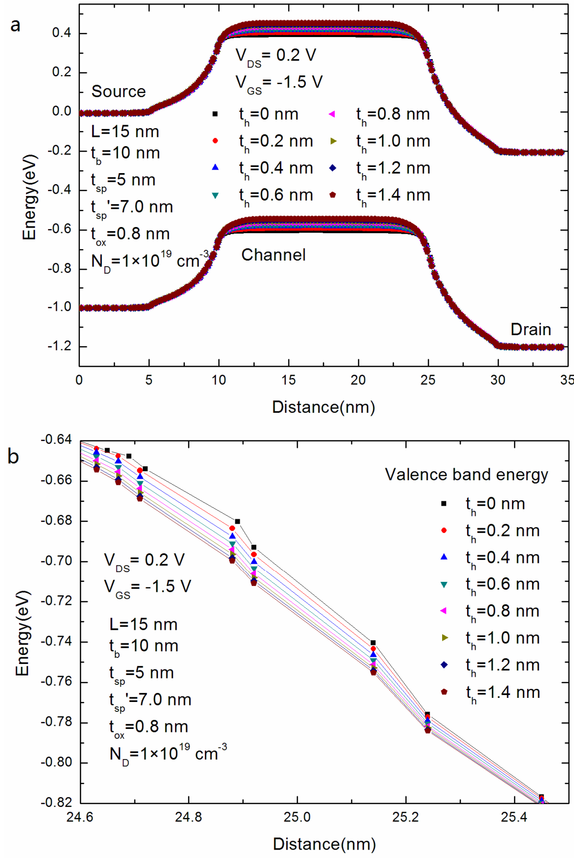

Fig. 6. (a) Energy bands of the DG JL FETs with t_{ox} =0.8 nm, t_{sp} =5 nm, t_{sp}' =7 nm and t_h ranging between 0 nm and 1.4 nm biased at V_{DS}=0.2V and V_{GS}=-1.5V, (b) Valence band of the channel in the part of the band bending between the channel and the drain region of the eight DG JL FETs. The band bending in this area is decreased by the rising of t_h .

the curves of the current in the ON and OFF state severally, it can be seen that the lessening of the current in the two states are both very small after t_h reaches 1.0 nm. Fig. 8(a) and (b) describe the curves of ΔV_{TH} - t_h and SS- t_h respectively. With the increase of t_h , ΔV_{TH} decreases and SS increases. Moreover, the increasing rate of the ΔV_{TH} slows down after t_h reaches 1.0 nm. By considering all above aspects, we choose t_l =2.0 nm and t_h =1.0 nm as an optimum parameters for reducing the effect of BTBT for 15 nm DG JL FETs.

IV. Conclusions

We have proposed an approach to reduce the effect of BTBT by selectively increasing the thickness of the gate oxide near both edges of the gate of double-gate

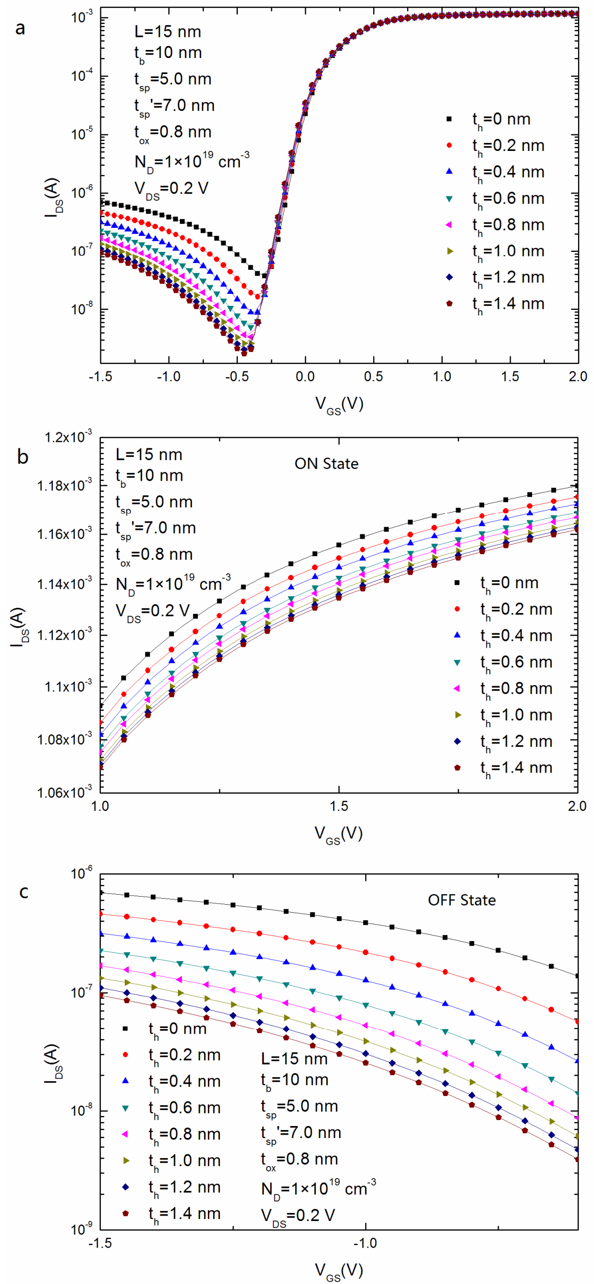

Fig. 7. (a) I-V characteristics of the DG JL FETs with t_{ox} =0.8 nm, t_{sp} =5 nm, t_{sp}' =7 nm and t_h ranging between 0nm and 1.4 nm biased at V_{DS}=0.2V, (b) Curves of the current in the ON state, (c) Curves of the current in the OFF state. Both of the two kinds of current decrease with the increase of t_h .

junction-less FET. The energy bands of carriers in the silicon nanowire under this area are reformed by changing the geometric parameters of the thickly formed gate oxide. Finally we have selected t_l =2.0 nm and t_h =1.0 nm as the optimal design parameters in the condition of the DG JL FETs with L=15 nm, t_b =10 nm,

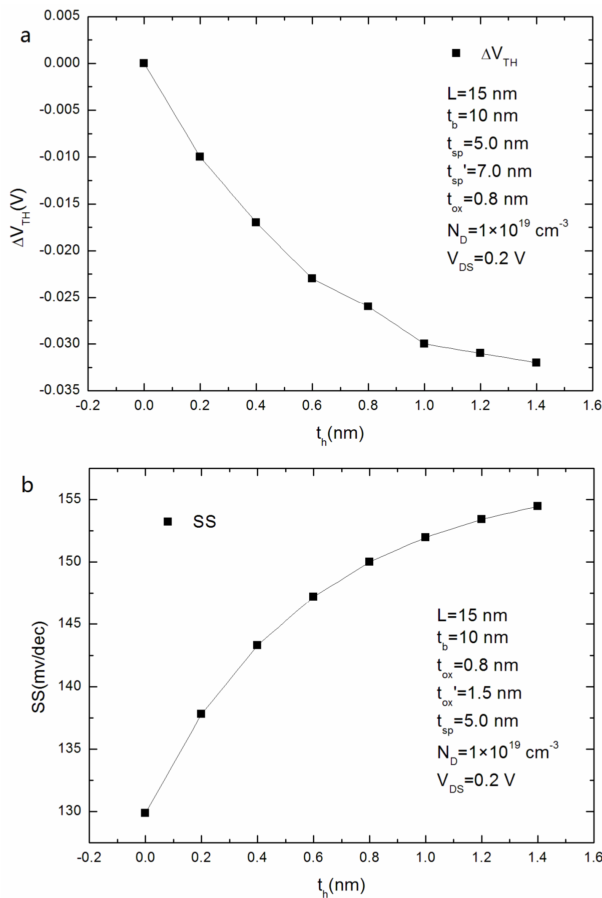

Fig. 8. (a) Curve of ΔV_{TH} - t_h. ΔV_{TH} is the difference between V_{TH} of the modified DG JL FETs with t_h =0.2 nm to 1.4 nm and the one of the reference DG JL FET, (b) Curve of SS- t_h. With the increase of t_h, ΔV_{TH} decreases and SS increases.

N_d =10^{19} cm^{-3} by considering current of ON and OFF states, the changing of ΔV_{TH} and SS, et al. The most reasonable design of the JL FETs with other geometric parameters can be given by this method for controlling the influence of BTBT.

ACKNOWLEDGEMENT

This Project is supported by the Fund of Liaoning Province Education Department (No. L2012028).

REFERENCES

[1] Jean-Pierre Colinge, Chi-Woo Lee, Aryan Afzalian, et al. Nanowire transistors without junctions. Nat. Nanotechnology, 2010, 5 (3): 225–229.

[2] Suresh Gundapaneni, Mohit Bajaj,Rajan K. Pajan, et al.Effect of band- to-band tunneling on junctionless transistors. IEEE Transactions on Electron Devices, 2012, 59 (4) : 1023-1029.

[3] Elena Gnani, Antonio Gnudi, Susanna Reggiani, et al. Theory of the junctionless nanowire FET. IEEE Transactions on Electron Devices, 2011, 58 (9): 2903-2910.

[4] E. Gnani, A. Gnudi, S. Reggiani, et al. Numerical investigation on the junctionless nanowire FET. Solid-State Electronic, 2012, 71: 13-18.

[5] Manuel Aldegunde, Antonio Martinez, John R. Barker, et al. Study of discrete doping-induced variability in junctionless nanowire MOSFETs using dissipative quantum transport simulations. IEEE Electron Device Letters, 2012, 33 (2): 194-196.

[6] Greg Leung, Chi On Chui. Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs. IEEE Electron Device Letters, 2012, 33 (6): 767-769.

[7] Elena Gnani, Antonio Gnudi, Susanna Reggiani, et al. Physical model of the junctionless utb soi-fet. Science of Advanced Materials, 2011, 3 (3): 477-482.

[8] Jean-Michel Sallese, Nicolas Chevillon, Christophe Lallement, et al. Charge-Based Modeling of Junctionless Double-Gate Field-Effect Transistors. IEEE Transactions on Electron Devices, 2011, 58 (8): 2628-2636.

[9] SILVACO International. ATLAS User’s Manual, 2005.

Meile Wu received the B.S. degree in electronics science and technology from Shenyang University of Technology, Shenyang, China, in 2012. She is currently working toward the M.S. degree in the School of Information Science and Engineering, Shenyang University of Technology, Shenyang, China. Her research interests include design and optimization of nanoscale junctionless MOSFETs devices and high accuracy A/D and D/A converter.

Xiaoshi Jin received the B.S. degree in physics from Dalian University of Technology, Dalian, China, in 2004, the M.S. degree in physics from Gyeongsang National University, Jinju, Korea, in 2006 and the Ph.D. degree in semiconductor and display engineering from Kyungpook National University, Daegu, Korea, in 2010. Since 2010, he works in the School of Information Science and Engineering, Shenyang University of Technology as an assistant professor. His research interests include semiconductor physics and device modeling, design of advanced semiconductor devices and optimization of RF and analog circuits.

Hyuck-In Kwon was born in Seoul, Korea, in 1976. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, in 1999, 2001, and 2005, respectively. From August 2004 to March 2006, he was a Research Associate with the University of Illinois, Urbana. In 2006, he joined the System LSI Division, Samsung Electronics Company, Korea, where he was a Senior Engineer with the Image Development Team. From September 2007 to February 2010, he worked for the School of Electronic Engineering in Daegu University as a Full-Time Lecturer and an assistant professor. Since 2010, he has been with Chung-Ang University, Seoul, Korea, where he is currently an assistant professor in the School of Electrical and Electronics Engineering. His research interests include CMOS active pixel image sensors, oxide thin-film transistors, GaN-based power devices, and silicon nanotechnologies.

Rongyan Chuai was born in 1963. He received the Ph.D. degree from HIT (harbin Institute of Technology), harbin, China. He works in the School of Information Science and Technology, Shenyang, China as a professor. His research interests include semiconductor physics, design of devices and MEMS technology.

Xi Liu received the B.S. and M.S. degrees in applied mathematics from Dalian University of Technology, Dalian, China, in 2004 and 2006, respectively. She received the Ph.D. degree in semiconductor and display engineering from Kyungpook National University, Daegu, Korea, in 2010. Since 2010, he works in the School of Information Science and Engineering, Shenyang University of Technology as an assistant professor. Her research interests include design and optimization of nanoscale integrated circuits and devices, nonlinearity problems in integrated circuits, design of RF and analog circuits.

Jong-Ho Lee received the Ph.D. degree from Seoul National University, Seoul, in 1993, in electronic engineering. In 1994, he was with the School of Electrical Engineering, Wonkwang University, Iksan, Chonpuk, Korea. In 2002, he moved to Kyungpook National University, Daegu Korea, as a Professor of the School of Electrical Engineering and Computer Science. Since September 2009, he has been a Professor in the School of Electrical Engineering, Seoul National University, Seoul Korea. From August 1998 to July 1999, he was with Massachusetts Institute of Technology, Cambridge, as a postdoctoral fellow. He has authored or coauthored more than 160 papers published in refereed journals and over 280 conference papers related to his research and has been granted ~90 patents in this area. His research interests include CMOS technology, non-volatile memory devices, thin film transistors, sensors, bio interface, and neuromorphic technology. He has been served as a subcommittee member of IEDM, ITRS ERD member, a general chair of IPFA2011, and IEEE EDS Korea chapter chair. In 2006, he was a recipient of the “This Month’s Scientist Award” for his contribution in the development of practical high-density/high-performance 3-dimensional nano-scale CMOS devices. He invented Saddle FinFET (or recess FinFET) for DRAM cell and NAND flash cell string with virtual source/drain, which have been applying for mass production.