A Unified Channel Thermal Noise Model for Short Channel MOS Transistors

Sang Dae Yu

***Abstract*—A unified channel thermal noise model valid in all operation regions is presented for short channel MOS transistors. It is based on smooth interpolation between weak and strong inversion models and consistent physical model including velocity saturation, channel length modulation, and carrier heating. From testing for noise benchmark and comparing with published noise data, it is shown that the proposed noise model could be useful in simulating the MOSFET channel thermal noise in all operation regions.**

***Index Terms*—Unified channel thermal noise model, all region noise model, interpolation approach, BSIM3 noise model, short channel effect**

I. INTRODUCTION

Circuit design for reducing the power consumption of electronic systems is the ultimate goal of every circuit designer. For this low power design, it is essential to use low voltage and low current circuits. This fact means that MOSFETs in the low power circuit can operate in the weak or moderate inversion region [1, 2]. As a result, noise characteristic as well as electrical characteristics of transistors in these regions becomes more important. Therefore, the noise behavior of short channel MOS transistors should be well modeled from strong inversion through moderate inversion into weak inversion.

It has been observed that short channel MOS devices have somewhat higher channel thermal noise than long channel devices in the strong inversion and saturation region [3-5]. And it is known that this phenomenon is due to short channel effects associated with velocity saturation (VS), channel length modulation (CLM), and carrier heating (CH). As a result of accounting for these effects, it was shown that the dominant contribution to the drain current noise mainly comes from the linear channel region [3]. Nevertheless, this issue of *excess* noise is still an active area of investigation [1].

There are some unified channel thermal noise models for all quasi-static (QS) operation regions, namely weak to strong inversion and linear to saturation region. One is based on the MM11 or PSP model [6], another the EKV model [7], and a third the BSIM3 model [8]. The difference among these noise models lies in the way the short channel effects are realized within the framework of each compact transistor model. The channel thermal noise is mainly dependent on carrier mobility and inversion charge density. In above EKV and BSIM models, the effective electron mobility is modeled as $\mu_0/(1+E_x/E_c)$, while it is modeled as $\sqrt{\mu_0/(1+E_x/E_c)}$ in the PSP model. The PSP model is a surface potential based model in which the inversion charge density is computed from surface potential. The EKV model has been reformulated as an inversion charge based model since version 2.8. Because these models give a continuous inversion charge density throughout all operation regions, a unified thermal noise model can be consistently implemented without interpolation in their own compact model. But very accurate evaluation of surface potential or inversion charge density from *implicit* nonlinear equations is generally considered to be computationally expensive.

Manuscript received Sep. 22, 2012; accepted Jan. 28, 2013
School of Electronics Engineering, Kyungpook National University
1370 Sankyuk-dong, Buk-gu, Daegu 702-701, Korea
E-mail : sdyu@mail.knu.ac.kr

On the other hand, the BSIM3 model is a threshold voltage based model in which the inversion charge density is described by separate expressions for different operation regions. To obtain the unified model ensuring numerical continuity, such expressions are combined into a single expression with suitable interpolation. As a result, the inversion charge density can be efficiently computed from *explicit* functions of terminal voltages.

It is likely that integrated circuits have been designed with the BSIM3 model more than with any other compact model [1]. However, the BSIM3 noise model to account for the short channel effects has not yet been implemented in Spice. Moreover, in the previous BSIM3 based noise model [8], it was ignored that the velocity saturation is absent in weak inversion. So its noise predictions will be incorrect in weak inversion. In this article, a *unified* channel thermal noise model based on the *interpolation* approach and valid in *all* operation regions will be presented for the BSIM3 compact model. In addition, non-quasi-static (NQS) effect and extrinsic noises showing frequency dependence in power spectral density will be described, and a channel length limit for validity of the drift diffusion model used in noise analysis will be discussed. Finally the noise predictions of the proposed model will be compared with published noise data.

II. UNIFIED THERMAL NOISE MODELING

1. Linear Drain Current

Using the inversion charge density Q_i valid from weak to strong inversion, the general expression to account for both drift and diffusion currents in channel is given by

$$I_{d0} = \mu_{\text{eff}} W Q_i \frac{dV_c}{dx} \tag{1}$$

where V_c is the channel voltage at point x with respect to the source. Besides, Q_i in the *linear* region is given by $C_{ox} V_{gsteff}(1 - V_c / V_b)$, V_b is given by $(V_{gsteff} + 2V_T) / A_{\text{bulk}}$, and V_{gsteff} is the effective overdrive voltage [9]. In order to consider velocity saturation in many compact models as well as BSIM3, the effective mobility has been modeled as

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + E_x / E_c} \tag{2}$$

where μ_0 is the low lateral field mobility including mobility reduction due to the vertical field. Using the surface potential ϕ_s, the magnitude of lateral electric field is given by $E_x = d\phi_s / dx$. In strong inversion and linear region, E_x can be approximated as dV_c / dx. The critical electric field and the saturated drift velocity are related by $E_c = 2v_{\text{sat}} / \mu_0$. By integrating (1) over the electrical channel length L_e shown in Fig. 1, the unified expression for the drain dc current in the all linear channel regions can be obtained as

$$I_{d0} = \frac{g_0 V_{ceff}(1 - V_{ceff}/2V_b)}{(L_c / L_{eff})} \tag{3}$$

where V_{ceff} is the effective channel voltage, L_c is given by $L_e(1 + V_{ceff} / L_e E_c)$, and g_0 is given by $\mu_0 W C_{ox} V_{gsteff} / L_{eff}$.

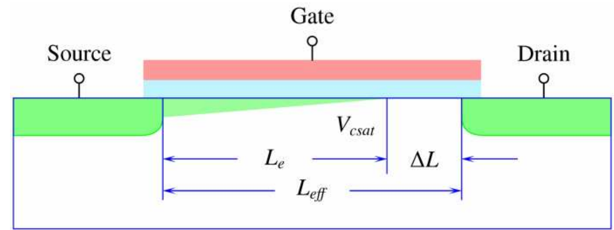

Fig. 1. Channel cross section of an MOS transistor with the velocity saturation region.

For noise modeling in strong inversion, voltage V_{ceff} in the linear or saturation region can be expressed as

$$V_{ceff} = \begin{cases} V_{ds} & \text{for } V_{ds} \le V_{dsat} \\ V_{csat} & \text{for } V_{ds} > V_{dsat} \end{cases} \tag{4}$$

where V_{dsat} is the drain saturation voltage and V_{csat} is the channel saturation voltage at $x = L_e$ [10]. This is obtained by using L_e instead of L_{eff} in the BSIM3 expression for V_{dsat}. The electrical channel length is given by $L_e = L_{eff} - \Delta L$. Also the length of velocity saturation region [11] is modeled as

$$\Delta L = \ell \ln \left(a + \sqrt{a^2 + 1} \right) \tag{5}$$

using following parameters with a model parameter t_j

$$a = \frac{V_{ds} - V_{ceff}}{\ell\, E_c} \quad \text{and} \quad \ell = t_j \sqrt{\frac{\epsilon_s x_j}{C_{ox}}} \tag{6}$$

The exact values of V_{csat} and L_e are determined by an iterative process. But a single step can be used at a few percent errors. In order to model the effect of parasitic drain and source resistance R_{ds}, the linear drain current is approximated by

$$I_d \simeq \frac{I_{d0}}{1 + R_{ds} I_{d0}/V_{ceff}} \equiv \frac{I_{d0}}{\kappa} \tag{7}$$

Here V_{ceff} has been used instead of V_{deff} in the BSIM3 model. Then the drain conductance at $V_{ds} = 0$ can be obtained as

$$g_{d0} = \frac{g_0}{1 + g_0 R_{ds}} \tag{8}$$

2. Strong Inversion Region

Since the carriers in the VS region travel at their maximum velocity, they will not respond to the fluctuations of the electric field caused by noise voltage in that region. Therefore, the contribution of the VS region to the drain noise current resulting from fluctuations of carrier velocity should be ignored [3]. As a result, a general power spectral density (PSD) of the channel thermal noise current is given by

$$S_{id} = 4kT \frac{W}{L_s^2} \int_0^{L_e} \frac{T_c}{T} \frac{\mu_{\text{eff}}^2}{\mu_{\text{dif}}} Q_i dx \tag{9}$$

where μ_{dif} is the differential mobility defined as dv_d / dE_x and L_s is given by $L_s \equiv L_e - \int_0^{V_{ceff}} (\mu'_{\text{eff}} / \mu_{\text{dif}}) dV_c$ [11].

Under high electric fields, the carrier temperature T_c increases with increasing electric field intensity. This hot carrier effect is not exactly known [12]. For simple noise modeling, the general relation between T_c and electric field has been assumed as

$$\frac{T_c}{T} = \left(\frac{\mu_0}{\mu_{\text{eff}}}\right)^{\eta} = \left(1 + \frac{E_x}{E_c}\right)^{\eta} \tag{10}$$

where η depends on the type of scattering mechanism [13]. When acoustic deformation potential scattering dominates, η has a numerical value of 2 for silicon. Typically this value has been used in compact noise modeling [14]. Here this parameter will be treated as a modeling parameter. Then the PSD expression taking into account the parasitic drain and source resistance can be approximated by

$$S_{id} \simeq 4kT \frac{\mu_0^2 W^2}{\kappa^2 L_c^2 I_d} \int_0^{V_{ceff}} \left(1 + \frac{E_x}{E_c}\right)^{\eta - 1} Q_i^2 dV_c \tag{11}$$

In the strong-inversion linear channel region, the magnitude E_x of channel electric field can be approximated by average electric field $\bar{E} \simeq V_{ceff} / L_e$. After performing the integral, the PSD of the channel thermal noise current can be obtained as

$$\frac{S_{id}}{4kT} \equiv g_{d0}\gamma = \frac{g_0}{\kappa} \frac{\rho^{\eta}}{\rho^2} \frac{L_{eff}}{L_e} \frac{(1 - u + u^2/3)}{(1 - u/2)} \tag{12}$$

where γ is the thermal noise coefficient, $\rho \equiv 1 + \bar{E} / E_c$, and $u \equiv V_{ceff} / V_b$. Since $E_x = 0$ at zero drain bias, a transistor operates as a passive conductor g_{d0} without velocity saturation effects. For any inversion level, therefore the noise coefficient γ should be equal to unity at $V_{ds} = 0$. Zero drain bias implies that $V_{ceff} = 0$, $u = 0$, $\rho = 0$, $L_c = L_e = L_{eff}$, and $g_0 / \kappa = g_{d0}$. These results verify the fact that $\gamma = 1$ at $V_{ds} = 0$.

Typical variations of the thermal noise coefficient γ and its factors for $\eta = 2$ are shown in Fig. 2. The factor f_1 is defined as $(g_0 / \kappa)(L_{eff} / L_e) / g_{d0}$ and the factor f_2 as $(1 - u + u^2/3)/(1 - u/2)$. For a long channel transistor with $L = 18\ \mu\text{m}$, it can be seen that its noise coefficient γ_∞ is equal to about 2/3 in strong inversion but is *not* equal to its known value 1/2 in weak inversion. This can be understood by considering the facts that the drain saturation voltage in weak inversion is *not* associated with the velocity saturation but associated with the exponential inversion charge density, and the phenomenon of the velocity saturation is *not* associated with diffusion current [1]. Such facts mean that the velocity saturation in weak inversion must be neglected

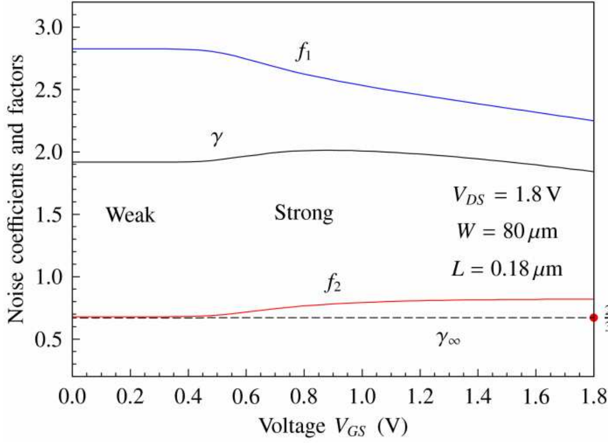

Fig. 2. Typical variations of the thermal noise coefficient γ in (12) and its factors for a 0.18 μm CMOS process. Here γ is expressed as $f_1 f_2$ and γ_∞ is the noise coefficient for a long channel MOS transistor with L of 18 μm. Note that γ_∞ is not equal to its known value 1/2 in weak inversion.

because drift current is negligible [11]. Hence $V_{ceff} = V_{ds}$, $L_e = L_{eff}$, and $E_x = d\phi_s / dx$ should be used in weak inversion to *exclude* the velocity saturation and channel length modulation. In addition, since the inversion charge density Q_i is valid in weak inversion *only* when $V_c \le 2V_T$, it can not be used in noise modeling of weak inversion with $V_{ds} > 2V_T$. As a result, (12) is *not* valid in the weak-inversion saturation region. Naturally this gives rise to incorrect noise predictions for a similar approach used in [8]. Thus there is need to model the channel thermal noise PSD taking into account the CLM exclusion and correct inversion charge density in the weak inversion region.

3. Weak Inversion Region

In the weak inversion region, the inversion charge density along the channel from source to drain can be written as

$$Q_i = Q_0 e^{(V_{gs}-V_t-nV_c)/nV_T} = C_{ox} V_{gsteff} e^{-V_c/V_T} \quad (13)$$

where nV_c instead of αV_c has been used for accuracy [9, 15]. In the BSIM3 model, Q_0 is given by

$$Q_0 = \left(\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}\right)^{1/2} V_T e^{-V_{off}/nV_T} \quad (14)$$

where ϕ_s is the surface potential in weak inversion and V_{off} is used to account for the V_t difference between weak and strong inversion regions. For short channel devices in weak inversion, the surface potential is not constant along the channel length due to drain induced barrier lowering (DIBL). So this variation will be approximated by average electric field. In the BSIM3 model, the DIBL effect itself on the drain current is modeled as a decrease in the threshold voltage.

When frequency is much smaller than collision frequency of carriers, the *two* diffusion coefficients involved in noise current and diffusion current are identical [16]. In the short channel device with high electric field, the longitudinal diffusion coefficient can be given by a generalized Einstein relation

$$D_n = \frac{kT_n}{q}\mu_{\text{dif}} = \frac{kT}{q}\mu_0\left(1+\frac{E_x}{E_c}\right)^{\eta-2} \equiv V_T\mu_w \quad (15)$$

where T_n is the noise temperature which becomes equal to the carrier temperature T_c for displaced Maxwellian velocity distribution of the channel inversion layer [11, 16, 17].

In general, the drain current is caused by both drift and diffusion. But since the current is mainly due to diffusion in weak inversion, the drain current can be approximated as

$$I_{d0} = W\left(-\mu_{\text{eff}}Q_i\frac{d\phi_s}{dx} + D_n\frac{dQ_i}{dx}\right) \simeq \mu_w W Q_i \frac{dV_c}{dx} \quad (16)$$

where μ_{eff} of the drift component has been replaced by μ_w. Since $\mu_w = \mu_0$ for $\eta = 2$, it can be seen that the velocity saturation is *absent* in weak inversion. Applying (9) to this charge sheet model with the mobility μ_w, the PSD of the channel thermal noise current can be expressed as

$$S_{id} = 4kT\frac{W}{L_w^2}\int_0^{L_{eff}} \frac{\mu_0(1+E_x/E_c)^\eta Q_i}{[1+(\eta-1)E_x/E_c]^2}\,dx \quad (17)$$

where L_{eff} has been used to exclude the channel length modulation. Then the PSD expression taking into account the parasitic drain and source resistance can be

approximated as

$$S_{id} \simeq 4kT\frac{\mu_0^2 W^2}{\kappa^2 L_w^2 I_d}\int_0^{V_{ds}}\frac{(1+E_x/E_c)^{2(\eta-1)}Q_i^2}{[1+(\eta-1)E_x/E_c]^2}\,dV_c \quad (18)$$

where E_x can be approximated as $\overline{E}$ and L_w can be obtained as $L_{eff}(1+\overline{E}/E_c)/[1+(\eta-1)\overline{E}/E_c]$. In contrast to the constant surface potential of long channel devices in weak inversion, a large variation in surface potential was predicted for short channel devices in weak inversion [18]. In order to take into account this variation, the average electric field can be modeled as $\overline{E}=d\overline{\phi}_s/dx \simeq \delta_w V_{ds}/L_{eff}$ where symbol δ_w is a modeling parameter. Using (13) and (16), the above PSD of the channel thermal noise current can be expressed as

$$\frac{S_{id}}{4kT} \equiv g_{d0}\gamma = \frac{g_0}{\kappa}\frac{\rho^\eta}{\rho^2}\frac{1}{2}\left(1+e^{-V_{ds}/V_T}\right) \quad (19)$$

For modeling flexibility in weak inversion, a different parameter η_w can be used instead of η. In the devices with $\eta=2$ or long channel devices with $\rho \simeq 1$, the noise coefficient γ is equal to about 1/2 in the saturation region. And the spectral density increases when V_{ds} is reduced from saturation to zero. When $V_{ds}=0$, the noise coefficient is equal to 1, namely the spectral density is equal to that of the channel conductance g_{d0}. This result was also true for strong inversion.

In weak inversion, the drain current can be obtained as

$$I_d = V_T\frac{g_0}{\kappa}\frac{\rho^\eta}{\rho^2}\left(1-e^{-V_{ds}/V_T}\right) \quad (20)$$

Using this in (19), the PSD of channel thermal noise current in the weak-inversion saturation region can be expressed as

$$S_{id} = 2qI_d\frac{\left(1+e^{-V_{ds}/V_T}\right)}{\left(1-e^{-V_{ds}/V_T}\right)} \simeq 2qI_d \quad (21)$$

This is the shot noise expression. The physical origin of white noise in weak inversion has been assumed to be either thermal or shot noise. But both assumptions lead to the same result for all bias points since both noises are related each other [1]. According to recent theoretical and experimental results, the short channel noise at low drain currents is dominated by shot noise due to the diffusion current near the source [19].

4. Moderate Inversion Region

In moderate inversion, both drift and diffusion significantly contribute to the value of the drain current. Moreover, channel length modulation as well as current component is smoothly changed between weak and strong inversion regions. So the effect of velocity saturation should be gradually removed as operation transits from strong inversion to weak inversion [1]. As a result, it is difficult to obtain a simple expression for PSD of the channel thermal noise current in this region. Like in the EKV model [20], this problem can be solved by interpolating thermal noise PSD from weak to strong inversion. Hence a unified channel thermal noise PSD can be described as

$$S_{id} = c_i S_{id}^s + (1-c_i)S_{id}^w \quad (22)$$

where S_{id}^w and S_{id}^s are PSDs for weak and strong inversion respectively, c_i is a sigmoid function given as follows [21].

$$c_i = \frac{1}{2}\left[1+\frac{V_{gs}-V_t+V_m}{\sqrt{\left(V_{gs}-V_t+V_m\right)^2+\delta_m}}\right] \quad (23)$$

This function has the value of one in the strong inversion region and smoothly transits to zero in the weak inversion region as shown in Fig. 3. In order to model the position and slope of the transition, model parameters $V_m = 0.04$ V and $\delta_m = 0.017\,\mathrm{V}^2$ will be used for noise simulation.

Similarly, by applying the sigmoid function into (5), the length of velocity saturation region is modified as

$$\Delta L = \ell \ln\left(c_i a + \sqrt{(c_i a)^2+1}\right) \quad (24)$$

Then channel length modulation is reduced to zero in the weak inversion region where diffusion current is totally

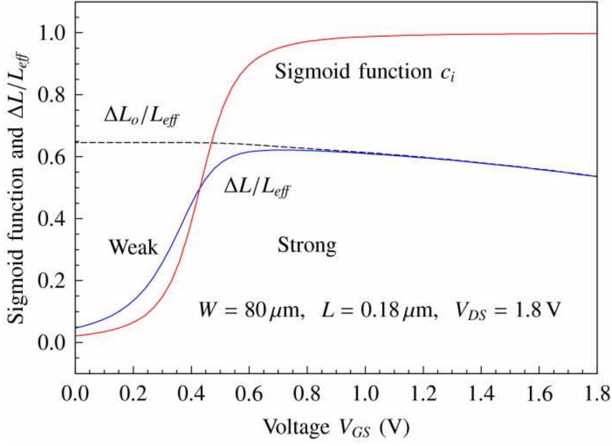

Fig. 3. Sigmoid function and $\Delta L / L_{eff}$ as a function of gate-source voltage.

dominant. The ratio $\Delta L / L_{eff}$ versus gate-source voltage is also shown in Fig. 3. In weak inversion without CLM, we can confirm that the original length ΔL_o of the VS region does not decrease but the modified length ΔL decreases appropriately.

5. NQS Effect and Extrinsic Noise

The intrinsic channel thermal noise due to resistive channel is *white noise* with a flat PSD up to 10^{12} Hz [1, 4, 22]. From microscopic noise analysis for carrier scattering, the PSD of the thermal current noise due to carrier velocity fluctuations in a conductor G is given by $S_{id} = 4kTG/(1+\omega^2\tau_c^2)$ where τ_c is the mean free time between collisions [23]. Thus the intrinsic channel thermal noise can be approximated as

$$S_{id}^{\tau_c} \simeq \frac{S_{id}}{1+\omega^2\tau_c^2} \tag{25}$$

The mean free time is typically 0.1 ps at room temperature. Then the white noise approximation will be valid up to about 1 THz. But NQS effect and extrinsic noises show frequency dependence in the PSD below 1 THz.

An approach to account for the NQS effect is to use the multisegment model in which a transistor is divided into several channel segments. Each segment as a subtransistor is scaled appropriately and represented by an intrinsic QS model. Then noise PSDs can be obtained by circuit simulation [6]. Using a long channel NQS small signal equivalent circuit, an NQS noise model can be written as numerical integrations. This is because the transistor at nonzero drain bias is modeled as an active nonuniform transmission line. As a result, no analytical NQS expressions are given for such integrals. From numerical integration and multisegment simulation, it has been shown that the drain current noise PSD tends to slowly increase with frequency approximately as $\sqrt{\omega}$ [24]. Since a transistor at zero drain bias can be regarded as an active uniform transmission line, its drain current noise PSD can be expressed as an analytical form [25]. At this point, the crude noise behavior at very high frequencies will be explored by generalizing such NQS effect for nonzero drain bias. Hence the NQS drain current noise PSD can be approximated as

$$S_{id}^{nqs} \simeq S_{id}^{\tau_c}\sqrt{\frac{\omega}{8\omega_o}\frac{\sinh\left(\sqrt{2\omega/\omega_o}\right)+\sin\left(\sqrt{2\omega/\omega_o}\right)}{\left|\sinh\left(\sqrt{\omega/2\omega_o}+j\sqrt{\omega/2\omega_o}\right)\right|^2}} \tag{26}$$

where the cutoff frequency ω_o is given by $(g_{d0}/C_{ox}WL_{eff})$ and corresponds to a frequency limit between QS and NQS operation. For $\omega \ll \omega_o$, S_{id}^{nqs} will be equal to $S_{id}^{\tau_c} \simeq S_{id}$.

One extrinsic noise is associated with the substrate resistance noise [26]. The thermal noise of effective resistance between the channel and substrate gives rise to fluctuations in the intrinsic substrate voltage. These produce an additional drain noise current via body transconductance g_{mb} [27]. As a result, the PSD of this noise current can be written as

$$S_{id}^{R_b} \simeq \frac{4kTR_b g_{mb}^2}{1+\omega^2 R_b^2 C_b^2} \tag{27}$$

where R_b is the body or substrate resistance and C_b is the body depletion capacitance due to the depletion regions under the channel, source, and drain. This capacitance can be modeled as $(C_{bs}+C_{bd}+C_{gb})$. For high frequency accuracy, this thermal noise can be expressed as the sum of multiple components with different poles due to the three-dimensional distributed effect of the substrate. But the above model with a single

resistance can be simply used at frequencies below 10 GHz [28].

Another extrinsic noise is associated with the gate resistance noise [6]. At low frequencies, this noise can be modeled as an effective gate resistance [29]. The thermal noise voltage across the gate resistance R_g produces a drain noise current via transconductance g_m. At very high frequencies, it is known that this effect tends to be filtered out by the distributed gate resistance and capacitance [30]. This is true only when the effective gate resistance R_n is not much smaller than $1/g_m$. But this resistance in modern short channel devices has been greatly reduced by using the folded and silicided gate with contacts on both sides. For this gate structure, the PSD of the drain noise current due to its resistance can be modeled as

$$S_{id}^{R_g} \simeq \frac{4kTR_n g_m^2 (1+\omega^2 C_{gd}^2/g_m^2)}{(1+1.5\omega^2 C_g^2 R_n^2)(1+\omega^2 C_m^2/g_m^2)} \quad (28)$$

where R_n is given by $(R_g/12n^2)$ using folding factor n, $C_g = (C_{gs}+C_{gd}+C_{gb})$, $C_m = (C_{dg}-C_{gd})$, and the transadmittance $g_m^* = g_m/(1+j\omega C_m/g_m)$ instead of g_m has been used to account for the channel NQS effect. From this equation, it can be seen that the effect of the gate noise on the drain might not diminish but increase in a very high frequency band.

Using the drain current noises discussed in this section, a total channel thermal noise PSD can be described as

$$S_{id}^{tot} = S_{id}^{R_b} + S_{id}^{R_g} + S_{id}^{nqs} \quad (29)$$

Fig. 4 shows the calculated and measured drain current noise PSDs for a short channel transistor with width of 192 µm and length of 0.18 µm [6]. Here R_n is obtained as $0.2\,\Omega$. Although the frequency limit of validity is exceeded, the frequency is driven to values higher than the cutoff frequency $f_o = 90$ GHz of the transistor to show approximate noise behavior there. The NQS noise in the figure means $(S_{id}^{nqs} - S_{id}^{T_c})$. It can be seen that a frequency dependence of drain current noise PSD in the GHz frequency range is modeled by the body resistance noise.

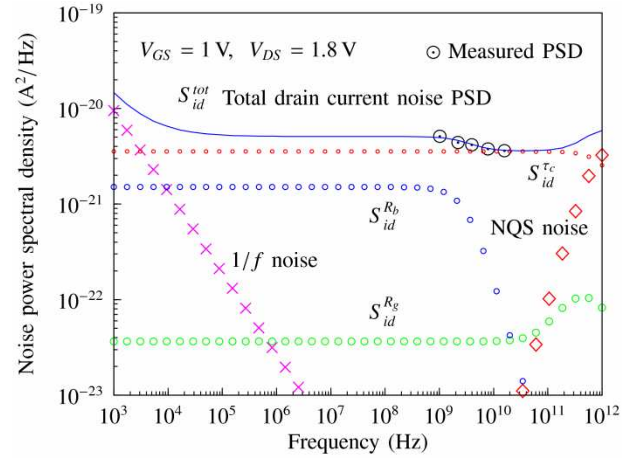

Fig. 4. Power spectral density of drain current noises for an MOS transistor with $W = 64 \times 3$ µm and $L = 0.18$ µm. Circled dots are the measured values of PSD [6]. The body resistance R_b of $250\,\Omega$ is used for modeling.

6. Channel Length Limit of Validity

At low electric fields, the carrier scattering is strong enough to ensure that carriers and lattice are in thermal equilibrium with $T_c = T$. For nonuniform high electric fields at which the voltage drop over the mean free path is larger than kT/q, carriers are heated due to low scattering rate, so $T_c > T$. Then the carriers and lattice are in nonequilibrium with temperature gradient. In ultrashort devices, steep junctions result in huge built-in electric fields. When the electric field varies rapidly in the devices, carriers display their wave nature. As a result, the drift diffusion (DD) approximation appears to be problematic for such devices [31]. Moreover the carrier mobility relates statistically the average carrier velocity to the electric field. Such averaging make sense if the channel length is much larger than the mean free path. To treat carriers as classical Newton particles, the mean free path ℓ_c must be much longer than the mean electron wavelength λ_c [13]. From this discussion, it follows justly that $L > \ell_c > \lambda_c \simeq 10$ nm in silicon at room temperature. If the channel length is smaller than the mean free path, carriers go through the channel ballistically without significant scattering. Then the DD model used so far in noise analysis loses its validity for such nanoscale transistors. Recently the existence of new excess noise above the Nyquist thermal noise level was observed for sub-100 nm transistors but its insignificant

effect in transistors with $L \geq 100$ nm was confirmed [32]. Thus it is desirable that a channel length limit of the proposed model is suggested as $L \geq 100$ nm.

III. NOISE MODELING RESULTS

For model testing, the above model has been implemented in the Spice BSIM3v3 source code. Since no model parameters for published noise data are available, the BSIM3v3 model parameters for a 0.18 μm process (MOSIS T77A: MM NONEPI [33]) will be used in all noise simulations. Before the thermal noise model is verified against experimental noise data, a simple benchmark test is performed [1, 34]. In an MOSFET biased at $V_{DS} = 0$, its channel is equivalent to a conductor g_{d0}. As a result, the channel should show thermal noise consistent with its conductance [1]. This means that the γ value for zero drain bias must be equal to 1 in any inversion level as well as in both weak and strong inversion. For a long channel transistor operating in the saturation region, its γ is equal to 2/3 in strong inversion and 1/2 in weak inversion. Thus in strong inversion, this γ should decrease from 1 at $V_{DS} = 0$ to 2/3 in saturation. On the other hand, this γ in weak inversion should decrease to 1/2 in saturation.

Fig. 5 shows the results of the benchmark noise test for a long channel *n*MOS device with $t_j = 0.856$ and $\eta = \eta_w = 2$. As expected, the results in both weak and strong inversion pass the noise test. This confirms that the proposed noise model is applicable in all operation regions. In this figure, dashed lines show the results of the original BSIM3v3 noise model. Its charge-based thermal noise model is given by

$$\frac{S_{id}}{4kT} \equiv g_{d0}\gamma = \frac{\mu_{\text{eff}}|Q_{\text{inv}}|}{L_{\text{eff}}^2 + \mu_{\text{eff}}|Q_{\text{inv}}|R_{ds}} \qquad (30)$$

where Q_{inv} is the inversion channel charge [35, 36]. As can be seen, only the result in strong inversion passes the noise test. In weak inversion, γ is not equal to 1 at $V_{DS} = 0$ and does not decrease to its value 1/2 over a V_{DS} range of about $5V_T$. Small circles show the results of another BSIM3 noise model [8]. As discussed in Section II.2, it is clear that γ in weak inversion does not decrease to 1/2 in saturation where $V_{DS} > 5V_T$.

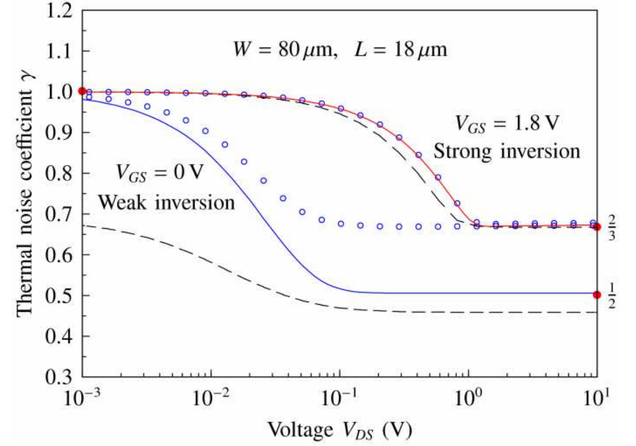

Fig. 5. Benchmark noise test for a long channel *n*MOS transistor with L of 18 μm. For $V_{DS} = 0$, it was confirmed from simulation data that γ is 1 in both weak and strong inversion. In the saturation region, it can be seen that γ is about 1/2 in weak inversion and γ is about 2/3 in strong inversion. Dashed lines are obtained from the original charge-based thermal noise model of BSIM3v3. Small circles are obtained from another BSIM3 noise model [8].

Now the predictions of the noise model will be compared with the published predictions and experimental data. Fig. 6 shows thermal noise coefficient γ as a function of gate-source voltage. The used parameters are $t_j = 0.856$, $\eta = 1.442$, $\eta_w = 2.35$, and $\delta_w = 0.1$. In the saturation region from weak to strong inversion, the γ values of the noise model are compared with those of the published approach [7]. It can be seen that there is good agreement between the predictions of the two models. For $V_{DS} = 0$, it is confirmed that γ has a value of 1 for all values of V_{GS}. But the original BSIM3v3 model does not accurately predict $\gamma = 1$ for $V_{DS} = 0$ in weak and moderate inversion as well as the excess noise in moderate and strong inversion.

Fig. 7 shows thermal noise coefficient γ as a function of drain-source voltage. The used parameters are $t_j = 0.856$, $\eta = 1.21$, $\eta_w = 2$, LINT = 0.015 μm, and RDSW = 186. From linear to saturation region in strong inversion, the results of the noise model are compared with the published noise data [4]. A good agreement between simulation and measurement is observed from linear to saturation region. Fig. 8 shows the PSD of channel thermal noise current as a function of gate-source voltage. The used parameters are $t_j = 0.856$, $\eta = \eta_w = 2$, LINT = 0.39 nm, and RDSW

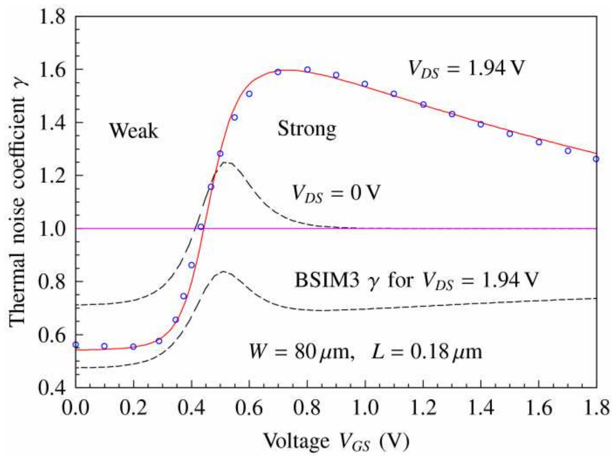

Fig. 6. Thermal noise coefficient γ as a function of gate-source voltage for a short channel MOSFET with L of 0.18 µm. Small circles were predicted by another model [7]. For $V_{DS} = 0$, it can be seen that γ is 1 in all inversion levels. Dashed lines are obtained from the original BSIM3v3 noise model.

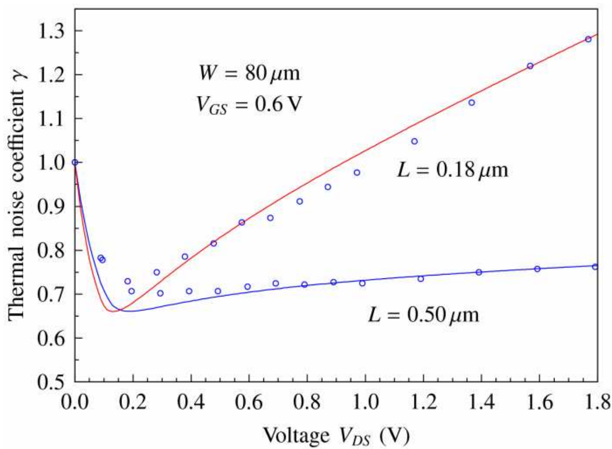

Fig. 7. Thermal noise coefficient γ as a function of drain-source voltage for two channel lengths of a short channel MOSFET with W of 80 µm. Circles are measured thermal noise coefficients [4]. These are fitted to 1 at $V_{DS} = 0$.

= 235. Except these parameters, all other BSIM3 parameters have the same values as those used in noise simulations for Fig. 7. For the saturation region in strong inversion, the PSDs of the noise model are compared with the published noise data [5]. In this figure, there is a good agreement between simulation and measurement for high gate-source voltages. For low gate-source voltages, it is observed that simulated PSDs have somewhat low values. To analyze this result, noise data consistent with known BSIM3 parameters should be available. Finally, it is pointed out that no noise model

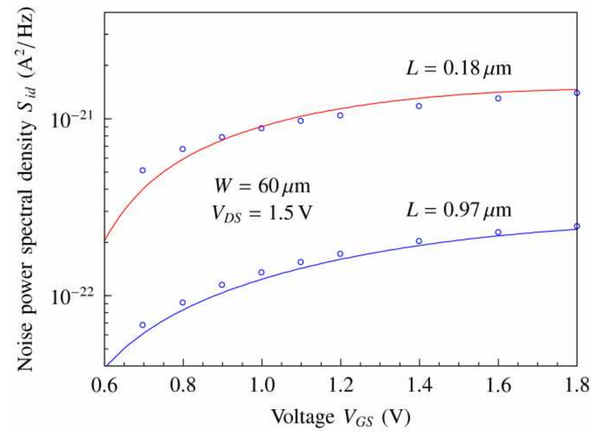

Fig. 8. PSD of channel thermal noise current as a function of gate-source voltage for two channel lengths of a short channel MOSFET with W of 60 µm. Circles are measured values of power spectral density [5].

for weak or moderate inversion was included in [4] and [5] unlike unified noise models for all regions.

IV. CONCLUSIONS

A unified channel thermal noise model valid in all regions of operation has been presented for the BSIM3 model. For a long channel transistor, the modeling results in both weak and strong inversion passed the benchmark noise test. From comparing with published noise data, a good agreement between simulation and measurement was observed for short channel transistors. Hence, this noise model could be usefully used in simulating the MOSFET channel noise in all operation regions.

ACKNOWLEDGMENTS

This research was supported by Kyungpook National University Research Fund, 2012.

REFERENCES

[1] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*. Oxford University Press, 2011.

[2] S. D. Yu, "Design of CMOS op amps using adaptive modeling of transistor parameters," *Journal of Semiconductor Technology and Science*, vol. 12, pp. 75-87, Mar. 2012.

[3] C. H. Chen and M. J. Deen, “Channel noise modeling of deep submicron MOSFETs,” *IEEE Trans. Electron Devices*, vol. 49, pp. 1484-1487, Aug. 2002.

[4] K. Han, H. Shin, and K. Lee, “Analytical drain thermal noise current model valid for deep submicron MOSFETs,” *IEEE Trans. Electron Devices*, vol. 51, pp. 261-269, Feb. 2004.

[5] S. Asgaran, M. J. Deen, and C. H. Chen, “Analytical modeling of MOSFETs channel noise and noise parameters,” *IEEE Trans. Electron Devices*, vol. 51, pp. 2109-2114, Dec. 2004.

[6] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, “Noise modeling for RF CMOS circuit simulation,” *IEEE Trans. Electron Devices*, vol. 50, pp. 618-632, Mar. 2003.

[7] A. S. Roy and C. C. Enz “An analytical thermal noise model of the MOS transistor valid in all modes of operation,” *Proc. of the Int. Conf. on Noise and Fluctuations*, vol. 780, pp. 741-744, Sep. 2005.

[8] Z. Li, J. Ma, Y. Ye, and M. Yu, “Compact channel noise models for deep-submicron MOSFETs,” *IEEE Trans. Electron Devices*, vol. 56, pp. 1300-1308, June 2009.

[9] Y. Cheng, M. C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P. K. Ko, and C. Hu, “A physical and scalable I-V model in BSIM3v3 for analog/digital circuit simulation,” *IEEE Trans. Electron Devices*, vol. 44, pp. 277-287, Feb. 1997.

[10] D. P. Triantis, A. N. Birbas, and D. Kondis, “Thermal noise modeling for short-channel MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 43, pp. 1950-1954, Nov. 1996.

[11] C. C. Enz and E. A. Vittoz, *Charge-based MOS Transistor Modeling*. John Wiley & Sons, 2006.

[12] A. van der Ziel, *Noise in Solid State Devices and Circuits*. John Wiley & Sons, 1986.

[13] M. Lundstrom, *Fundamentals of Carrier Transport*. Addison-Wesley, 1990.

[14] A. S. Roy and C. C. Enz, “Compact modeling of thermal noise in the MOS transistor,” *IEEE Trans. Electron. Devices*, vol. 52, pp. 611-614, Apr. 2005.

[15] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. Springer-Verlag, 1993.

[16] J. P. Nougier, “Fluctuations and noise of hot carriers in semiconductor materials and devices,” *IEEE Trans. Electron. Devices*, vol. 41, pp. 2034-2049, Nov. 1994.

[17] M. A. Omar and L. Reggiani, “Drift and diffusion of charge carriers in silicon and their empirical relation to the electric field,” *Solid-State Electronics*, vol. 30, pp. 693-697, Jul. 1987.

[18] Z. H. Liu, C. Hu, J. H. Huang, T. Y. Chan, M. C. Jeng, and P. K. Ko, “Threshold voltage model for deep-submicrometer MOSFET’s,” *IEEE Trans. Electron. Devices*, vol. 40, pp. 86-95, Jan. 1993.

[19] S. Andersson and C. Svensson, “Direct experimental verification of shot noise in short channel MOS transistors,” *Electronics Letters*, vol. 41, pp. 869-871, Jul. 2005.

[20] C. C. Enz, F. Krummenacher, and E. A. Vittoz, “An analytical MOS transistor model valid in all regions of operation and dedicated to lowvoltage and low-current applications,” *Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83-114, July 1995.

[21] S. H. Jen, B. J. Sheu, and Y. Oshima, “A unified approach to submicron DC MOS transistor modeling for low-voltage ICs,” *Analog Integrated Circuits and Signal Processing*, vol. 12, pp. 107-118, Feb. 1997.

[22] J. Jeon, B.-G. Park, J. D. Lee, and H. Shin, “Analytical noise parameter model of short-channel RF MOSFETs,” *Journal of Semiconductor Technology and Science*, vol. 7, pp. 88-93, June 2007.

[23] F. Bonani and G. Ghione, *Noise in Semiconductor Devices*. Springer-Verlag, 2001.

[24] A.-S. Porret and C. C. Enz, “Non-quasi-static (NQS) thermal noise modelling of the MOS transistor,” *IEE Proc. Circuits Devices Syst.*, vol. 151, pp. 155-166, Apr. 2004.

[25] J.-S. Goo, C.-H. Choi, F. Danneville, E. Morifuji, H. S. Momose, Z. Yu, H. Iwai, T. H. Lee, and R. W. Dutton, “An accurate and efficient high frequency noise simulation technique for deep submicron MOSFETs,” *IEEE Trans. Electron. Devices*, vol. 47, pp. 2410-2419, Dec. 2000.

[26] R. P. Jindal, “Distributed substrate resistance noise in fine-line NMOS field-effect transistors,” *IEEE Trans. Electron. Devices*, vol. 32, pp. 2450-2453, Nov. 1985.

[27] J.-S. Goo, S. Donati, C.-H. Choi, Z. Yu, T. H. Lee, and R. W. Dutton, "Impact of substrate resistance on drain current noise in MOSFETs," in *Proc. Int. Conf. SISPAD*, pp. 182-185, Sep. 2001.

[28] C. Enz, "An MOS transistor model for RF IC design valid in all regions of operation," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 342-359, Jan. 2002.

[29] B. Razavi, R.-H. Yan, and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits and Systems I*, vol. 41, pp. 750-754, Nov. 1994.

[30] E. Abou-Allam and T. Manku, "A small-signal MOSFET model for radio frequency IC applications," *IEEE Trans. Computer-Aided Design of Integr. Circuits and Syst.*, vol. 16, pp. 437-447, May 1997.

[31] C. Jungemann, T. Grasser, B. Neinhüus, and B. Meinerzhagen, "Failure of moments-based transport models in nanoscale devices near equilibrium," *IEEE Trans. Electron. Devices*, vol. 52, pp. 2404-2408, Nov. 2005.

[32] G. D. J. Smit, A. J. Scholten, R. M. T. Pijper, R. van Langevelde, L. F. Tiemeijer, and D. B. M. Klaassen, "Experimental demonstration and modeling of excess RF noise in sub-100-nm CMOS technologies," *IEEE Electron Device Lett.*, vol. 31, pp. 884-886, Aug. 2010.

[33] The Mosis Service, http://www.mosis.com/requests/test-data, Dec. 2012.

[34] A. J. Scholten, R. van Langevelde, L. F. Tiemeijer, and D. B. M. Klaassen, "Compact modeling of noise in CMOS," *Proc. of the IEEE Custom Integrated Circuits Conference*, pp. 711-716, Sep. 2006.

[35] W. Liu, et al., *BSIM3v3.3 MOSFET Model User's Manual*. University of California, Berkeley, 2005.

[36] Y. Cheng and C. Hu, *MOSFET Modeling & BSIM3 User's Guide*. Kluwer Academic Publishers, 1999.

Sang Dae Yu was born in Ulsan, South Korea on February 12, 1958. He received the B.S. degree in electronics engineering from Kyungpook National University, Daegu, Korea in 1980, and the M.S. degree and the Ph.D. degree in electrical engineering from Korea Advanced Institute of Science and Technology in 1982 and 1998, respectively. Since 1982, he has been with the School of Electronics Engineering, Kyungpook National University, Korea, where he is currently a Professor. His current interests include integrated circuit design, design automation, semiconductor device modeling, SAW filters, and embedded systems. Prof. Yu is a member of the Institute of Electronics Engineers of Korea and the Korean Sensors Society.