Low Phase Noise LC-VCO with Active Source Degeneration

D. B. Yen Nguyen*, Young-Hun Ko*, Seok-Ju Yun, Seok-Kyun Han*, and Sang-Gug Lee***

Abstract—**A new CMOS voltage-bias differential LC voltage-controlled oscillator (LC-VCO) with active source degeneration is proposed. The proposed degeneration technique preserves the quality factor of the LC-tank which leads to improvement in phase noise of VCO oscillators. The proposed VCO shows the high figure of merit (FOM) with large tuning range, low power, and small chip size compared to those of conventional voltage-bias differential LC-VCO. The proposed VCO implemented in 0.18-μm CMOS shows the phase noise of -118 dBc/Hz at 1 MHz offset oscillating at 5.03 GHz, tuning range of 12%, occupies 0.15 mm^2 of chip area while dissipating 1.44 mW from 0.8 V supply.**

Index Terms—**LC voltage-controlled oscillator, phase noise, voltage-bias differential LC-VCO, RF transceivers, source degeneration**

I. INTRODUCTION

In the VCO design for the RF transceivers, the low phase noise is the most important performance parameter. The conventional differential LC-VCO compensates the energy loss of LC-tank by the negative resistance which is generated from a differential switching pair. The current source plays two main roles in the conventional differential LC-VCO: setting the bias current and providing high impedance in series with the on-resistor of the switch transistors. However, the bias current contains the low frequency noise components coming from the current mirror circuit. The low frequency noise components which consist of not only the thermal noise but also the flicker noise are translated up in frequency and degrade the phase noise performance. In the conventional LC-VCO, the noise of the differential switch pair appears at the output during the short time when both switch transistors operate in saturation. Thus, the current source dominates the overall noise contribution of the active device in the conventional differential LC-VCO [1]. Several techniques have been reported that suppress the noise contribution of the current source in the differential LC-VCO [2, 3]. One common technique is placing an LC filter in shunt with the current source to short the noise signal to the ground. Another technique is substituting the current source with a poly-silicon resistor in series with an inductor. In both techniques, an additional inductor is required to increase the tail impedance at the oscillation frequency and its harmonics in order to preserve the quality factor of LC tank. However, the additional inductor increases the chip size and causes unpredicted effects of two inductors working at different resonant frequencies. The phase noise performance of the conventional differential LC-VCO can be improved obviously if the current source can be removed.

This paper concerns the LC-VCO architectures which eliminates the current source completely. In this paper, the differential LC-VCO without the current source (i.e. the voltage-bias differential LC-VCO) is studied where the quality factor degradation of the LC-tank is an issue. The bias condition of the voltage-bias differential LC-

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VCO can be controlled by the supply voltage. To reduce the power consumption, the voltage-bias differential LC-VCO can be fed with a low supply voltage. The low supply voltage architecture is not considerable for VCO design but it can be useful for current reused applications which pile up VCO block over other blocks [4]. In this work, a new voltage-bias differential LC-VCO architecture with active source degeneration is proposed in which the quality factor of the LC-tank is preserved. The proposed voltage-bias LC-VCO is suitable for low phase noise, low power and small size LC-VCO implementation.

II. PROPOSED VOLTAGE-BIAS DIFFERENTIAL LC-VCO

Fig. 1 illustrates the conventional voltage-bias differential LC-VCO (Fig. 1(a)); the proposed voltage-bias differential LC-VCO (Fig. 1(b)) and its improved architecture (Fig. 1(c)).

The conventional voltage-bias LC-VCO in Fig. 1(a) preserves oscillation by negative resistance generated by the NMOS differential switch pair (30u/180n) in shunt with LC-tank (2.5 nH/500 fF). In Fig. 1(a), the drain-source voltages of the M_1, M_2 are identified as V_o^+, V_o^- as the source of M_1, M_2 are shorted to ground. The gate-drain voltages of M_1, M_2 are $V_o^- - V_o^+$ and $V_o^+ - V_o^-$, respectively. Due to the symmetry of the differential topology, the gate-drain voltages are equal in magnitude but opposite in signs. When V_o^+ and V_o^- are small, the differential output voltage $|V_o^+ - V_o^-|$ is close to zero, such that both M_1 and M_2 operate in saturation region and isolates LC-tank from ground. With increase in output voltage swing, for example, during the first half oscillation cycle, when $V_o^+ - V_o^-$ increases above the threshold voltage of NMOS transistor (V_t), the gate-drain of M_2 exceeds $+V_t$, forcing M_2 into triode mode operation. While the gate-drain of M_1 falls below $-V_t$, driving M_1 deeper into saturation mode operation. The resistance between the drain and source of M_2 in triode mode operation reduces rapidly with increase in differential voltage, thus, the quality factor of the LC-tank is degraded heavily. Likewise, during the next half cycle, the quality factor is degraded by M_1. Over the full oscillation cycle, both of the switch transistors degrade the average quality factor of LC-tank. Due to this quality factor degradation, the conventional voltage-bias LC-VCO cannot improve the phase noise performance though it removed the current source which is known as the main noise contributor of the differential LC-VCO. Fig. 2(a) depicts above explanations by figures in time domain. In Fig. 2(a), in each half oscillation cycle, the LC-tank is loaded with high resistance only when the output voltages are small. However, for the most part of an oscillation cycle, the loaded impedance of LC-tank is low which leads to poor average quality factor of LC-tank.

In Fig. 1(b), the proposed voltage-bias LC-VCO has additional MOS transistors M_3 and M_4 to the source of the two switch transistors M_1 and M_2, respectively. The gates of M_3 and M_4 are cross-connected with the gates of M_1 and M_2, respectively. M_3, M_4 are sized corresponded

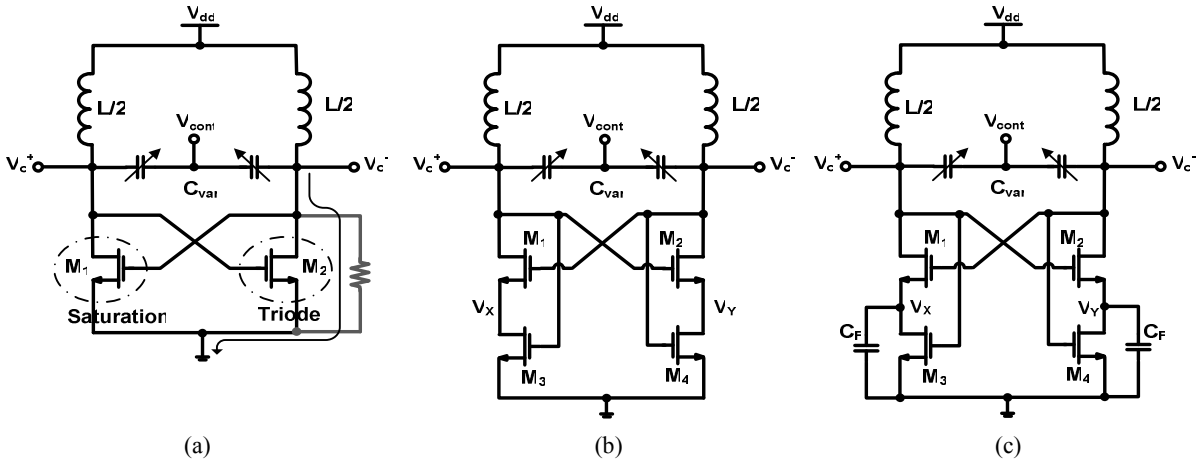


Fig. 1. Voltage-bias differential LC-VCOs: Conventional (a), proposed (b) and proposed including capacitor filter (c).

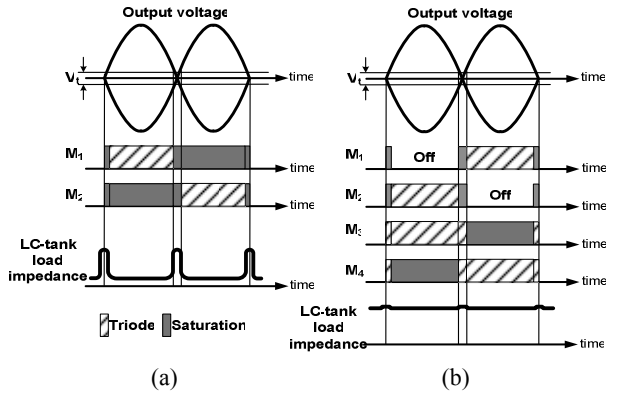


Fig. 2. Circuit operation in time domain: Conventional (a) and proposed voltage-bias differential LC-VCO (b).

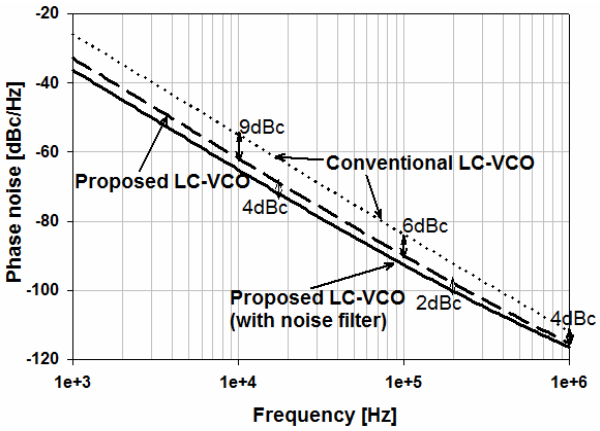


Fig. 3. Simulated phase noise performance of the three voltage-bias differential LC-VCOs.

to M_1, M_2 in order to maintain the same oscillation. In Fig. 1(b), for zero differential voltage (V_o^+-V_o^- is small), the drain voltages (V_x, V_y) of M_3, M_4 are small which leads them into triode mode operation. M_1 and M_2 that operate in saturation mode not only isolate the LC-tank from ground but also operate as the common source stages with source degeneration by M_3 and M_4, respectively. The common source architecture with source degeneration improves the phase noise of the LC-VCO by suppressing the 1/f noise of the switch transistors [5].

During the steady-state operation with V_o^+-V_o^->V_t, in the first half of oscillation cycle, the output voltage swing drives M_2 and M_1 into triode and saturation mode operation, respectively. The condition of M_2 in triode region can be expressed as

$$V_{DS} < V_{GS} - V_t \quad (1)$$

$$V_o^- - V_Y < V_o^+ - V_Y - V_t \quad (2)$$

$$V_o^- - V_Y < V_o^+ - V_o^- \quad (3)$$

$$V_o^- - V_Y < V_t \quad (4)$$

The left side of (4) represents the gate-drain voltage of M_4. From (4), the gate-drain voltage of M_4 falls below V_t driving M_4 into saturation mode operation. With increase in differential voltage, M_1 and M_4 are forced into saturation mode operation such that the LC-tank is isolated from ground, thus, the quality factor of LC-tank is not degraded. In the next half cycle, M_2 and M_3 are forced into saturation mode operation isolating LC-tank from ground. Therefore, the average quality factor of LC-tank is preserved over the full oscillation cycle. Fig. 2(b) shows the operation of the proposed voltage-bias LC-VCO shown in Fig. 1(b) in time domain. As can be seen in Fig. 1(b), over the entire oscillation cycle, the loaded impedance of LC-tank is high due to the degenerating transistors M_3 and M_4 which operate in saturation mode. The high loaded impedance of the LC-tank preserves the average quality factor of the LC-tank. Therefore, the phase noise of the proposed voltage-bias LC-VCO can be improved much more compared to that of the conventional one. However, in Fig. 1(b) although the voltage-bias differential LC-VCO do not have the noise contribution from the current sources, the noise frequencies around $2\omega_0$ (ω_0 is the oscillation frequency) which originates in the switch pair and degeneration transistors still disturb the LC-VCO phase noise performance. In Fig. 1(c), the large capacitors, C_F, are added in parallel with transistors M_3 and M_4 to short the noise signals near $2\omega_0$ to ground.

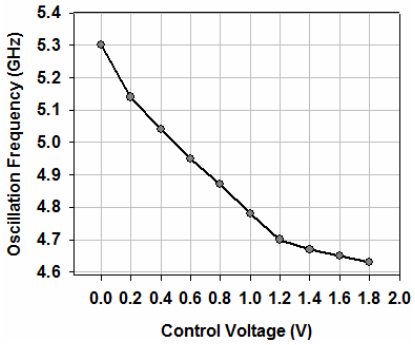
Fig. 3 shows the simulated phase noise performance of the proposed voltage-bias LC-VCO compare to the conventional voltage-bias LC-VCO. As can be seen in Fig. 3, the phase noise of the proposed voltage-bias LC-VCO improves significantly compare to that of the conventional voltage-bias LC-VCO. The additional of filter capacitor, CF, leads to additional 2-4 dBc/Hz improvement in phase noise.

III. MEASUREMENT RESULTS

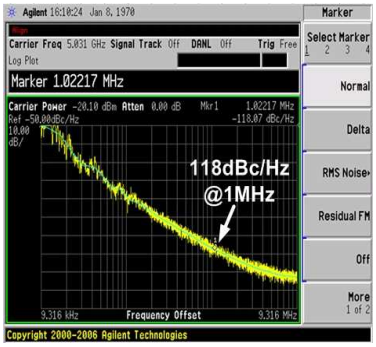
The proposed voltage-bias differential LC-VCO (Fig. 1(c)) is fabricated in 0.18 μm CMOS technology. The proposed oscillator has a inverter amplifier as a buffer at

each output. The measured oscillation frequency shows 12% tuning range 4.64-5.3 GHz with the control voltage of 0-1.8 V which shown in Fig. 4(a). The measured phase noise, as shown in Fig. 4(b), is -118 dBc/Hz at 1MHz offset from 5.03 GHz oscillation frequency. Fig. 5 shows a microphotograph of fabricated chip which occupies an area of 0.15 mm^2 (0.35x0.45 mm^2). The proposed voltage-bias LC-VCO dissipates 1.8 mA at 0.8 V supply.

Table 1 summaries the overall performance of the proposed voltage-bias LC-VCO in comparison with



(a)



(b)

Fig. 4. Measured performance of the proposed voltage-bias differential LC-VCO (a) Oscillation frequency vs. control voltage, (b) phase noise at 5.03 GHz oscillation frequency.

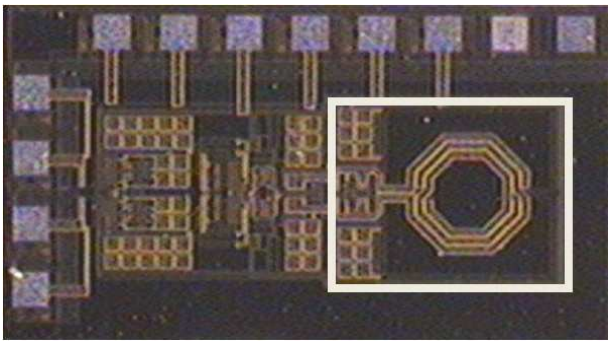


Fig. 5. Chip photograph of proposed voltage-bias differential LC-VCO (white line frame).

Table 1. Perform summary of the proposed voltage-bias LC-VCO in comparison with previous works

	This work	[6]	[7]	[8]	[9]
I_{DC}(core) [mA]/ VDD [V]	**1.8 /0.8**	7.5 /1.8	2 /1.5	3.5 /1.8	5.6 /1.8
Output Freq. [GHz] Tuning range (%)	**4.64~ 5.3 /12**	5.1~5.5 /8	4.6~5 /8.3	4.39~5.3 /18	5.3~6.4 /18
Phase noise at 1 MHz [dBc/Hz]	**-118**	-124	-120	-113.7	-117
Core size (mm^2)	**0.15**	NA	0.41	0.35	0.16
FOM1 (Power, osc. freq. effects)	**190.4**	187.2	189.6	162	156
FOM2 (Tuning range effect)	**171.2**	167	167.3	180	184
Technology	**0.18 µm CMOS**	0.18 µm BiCMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS

previously reported differential LC-VCOs. In Table 1, the power-frequency-normalized Figure of Merit (FOM1) [10] and the power-frequency-tuning-normalized Figure of Merit (FOM2) [11] are added for fair comparison. As can be seen in Table 1, the proposed voltage-bias LC-VCO shows the best FOM1 and FOM2 of the 5 GHz differential LC-VCOs.

IV. CONCLUSIONS

In this letter, the issue with conventional voltage-bias differential LC-VCO is analyzed and a CMOS voltage-bias differential LC-VCO with active source degeneration is proposed. The proposed voltage-bias LC-VCO preserves the quality factor of the resonator by providing high impedance transistors to the LC-tank. The proposed voltage-bias LC-VCO is implemented in 0.18-µm CMOS technology. The measurement results show the phase noise performance of -118 dBc/Hz at 1 MHz offset from the 5.03 GHz oscillation frequency. While dissipating 1.8 mA from 0.8V supply, the measured tuning range is about 12% from 4.64 to 5.3 GHz and the chip occupies 0.15 mm^2.

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REFERENCES

[1] Rael, J. J., and Abidi, A. A., "Physical process of phase noise in differential LC oscillator's ", Proc. IEEE CICC, Orlando, FL, USA, 2000, pp. 569-572.

[2] Emad Hegazi et al., "A Filtering Technique to Lower LC oscillator Phase Noise", IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 1921-1930, Dec, 2001.

[3] Ismail, A., Abidi, A. A, "CMOS differential LC oscillator with suppressed up-converted flicker noise". ISSCC Tech, Dif., San Francisco, CA, USA, 2003, pp. 98-99.

[4] Kyung-Gyu Park et al., "Current reusing VCO and divide-by-two frequency divider for quadrature LO generation", IEEE Microw. Wireless Compon. Lett., vol. 18, no. 06, pp. 413-415, June, 2008.

[5] S. J. Yun and S. G. Lee, "RF CMOS LC-Oscillator with source damping resistors", IEEE Microw. Wireless Compon. Lett., vol. 16, no. 09, pp. 511-513, Sep, 2006.

[6] A. Jerng and C. G. Sodini, "The impact of device type and sizing in phase noise mechanisms", IEEE J. Solid-State Circuits, vol. 40, no. 2, pp. 360-369, Feb, 2005.

[7] Ming-Da Tsai et al., "A 5-GHz low phase noise differential Colpitts CMOS VCO", IEEE Microw. Wireless Compon. Lett., vol. 15, no. 05, pp. 327-329, May, 2005.

[8] Young-Jin Moon, Yong-Seong Roh, Chan-Young Jeong, and Changsik Yoo, "A 4.39–5.26 GHz LC-Tank CMOS Voltage-Controlled Oscillator With Small VCO-Gain Variation" IEEE Microwave and Wireless Components Letters, vo. 19, NO. 8, AUGUST 2009.

[9] Chao Guo, Jun Hu, Siheng Zhu, Houjun Sun, Xin Lv, "A 5-GHz Low-Phase-Noise CMOS LC-VCO for China ETC Applications", Microwave Technology & Computational Electromagnetics (ICMTCE), 2011 IEEE International Conference, p. 267-269, 2011

[10] Y. K. Chu and H. R. Chuang, "A fully integrated 5.8GHz U-NII band 0.18-μm CMOS VCO", IEEE Microw. Wireless Compon. Lett., vol. 13 no. 07, pp. 287-289, Jul, 2003.

[11] Marc Tieout, Low power VCO design in CMOS, Birkhäuser, 2006.

[12] D. Ham and A. Hajimiri, "Concept and methods in optimization of integrated LC VCOs", IEEE J. Solid-State Circuits, vol. 36, no. 6, pp.896-909, Jun. 2001.

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