A 5-20 GHz 5-Bit True Time Delay Circuit in 0.18 μm CMOS Technology

Jae Young Choi[*], Moon-Kyu Cho[*], Donghyun Baek[**], and Jeong-Geun Kim[*]

Abstract—**This paper presents a 5-bit true time delay circuit using a standard 0.18 μm CMOS process for the broadband phased array antenna without the beam squint. The maximum time delay of ~106 ps with the delay step of ~3.3 ps is achieved at 5-20 GHz. The RMS group delay and amplitude errors are < 1 ps and <2 dB, respectively. The measured insertion loss is <27 dB and the input and output return losses are <12 dB at 5-15 GHz. The current consumption is nearly zero with 1.8 V supply. The chip size is 1.04 × 0.85 mm² including pads.**

Index Terms—**True time delay, CMOS, phased array antenna, beam squint, DPDT switch**

I. INTRODUCTION

Recently, the phased array antenna using the CMOS process is paid great attentions because the CMOS technology can enable to design low cost phased array antenna. The CMOS based phased array antennas are successfully demonstrated for the narrowband applications, which employ the phase shifter or the multiple phase of the local oscillator for the beam steering [1, 2]. However, the constant phase characteristic over the frequency in the phase shifter results in the different steered antenna beam position versus the frequency, which is known as beam squint [3].

Therefore, the true time delay (TTD) providing constant time delay, τ, over the frequency becomes one of the most essential elements in the broadband phased array antenna since the TTD can prevent the beam squint. Integrating the TTD circuit on a chip is difficult because it requires large chip area to realize the required time delay. Therefore, reducing the chip size is very important design issue in the TTD design. Most of the TTD has been realized using the SPDT switch and the artificial time delay with GaAs technology in Fig. 1(a) or MEMS technology [4, 5]. Since the conventional TTD requires many SPDT switches and inductors which result in high insertion loss and large chip size, the number of the switches and the size of inductor should be reduced. CMOS TTDs reported as trombone or active distributed configuration, however, they cannot provide compact
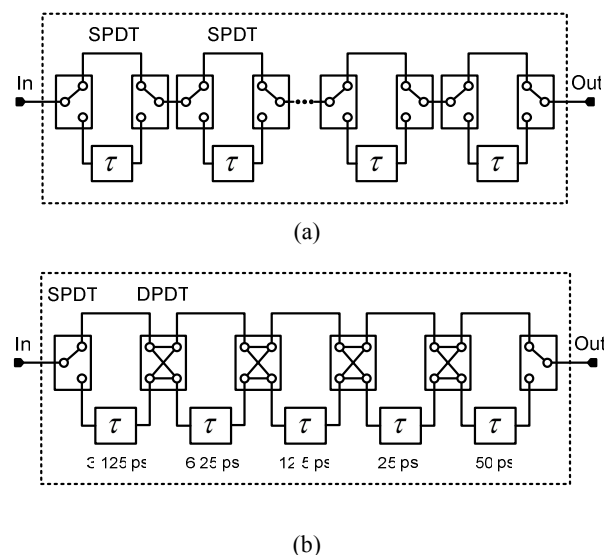

(a)

(b)

Fig. 1. Block diagrams of (a) the conventional TTD circuit using the SPDT switches, (b) the proposed TTD circuit using the DPDT switches.

size and flat delay performance [6, 7].

In this paper, a 5-bit bi-directional CMOS TTD with compact size and flat time delay response is presented.

II. CIRCUIT DESCRIPTION

1. Design of 5-Bit True Time Delay Circuit

The 5-bit TTD circuit is composed of two SPDT switches, four DPDT switches, time delay elements, and a switch controller as shown in Fig. 1(b). The group delay variation range of the designed TTD circuit is 97 ps with 3.125 ps delay step, which is equivalent of 760° phase shift with 11.25° step at 10 GHz. The minimum time delay of 3.125 ps for the least significant bit is implemented with a grounded CPW transmission line of the characteristic impedance of 50 Ω. The other time delay elements are implemented by cascading artificial transmission lines with CLC π-network in series to reduce the chip size as shown in Fig. 2. The group delay of π-network is approximately written by

$$T_D = n\sqrt{LC} \qquad (1)$$

where n is the number of sections. The calculated inductance of L and the capacitance of C to obtain the required time delay of 3.125 ps are 158 pH and 62 fF, respectively, while maintaining the characteristic impedance of 50 Ω. 16 inductors are used in the longest time delay line of 50 ps, therefore, vertically stacked spiral inductors with the top metal (M6) and the two connected metals (M4 and M5) with via are used to reduce the chip size in Fig. 2(b). The simulated quality factor of the 158 pH is about 10 at 10 GHz. The shunt capacitance of 62 fF is too small to implement with MIM capacitor supported by PDK, therefore, the MOM (Metal-Oxide-Metal) capacitor is implemented with the
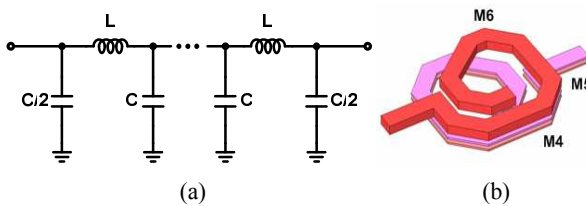
top plate of M1, M3, and M5 metals and the bottom plate of M2, M4, and M6 metals. All the inductors, MOM capacitors, transmission lines, and other interconnection lines were carefully simulated using the electromagnetic (EM) simulator of SONNET.

The proposed TTD employs the series-shunt DPDT switches, which can reduce the number of the series switching transistors in the signal path. Since the insertion loss of the TTD is mainly determined by the series transistors of the SPDT and the DPDT switches, therefore, the number of the series transistors in the signal path should be reduced to improve the insertion loss. Fig. 3(a) shows the DPDT switches using the series-shunt configuration for high isolation. The DPDT switch is implemented with four parallel- and cross-connected series transistors of 30-fingers 45 μm (T_1-T_4) and four shunt transistors of 10-fingers 15 μm (T_5-T_6). Only one transistor turns on between the input and output ports, so DPDT switch can provide low loss characteristics in the TTD compared to the TTD only with SPDT switches. The shunt transistors (T_5-T_6) improve the isolation to prevent unwanted leakage signals. The series inductors
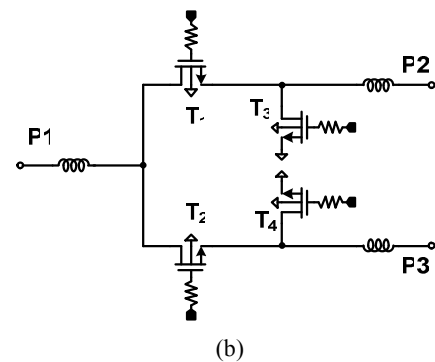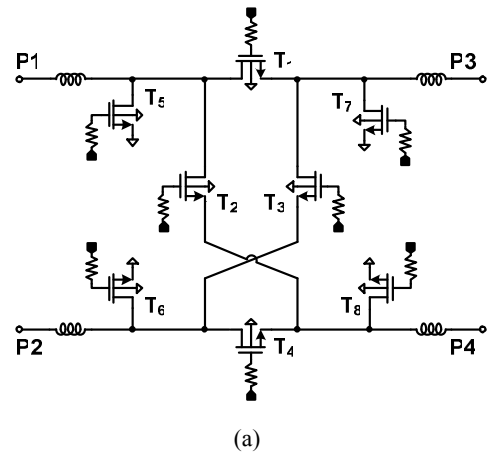

(a)

(b)

Fig. 3. Schematic of (a) the DPDT, (b) the SPDT switch.

Fig. 2. (a) Schematic the artificial delay element, (b) structure of the stacked spiral inductor.

(L_1) of 340 pH are included to improve the matching characteristic. The simulated insertion loss and the isolation are < 2 dB and >25 dB up to 20 GHz. The SDPT switch with the series-shunt configuration is used at the input and output ports in Fig. 3(b).

In the proposed 5-bit TTD configuration, the input signal passes through only 6 series transistors. The insertion loss can be saved by 4 series transistors when it is implemented only with SPDT switches. The simulated insertion losses of the TTD are achieved < 25 dB at 5-15 GHz. The simulated input and output return losses are less than 15 dB at 5-20 GHz. The proposed TTD circuit provides bi-directional operation since it is implemented with only passive devices. Also, the digital control circuit is integrated to turn on and off the switches properly.

IV. MEASUREMENT RESULTS

The 5-bit TTD circuit is fabricated in a standard 0.18 μm CMOS technology. Fig. 4 shows the microphotograph of the TTD circuit. The chip size is 1.04×0.85 mm^2 including pads. The SOLT calibration was performed for the on-wafer measurement. Fig. 5 shows the measured unwrapped phase and group delay characteristics in all states. The maximum time delay of 106 ps with 3.3 ps step at 10 GHz is achieved, which is equivalent to 31.8 mm in electrical length in the air. There are no overlapping group delay states and it shows flat time delay response at 5-20 GHz. Fig. 6 shows the measured input and output return losses in all states. The measured input and output return losses are less than 12 dB at 5-20 GHz. The measured insertion losses are
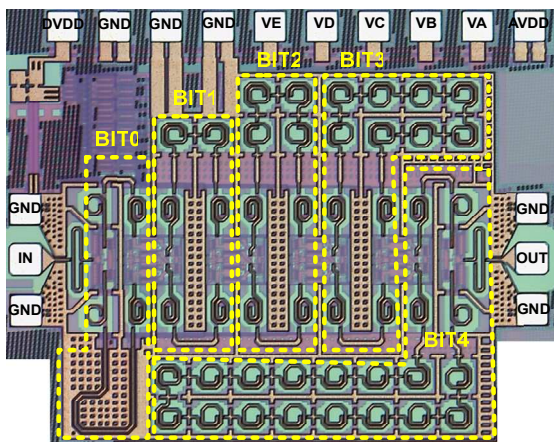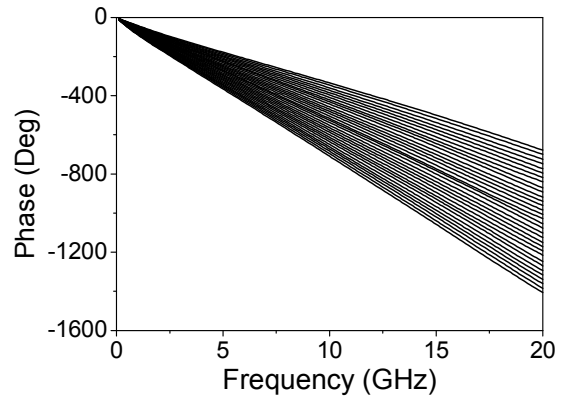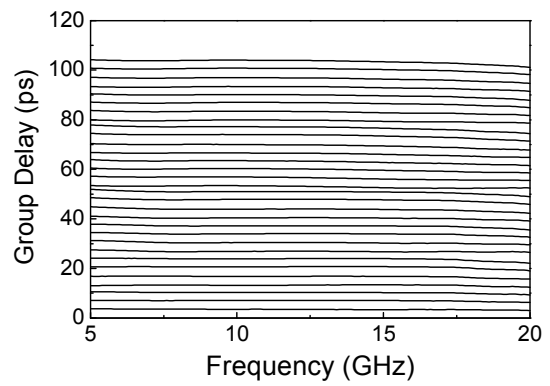
achieved < 27 dB at 5-15 GHz in Fig. 7. This is because the measured insertion loss of the SPDT switch is < 2 dB and the isolation is > 20 dB from DC to 20 GHz, while the insertion loss of < 1 dB and the isolation of > 20 dB are achieved in the DPDT. The measured RMS amplitude error of < 2 dB and the RMS group delay error of < 1 ps are achieved at 5-20 GHz in Fig. 8. The total

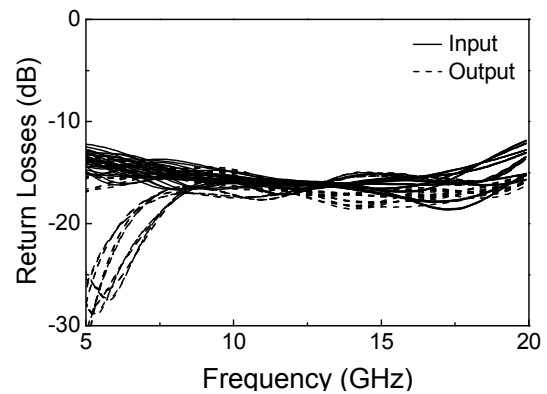**Fig. 5.** (a) Measured phase, (b) group delay of the TTD (all states).

Fig. 6. (a) Measured phase, (b) group delay of the TTD (all states).

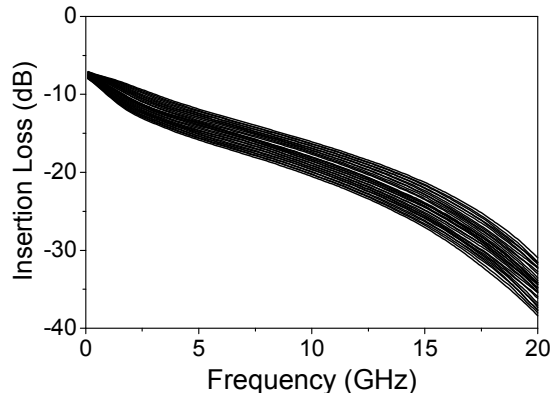**Fig. 4.** Microphotograph of the 5-bit CMOS TTD.

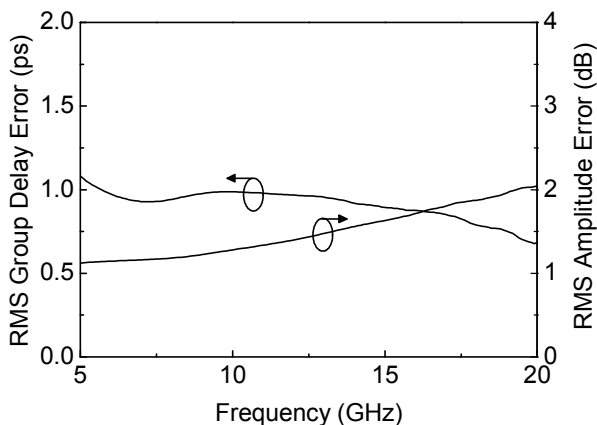**Fig. 7.** Measured insertion loss of the TTD (all states).

Fig. 8. Measured RMS group delay and amplitude errors of the TTD.

DC power consumption is nearly 0 mW with 1.8 V supply voltage.

V. CONCLUSIONS

This paper presents a 5-bit CMOS true time delay circuit. The series-shunt DPDT and SPDT switches are used in the proposed CMOS TTD. The chip size is reduced effectively using the artificial delay line with the on-chip stacked inductors and the MOM capacitors. The maximum group delay of ~106 ps with the delay step of ~3.3 ps is achieved. The RMS group delay and amplitude errors are <1 ps and <2 dB at 5–20 GHz, respectively. The measured insertion loss is <27 dB at 5-15 GHz. The insertion loss can be improved with the low loss switch configuration such as body floating technique. The current consumption is nearly zero with 1.8 V supply. The CMOS TTD circuit can be applied to the beam squint free wideband phased array antenna.

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