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비교기 기반 입력 전압범위 감지 회로를 이용한 6비트 500MS/s CMOS A/D 변환기 설계

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Design of a 6-bit 500MS/s CMOS A/D Converter with Comparator-Based Input Voltage Range Detection Circuit

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요 약

입력 전압 범위 감지 회로를 이용해서 저전력 6비트 플래시 500Ms/s ADC를 설계하였다. 입력 전압 범위 감지 회로는 변환기내 모든 비교기들 중에서 25%만 동작시키고, 나머지 75%는 동작시키지 않는 방법을 채택하므로 저전력 동작을 가능하게 설계 및 제작하였다. 설계된 회로는 0.13um CMOS 공정기술을 이용해서 제작하였고, 1.2V 전원전압에서 68.8mW 전력소모, 4.9 유효 비트수, 4.75pJ/step의 평가지수가 측정되었다.

Key Words : Analog-to-Digital Converter, flash, range detection circuits

ABSTRACT

A low power 6-bit flash ADC that uses an input voltage range detection algorithm is described. An input voltage level detector circuit has been designed to overcome the disadvantages of the flash ADC which consume most of the dynamic power dissipation due to comparators array. In this work, four digital input voltage range detectors are employed and each input voltage range detector generates the specific clock signal only if the input voltage falls between two adjacent reference voltages applied to the detector. The specific clock signal generated by the detector is applied to turn the corresponding latched comparators on and the rest of the comparators off. This ADC consumes 68.82mW with a single power supply of 1.2V and achieves 4.9 effective number of bits for input frequency up to 1MHz at 500 MS/s. Therefore it results in 4.75pJ/step of Figure of Merit (FoM). The chip is fabricated in 0.13-um CMOS process.

Ⅰ. Introduction

ULTRA-WIDEBAND is a radio technology which pioneered and may be used at a very low energy level for short-range, wide-bandwidth communications using a large portion of the radio spectrum. Wireless communication standards using impulse radio UWB such as either 802.15.4a WPAN or 802.15.6 WBAN, require low-resolution (3 to 6 bits) and high-speed ADCs. Because of the high speed of operation, flash-based converters are often preferred for this application, but alternatives based

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on pipelining or SAR are also being developed. High conversion speed also requires larger power dissipation. However, lower power dissipation should be met in some portable applications. Consequently, the main challenge to design the flash analog-to-digital converter is the trade-off between high speed and large power dissipation.

Averaging technique[1] in flash ADC reduces the offset voltage of pre-amplifiers. The adjacent outputs of pre-amps are coupled via averaging resistors. The averaging resistor network sums the outputs of many pre-amps, each possibly having errors, and finds the average balance point. If the pre-amp nearest to balance has errors, its output will not agree with the average balance point. Current will then flow between the pre-amp and averaging resistor network adjusting pre-amp gain. The equivalent circuit for error signals shows the pre-amp load to be a parallel combination of the load resistors and the integrating network resistors. The effect is a gain-selective architecture in which error signals see less gain than the input signal. Or in a more intuitive explanation, the effective gate area of the differential pairs is increased by averaging, thus, offset voltage is reduced.

Although the averaging over amplifier stages shows a positive effect for offset voltage and dynamic range, at the edges of the system a non-linearity is found. This error is called edge effect and caused by where the averaging amplifier array ends and not equal amount of averaging amplifiers are contributed. This problem can be easily solved by adding dummy amplifiers (generally more than 6 dummy amplifiers for each edge) but with a drawback of more power dissipation and die area. Instead of dummy amplifiers, specialized designed amplifiers are applied to the end of the amplifier array to reduce the power and chip area [2,3].

Another type of averaging is capacitive averaging [4]. Capacitors are applied to couple the adjacent amplifiers rather than resistors. The advantages of capacitive averaging is no need for a reference resistor ladder, implicit sample-and-hold operation, no edge effects in the averaging network (as compared to resistive averaging), and a very low input capacitance. Also, no external sample-and-hold is required, because the averaging capacitors at each stage are readily used as sampling capacitors implementing a multistage input- and output-offset-sampling architecture with distributed front-end sample-and-hold. In general, a distributed sample-and-hold poses a more severe burden on the driving stage than a dedicated sample-and-hold, because the capacitor to be charged is multiplied by the interpolation factor at the front-end of the converter. Additionally, the sampling capacitors in this architecture also retain the information of the last sample, because no discharge occurs during the amplification phase.

Analog input range detection circuits were applied in some design[5]. When the frequency of the input signal is high, the performance of the ADC drops fast due to the bandwidth limitation of analog input range detection circuits. In this design, we replace analog input range detection circuits to digital logic circuits. Thus the proposed input range detection circuits have a good performance in high speed operation.

The rest of the paper is followed as below. In section 2, the proposed ADC architecture is shown and the core idea block is explained. The measurement results are shown in section 3. At last, a brief summary is given in section 4.

Ⅱ. Input Voltage Range Detection Circuits

The block diagram of the proposed 6-bit flash ADC is illustrated in Figure 1. The proposed ADC consists of input range detection circuit with clock distribution, a resistor ladder, 1st and 2nd pre-amps, averaging circuits, latched comparators, an error correction circuit, encoder, and flip-flops.

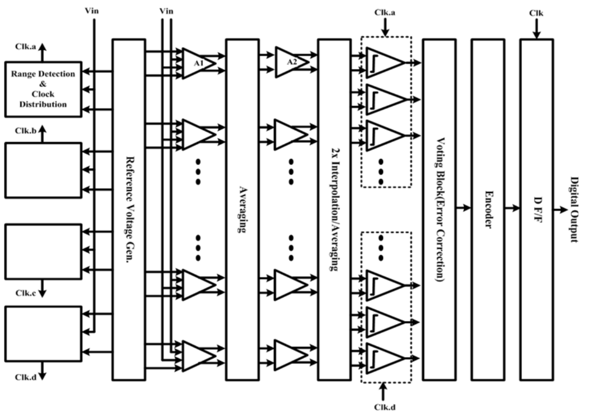


Fig. 1. Block diagram of proposed ADC.

The pre-amp array amplifies reduce the kick-back noise and overcome the offset of comparator in the next stage. Averaging and 2nd interpolation/Averaging blocks are employed not only to improve the offset and mismatch between adjacent pre-amps, but to enhance the static performances[6]. Latched comparators compare the output signals from pre-amp array with the reference signal. To overcome the weakness of the flash requiring a large power dissipation due to comparator array, four input range detection circuits are employed to turn the corresponding latched comparators on and the rest of the latched comparators off. In this manner, dynamic power dissipation of the proposed ADC can be reduced down to one fourth with respect to that of the conventional one. The circuit diagram of the input range detection circuit is shown in Figure 2. The range detection circuit compares the input signal to reference a. and reference b.

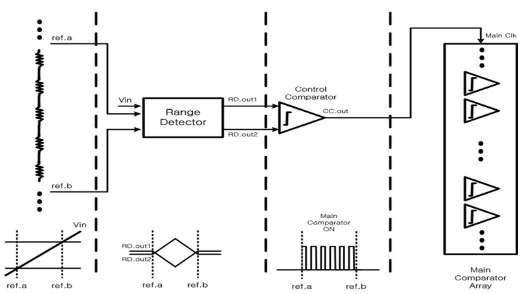


Fig. 2. On/off algorithm of comparator by Input voltage Range detector.

When the input signal is larger than ref b. and smaller than ref a, the output of the circuit becomes high, otherwise low. When the output becomes high, which means the signal level falls between reference a. and reference b, the clock will turn the corresponding main comparators on and others off. In this manner, the power dissipation due to the main comparator array is reduced because the operation of the total main comparator array is dynamic. Figure 3 shows the clock signals that are generated from four input range detection circuits in 500MHz sampling speed.

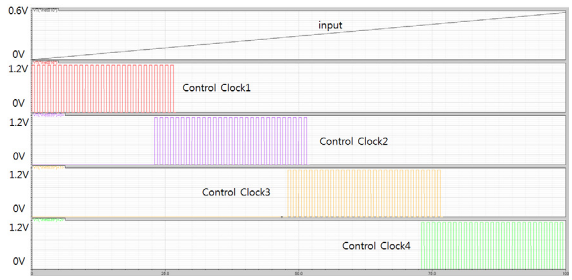


Fig. 3. The clock signals that generated from four input range detection circuits.

The input full scale is 0.6V. The digital power supply is 1.2V. The clock signals are distributed to the corresponding latched comparators. In this design, the four range detection circuits are used to generate total. 4 control clocks. Averaging technique is employed at the output of the pre-amplifier array to reduce the INL and DNL. Dummy pre-amplifiers are utilized to isolate the terminal effect of the averaging technique. Bubble-error-correction circuit changes the thermometer code to 1-of-N code and isolates the bubble error. Rom-type encoder is employed to change the 1-of-N code to binary output code. At last, the 6-bit binary output is synchronized by TSPC flip-flops.

Compared to the analog range detection circuit in [5], the proposed digital range detection circuit is robust with respect to the input signal speed. Analog range detection circuit suffers from bandwidth limitation, while digital range detection circuit doesn't. The schematic of the proposed digital range detection circuit is illustrated in Figure 4.

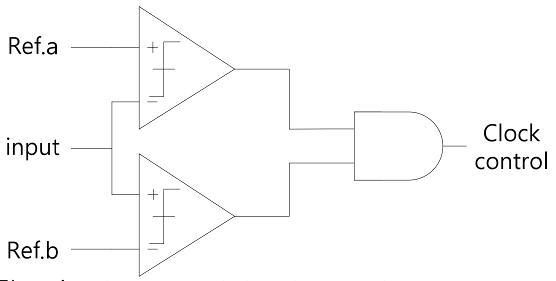


Fig. 4. The proposed digital range detection circuit.

The proposed digital range detection circuit consists of two high speed latched comparators and one AND gate. When the input signal stays larger than Ref b. and smaller than Ref a, then both of the output of the comparators become high, thus the clock control signal out of the AND gating with two outputs of the comparator becomes high. The simulation result of the proposed digital range detection circuit is shown in Figure 5.

The comparator employed in the digital range detection circuit receives the high frequency input signal and generates high speed control clock for data conversion. Hence a comparator with high performance and low offset is demanded[7]. The jitter noise of the control clock decides the performance of the A/D converter[8]. The schematic of the low offset comparator is illustrated in Figure 6.

The two regenerative flip-flops in the comparator for strobe consist of PMOS transfer gate pair (MP4, MP5), PMOS switch MP3 for reset and NMOS flip-flop(MN5, MN6) with NMOS pre-discharge transistors(MN3, MN5). The regeneration operation compares the signal directly, so that the operation speed is high and power dissipation is relatively low. There are two operation mode in this comparator, namely, reset mode and regeneration mode. When clkb becomes low, the comparator stays in reset mode. The logic output of the previous comparison is reset by the current flowing through MP3. PMOS pre-discharge transistor is reset and NMOS flip-flop is coupled to ground. When clkb becomes high, reset switch MP3 becomes open and clk stays low. The PMOS flip-flop and NMOS flip-flop are coupled to each other. This comparator is capable for high speed operation.

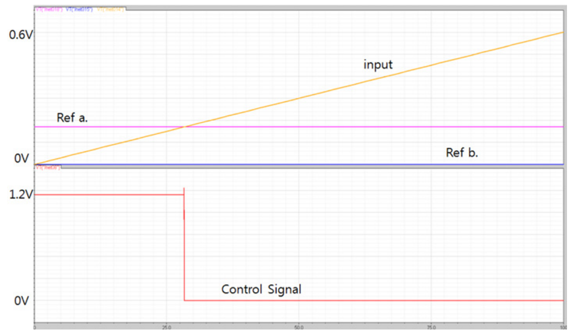


Fig. 5. Simulation result of the proposed digital range detection circuit.

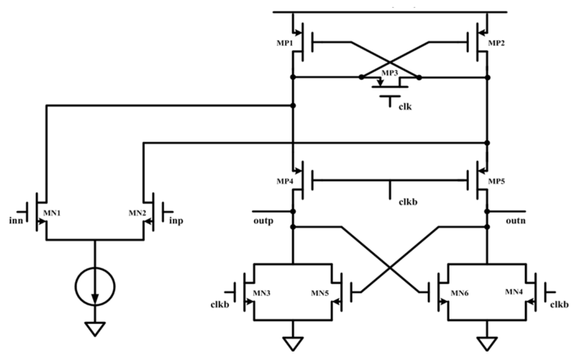


Fig. 6. Schematic of the low offset comparator.

Ⅲ. Measurement Results

The signal inputs and clocks are placed on the bottom and top, respectively; analog bias voltages or currents come into the top, while high speed digital data goes out at the bottom to eliminate coupling effects from analog signals. The conversion blocks are placed sequentially with the signal processing flow, in order to shorten their routing distance, and hence, delay[9]. Clock generation and output buffers are placed away from the analog cores to suppress the substrate noise coupling. The layout floor plan of the proposed flash A/D converter is shown in Figure 7. The proposed A/D converter is fabricated by the 0.13um CMOS 1-poly 6-metal process. The die photo is illustrated in Figure 8. The total chip area occupies 2.22mm2 (3700um×600um).

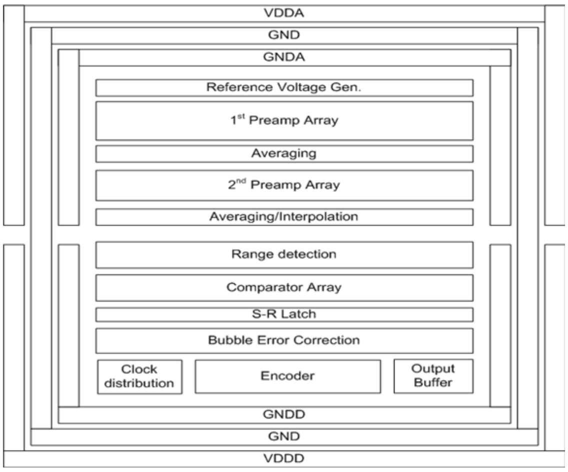


Fig. 7. Layout floor-plan of the proposed A/D converter.

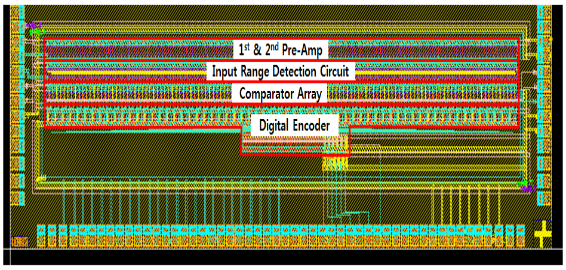


Fig. 8. Die photo of the proposed A/D converter.

The test PCB board to evaluate the performance of the proposed A/D converter is illustrated in Figure 9. The digital power and analog power are separated to isolate the switching noise. The analog input signal and clock signal are applied through SMA connectors. The single-ended analog input signal is then changed into differential signal by the transformer. The output 6bit digital signals are connected to logic analyzer with jumper pins.

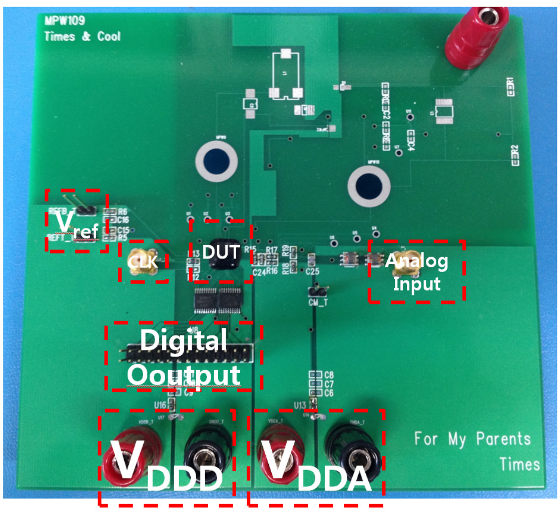


Fig. 9. Test-board of the proposed A/D converter.

The measurement environment is illustrated in Figure 10. The input analog signal is generated by the function generator [33250A]. The high speed clock signal is provided by the pattern generator [E4421B]. DC power and reference voltage are supplied by DC power supply [E3646A]. The output code of the proposed A/D converter is measured by logic analyzer [TLA601]. The Wave Vision software with National Semiconductor is used to evaluate the dynamic performance of the proposed A/D converter.

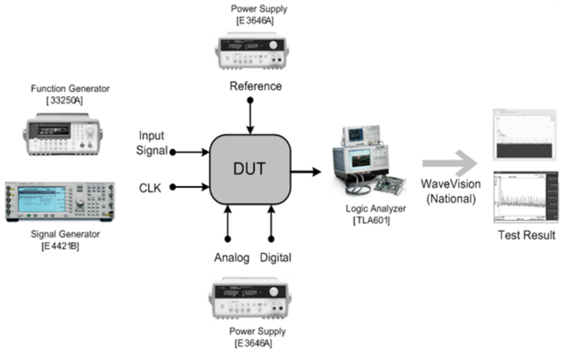


Fig. 10. Measurement environment

The frequency of the analog input signal is 1MHz with the full scale range 0.6V. The sampling speed is 100MS/S. In order to make the spectrum analysis, the reconstructed output is Fast-Fourier Transformed, as illustrated in Figure 11. The SINAD(Signal to Noise ratio with Distortion) of the proposed ADC in this measurement is 30.99dBc and SFDR(Suprious Free Dynamic Range) is 41.48dBc. SINAD and ENOB(Effective Number of Bit) versus input frequency at 250MHz sampling speed and 500MHz sampling speed are illustrated in Figure 12 and Figure 13, respectively.

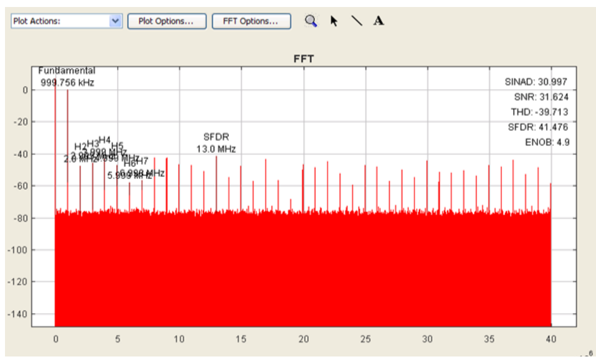


Fig. 11. Spectrum analysis @ 100MS/S.

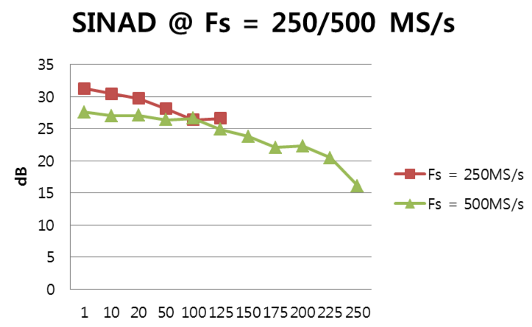


Fig. 12. SINAD versus input frequency.

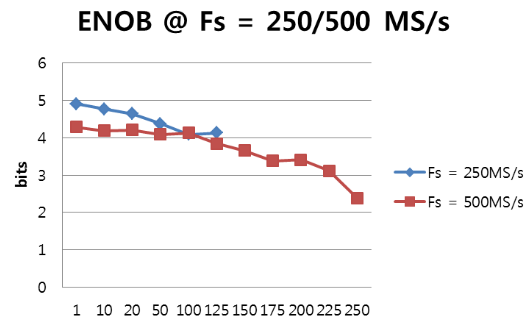
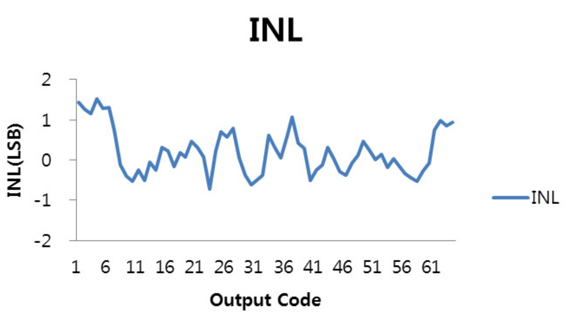


Fig. 13. ENOB versus input frequency.

Another important specification to evaluate A/D converter is its static performance, INL(Integral Non-Linearity) and DNL (Differential Non-Linearity). The measured INL and DNL of the proposed A/D converter are illustrated in Figure 14. The edge part of INL is worse than that in the center due to the terminal effect of the averaging technique. Although dummy pre-amplifiers were placed, the measurement results show more dummy pre-amplifiers are necessary.



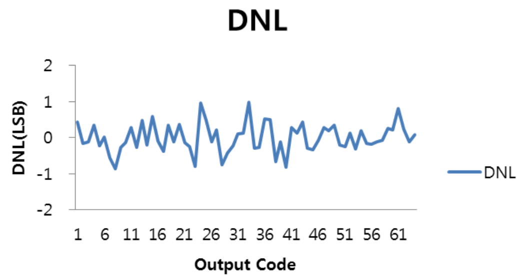


Fig. 14. INL/DNL measurement result.

The measurements result including FoM of the proposed A/D converter is compared with those from the literature in Table 1.

Table 1. Comparison with 6-bit resolution flash A/D converter

	This work	[5] Kim	[4] 2005	[2] 2008	[1] 2001
Resolution	6bit	6bit	6bit	6bit	6bit
Sampling Freq.	500MS/s	250MS/s	1.2GS/s	1.6GS/s	1.1GS/s
Power Supply	1.2V	1.8V	1.5V	1.2V	3.3V
P_{diss}	68.82mW	106mW	160mW	180mW	300mW
DNL/INL	−0.87/+0.95 LSB −0.72/+1.51 LSB	−0.7/+0.9 LSB −1.8/+1.2 LSB	±0.4/0.6 LSB	±0.5/0.4 LSB	<±0.7LSB
SINAD	30.99dBc(fin=1MHz)	33.5dBc (fin=1MHz)	35.4dBc (fin=600MHz)	30dBc (fin=800MHz)	35.7dBc (fin=450MHz)
FoM	4.75pJ/Hz	17.5pJ/Hz	5.2pJ/Hz	6.6pJ/Hz	12.8pJ/Hz
Input Range	0.6Vpp	0.8Vpp	1.0Vpp	0.84Vpp	1.5Vpp

The proposed A/D converter has a relatively lower sampling speed due to the input range detection circuit. Because the analog input is used to determine which control clock turns on by the range detection circuit first, if the sampling speed is too high, timing skew of the clock causes the performance degradation of the A/D converter.

Ⅳ. Summary

In this paper, the latched comparator array is divided into four groups and each group consists of 16 latched comparators.. They are controlled by four different clocks. Those clocks are generated from input range detection circuits. The input range detection circuits turn the corresponding latched comparators on and the rest of the comparators off which is decided by the input signal voltage level. In this manner, dynamic power dissipation of the proposed A/D converter can be reduced down to one fourth with respect to that of the conventional one.

In analog block, the input stage of the proposed A/D converter is differential architecture to reduce the common mode noise. The proposed A/D converter is implemented in the 0.13um CMOS 1Poly 6Metal technology. The measured results show 68.82mW power dissipation with a 1.2V supply voltage. It shows 4.3bit ENOB at maximum sampling frequency 500MHz with 1MHz input frequency and 4.9bit ENOB at maximum sampling frequency 250MHz with 1MHz input frequency. The measured results of DNL/INL are -0.9/+1.0 LSB, -0.7/+1.5 LSB. It is expected that the proposed A/D converter can be embedded into UWB applications such as wireless USB system and ubiquitous sensor network system, where power dissipation is a critical specification to the system.

감사의 글

반도체 설계 교육센터(IDEC)의 CAD Tool 지원에 감사드립니다. 본 논문은 인하대학교의 지원에 의하여 연구되었습니다.

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