

Simplified Control Scheme of Unified Power Quality Conditioner based on Three-phase Three-level (NPC) inverter to Mitigate Current Source Harmonics and Compensate All Voltage Disturbances

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Abstract – This paper proposes a simplified and efficient control scheme for Unified Power Quality Conditioner (UPQC) based on three-level (NPC) inverter capable to mitigate source current harmonics and compensate all voltage disturbances perturbations such as, voltage sags, swells, unbalances and harmonics. The UPQC is designed by the integration of series and shunt active filters (AFs) sharing a common dc bus capacitor. The dc voltage is maintained constant using proportional integral voltage controller. The shunt and series AF are designed using a three-phase three-level (NPC) inverter. The synchronous reference frame (SRF) theory is used to get the reference signals for shunt and the power reactive theory (PQ) for a series APFs. The reference signals for the shunt and series APF are derived from the control algorithm and sensed signals are injected in tow controllers to generate switching signals for series and shunt APFs. The performance of proposed UPQC system is evaluated in terms of power factor correction and mitigation of voltage, current harmonics and all voltage disturbances compensation in three-phase, three-wire power system using MATLAB-Simulink software and SimPowerSystem Toolbox. The simulation results demonstrate that the proposed UPQC system can improve the power quality at the common connection point of the non-linear load.

Keywords: Three-level(NPC) inverter, UPQC, Current harmonics mitigation, Voltage compensation, Shunt active filter, Series active filter, Power quality improvement

1. Introduction

There has been a continuous rise of nonlinear loads over the years due to intensive use of power electronic control in industry. The utility supplying these nonlinear loads has to supply large vars. Moreover, the harmonics generated by the nonlinear loads pollute the utility. The basic requirements for compensation process involve precise control with fast dynamic response and on-line elimination of load harmonics. The traditional compensation methods using switched capacitor and thyristor controlled inductor [1-2] coupled with passive filters are increasingly replaced by active power filters (APFs) [3-4]. The two types of APFs are shunt and series APF, the shunt APFs are used to mitigate current harmonics and reactive power compensation. The series APFs are used to compensate voltage related problems, such as voltage harmonics, sags, swells, unbalances, flicker, etc.

The Unified Power Quality Conditioner (UPQC) is one of the best solutions to compensate both current- and voltage-related problems simultaneously [5], it is the integration of shunt and series APFs through a common DC link capacitor. Unified Power Quality Conditioner has

been widely studied to eliminate or mitigate the disturbances propagated from the source side and the other loads interconnected [6-7]. In the normal operation of UPQC, the control circuitry of shunt APF calculates the compensating current for the current harmonics and the reactive power compensation. The error signal thus derived is processed in pwm current controller.

The function of the series APF in UPQC is to compensate the all voltage perturbations. The control circuitry of the series APF calculates the reference voltage to be injected by the series APF by comparing the terminal voltage with a reference value of voltage.

This paper presents a 3-phase, 3-wire UPQC configuration based on three-level (NPC) inverter using simplified control scheme. The series AF is controlled to maintain voltage load to the reference level and to eliminate supply voltage sag/swell, harmonics and unbalance from the load terminal voltage. The shunt AF is controlled to mitigate the supply current harmonics. The dc bus voltage is maintained constant by the shunt active filter. The performances of the proposed UPQC system are verified through simulations for transient and steady-state conditions using Matlab-Simulink software and SimPowerSystem Toolbox.

2. UPQC Configuration System

Fig. 1 shows the proposed three-phase three-wire UPQC

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connected to a power system feeding a nonlinear load. It consists of two three-level (NPC) inverters one for the shunt active filter and the second for a series active filter. The dc link of both active filters is connected to a common dc capacitor of 3000 μ F. The series filter is connected between the supply and load terminals using three single phase transformers with turn's ratios of 1:1. In addition to injecting the voltage, these transformers are used to filter the switching ripple of the series active filter. A small capacity rated C_{sf} filter [8] is used with inductance to eliminate the high switching ripple content in the series active filter injected voltage. The three-level inverters for both the active filters are designed with IGBTs (Insulated Gate Bipolar Transistors). The three leg shunt active filter is connected ahead of a series filter through a small capacity rated inductive filter. The control algorithm of UPQC is based on synchronous reference frame detection method for the shunt AF and instantaneous reactive power theory for the series [9].

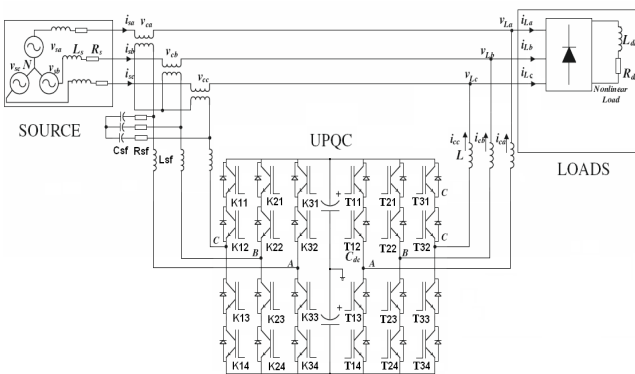


Fig. 1. UPQC configuration system

2.1 Three-level (NPC) inverter

Since the introduction in 1981 [10], the three-level neutral-point-clamped (NPC) voltage source inverter has attracted popular attentions. Apart from its application in high-capacity ac motor drive, other interesting applications of this topology include HVDC transmission, STATCOM, Active Power Filters, PWM rectifier, as well as renewable energy interfacing applications. Although the three-level NPC topology provides significant advantages over the conventional two-level's in high-power applications. In power quality applications, the three-level topology has been used in SVC's [3], UPFC [11], etc., due to its high speed and wide range of reactive power. On the other hand, the application of NPC voltage source converters to Unified Power Quality Conditioners (UPQCs) is being limited by the unbalance DC link voltages due to the inherent transient operating condition. The advantages of these structures are:

- Near sinusoidal current waveforms due to reduced unwanted harmonics in the voltage PWM waveforms,

- Each power valve takes half the DC link voltage, thus the topology can handle twice the voltage respect to the two level topology for a given semiconductor,
- The first set of unwanted harmonics is at twice the switching frequency,
- It reduces the overvoltage produced by the wave reflection in long cables.

Fig. 2 shows the power circuit of the three-level neutral point clamped inverter based on the six main switches (T11, T21, T31, T14, T24, T34) of the traditional two-level inverter, with six auxiliary switches (T12, T13, T22, T23, T32, T33) and two neutral clamped diodes added on each bridge arm. The diodes are used to create the connection with the point of reference to obtain midpoint voltages. This structure allows the switches to endure larger dc voltage input on the premise that the switches will not raise the level of their withstand voltage. For this structure, three output voltage levels can be obtained, namely, $U_d/2$, 0, and $-U_d/2$ corresponding to three switching states A, 0, and B. As a result, 27 states of switching output exist in the three-phase three-level inverter [12-13-22].

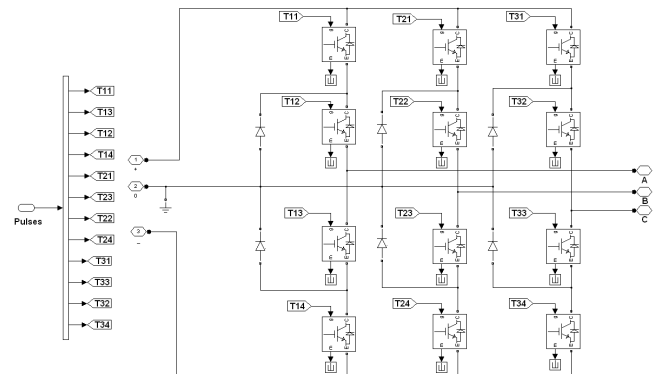


Fig. 2. Three-level (NPC) inverter

2.1.1 Hysteresis control

The principle of the conventional control scheme based on hysteresis technique in the case of shunt active filter using three-level (NPC) inverter is described below [14].

The three-phase source voltages are given as:

$$\begin{aligned} V_{sa} &= V \cdot \sin(\omega t) \\ V_{sb} &= V \cdot \sin(\omega t - \frac{2\pi}{3}) \\ V_{sc} &= V \cdot \sin(\omega t + \frac{2\pi}{3}) \end{aligned} \quad (1)$$

Where V is the peak value of phase voltage in the phases a, b, and c respectively. Hysteresis current controller is used to track the compensated current references. The relationship between the input and output of the hysteresis comparator is expressed as:

$$hys(\Delta i_{cx}) = \begin{cases} 1, & \text{if } \Delta i_{cx} > h \\ 0, & \text{if } \Delta i_{cx} < -h \end{cases} \quad (2)$$

$$\Delta i_{cx} = i_{cx}^* - i_{cx}; x = a, b, c$$

Three valid switching states in each phase are used to generate three different voltage levels on the ac side of the inverter. One high voltage level and one low voltage level are present in the positive and negative phase voltages. In the positive phase voltage, two voltage levels, 0 and $U_d/2$, are generated on the voltages U_{ao} , U_{bo} , and U_{co} . Voltage level $U_d/2$ is selected to decrease the compensated current. Voltage level 0 is used to increase the compensated current in the positive supply voltage. In the negative half-cycle of phase voltage, Voltage levels $-U_d/2$ and 0 are generated on the ac side voltage of the inverter. Voltage level $-U_d/2$ is produced to increase the compensated current. On the other hand, high level 0 is generated to decrease the compensated current in the negative phase voltage. Thus, the low voltage level is selected to increase the compensated current and high voltage level is employed to decrease the compensated current in each half-cycle of phase voltage. Based on the above description, the switching signals of power switches are expressed as [14-15]:

$$T_{a1} = \text{sign}(V_{sa})[1 - hys(\Delta i_{ca})] \quad (3)$$

$$T_{a2} = [1 - \text{sign}(V_{sa})]hys(\Delta i_{ca}) \quad (4)$$

$$S_a = \text{sign}(V_{sa})hys(\Delta i_{ca}) + [1 - \text{sig}(V_{sa})].[1 - hys(\Delta i_{ca})] \quad (5)$$

$$T_{b1} = \text{sign}(V_{sb})[1 - hys(\Delta i_{cb})] \quad (6)$$

$$T_{a2} = [1 - \text{sign}(V_{sb})]hys(\Delta i_{cb}) \quad (7)$$

$$S_b = \text{sign}(V_{sb})hys(\Delta i_{cb}) + [1 - \text{sig}(V_{sb})].[1 - hys(\Delta i_{cb})] \quad (8)$$

$$T_{c1} = \text{sign}(V_{sc})[1 - hys(\Delta i_{cc})] \quad (9)$$

$$T_{c2} = [1 - \text{sign}(V_{sc})]hys(\Delta i_{cc}) \quad (10)$$

$$S_c = \text{sign}(V_{sc})hys(\Delta i_{cc}) + [1 - \text{sig}(V_{sc})].[1 - hys(\Delta i_{cc})] \quad (11)$$

Where $\text{sign}(V_{sx}) = 1$ if $V_{sx} > 0$; or 0 if $V_{sx} < 0$ and $x = a, b, c$.

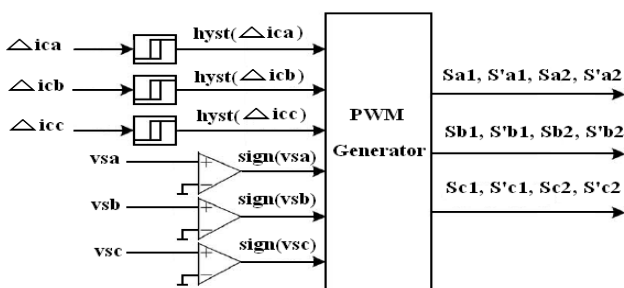


Fig. 3. Three-level (NPC) inverter hysteresis control

2.1.2 Logic control

To have the required gating signals a PWM logic controller is developed for both APFs. The difference

between the injected current (voltage) and the reference current (voltage) determine the modulation wave of the reference current (voltage). These signals are compared with two carrying triangular identical waves shifted one from other by a half period of chopping and generate switching pulses [14-15].

The control of inverter is summarized in the two following stages:

Determination of the intermediate signals V_{i1} and V_{i2} :

- If error $E_c \geq$ carrying 1 Then $V_{i1} = 1$
- If error $E_c <$ carrying 1 Then $V_{i1} = 0$
- If error $E_c \geq$ carrying 2 Then $V_{i2} = 0$
- If error $E_c <$ carrying 2 Then $V_{i2} = -1$

Where V_{i1} and V_{i2} are intermediate voltage, E_c is the difference between injected and reference currents.

Determination of control signals of the switches T_{ij} and V_{i2} ($i=1,2,3$; $j=1,2,3,4$):

- If $(V_{i1}+V_{i2})=1$ Then $T_{i1}=1, T_{i2}=1, T_{i3}=0, T_{i4}=0$,
- If $(V_{i1}+V_{i2})=0$ Then $T_{i1}=0, T_{i2}=1, T_{i3}=1, T_{i4}=0$,
- If $(V_{i1}+V_{i2})=-1$ Then $T_{i1}=0, T_{i2}=0, T_{i3}=1, T_{i4}=1$.

The simulink model of the logic control is shown in Fig. 4.

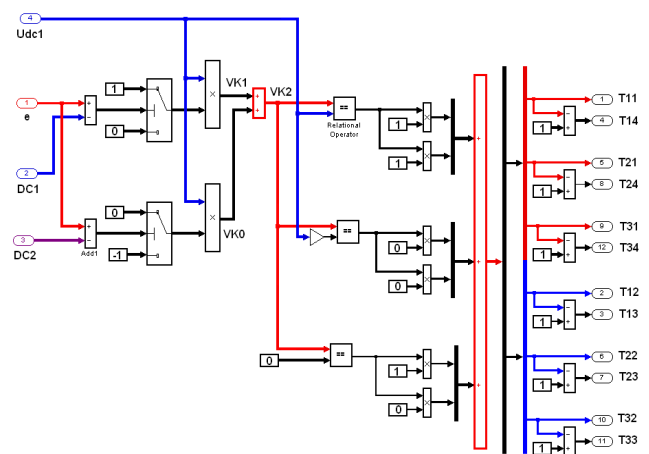


Fig. 4. Three-level (NPC) inverter PWM logic control

3. Control Strategy

The control strategy is basically the way to generate reference signals for both shunt and series APFs of UPQC. The compensation effectiveness of the UPQC depends on its ability to follow with a minimum error and time delay to calculate the reference signals to compensate the distortions, unbalanced voltages or currents or any other undesirable condition [16]. The conventional techniques reported in literature give poor results under distorted and/or unbalanced input/utility voltages, and they involve many calculations. The proposed control scheme is a simple

scheme to achieve effective compensation for source current harmonics, reactive power compensation and voltage harmonic mitigation even under distorted and/or unbalanced input/utility voltages.

3.1 Shunt AF control

The control strategy to compensate harmonic currents used in this work is based on the synchronous reference frame detection method. The principle of this technique is described below [17]. The three phase load currents i_{La} , i_{Lb} and i_{Lc} are transformed from three phase (abc) reference frame to two phase's (α - β) stationary reference frame currents i_α and i_β using:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (11)$$

Using a PLL (Phase Locked Loop), we can generate $\cos(\theta_{est})$ and $\sin(\theta_{est})$ from the phase voltage source v_{sa} , v_{sb} and v_{sc} .

The i_α and i_β currents expression in (d-q) reference frame are given by:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin(\theta_{est}) & -\cos(\theta_{est}) \\ \cos(\theta_{est}) & \sin(\theta_{est}) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (12)$$

The currents i_d is transformed to DC and harmonic components using a low pass filter:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \bar{i}_d + \tilde{i}_d \\ i_q \end{bmatrix} \quad (13)$$

The expression of the reference current $i_{\alpha-ref}$ and $i_{\beta-ref}$ are given by:

$$\begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} = \begin{bmatrix} \sin(\theta_{est}) & -\cos(\theta_{est}) \\ \cos(\theta_{est}) & \sin(\theta_{est}) \end{bmatrix}^{-1} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (14)$$

$$\begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} = \begin{bmatrix} \sin(\theta_{est}) & \cos(\theta_{est}) \\ -\cos(\theta_{est}) & \sin(\theta_{est}) \end{bmatrix} \begin{bmatrix} \bar{i}_d + \tilde{i}_d \\ i_q \end{bmatrix} \quad (15)$$

The reference currents in the (abc) frame are given by:

$$\begin{bmatrix} i_{a-ref} \\ i_{b-ref} \\ i_{c-ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} \quad (16)$$

Finally, the compensation currents i_{ca} , i_{cb} and i_{cc} are given by:

$$\begin{aligned} i_{ca} &= i_{a-ref} - i_{La} \\ i_{cb} &= i_{b-ref} - i_{Lb} \\ i_{cc} &= i_{c-ref} - i_{Lc} \end{aligned} \quad (17)$$

To compensate the inverter losses and regulate the DC link voltage U_{dc} , a proportional integral voltage controller is used. The control loop consists of the comparison of the measured voltage ($U_{dc1} + U_{dc2}$) with the reference voltage U_{dc-ref} . The loop generates corresponding current $I_{c,los}$ as given by:

$$I_{c,los} = K_p \cdot \Delta U_{dc} + K_i \int \Delta U_{dc} dt \quad (18)$$

3.1 Series AF control

The control strategy used for extracting the reference voltages of series active power filter is based on the p-q theory described in [18-19-22]. We assume that the three-phase voltage source in the grid is symmetric and distorted:

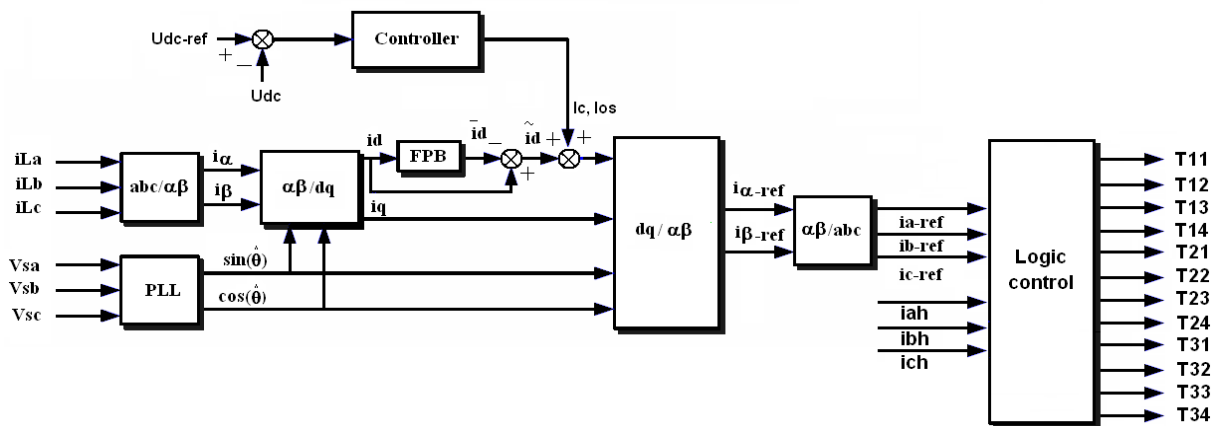


Fig. 5. Shunt active filter strategy control

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} \sqrt{2}U_n \sin(n\omega t + \theta_n) \\ \sum_{n=1}^{\infty} \sqrt{2}U_n \sin\left[(n\omega t - \frac{2\pi}{3}) + \theta_n\right] \\ \sum_{n=1}^{\infty} \sqrt{2}U_n \sin\left[(n\omega t + \frac{2\pi}{3}) + \theta_n\right] \end{bmatrix} \quad (19)$$

U_n and θ_n are respectively the rms voltage and initial phase angle, n is the harmonic order. When $n=1$, it means three-phase fundamental voltage source:

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} \sqrt{2}U_1 \sin(\omega t + \theta_1) \\ \sqrt{2}U_1 \sin\left[(\omega t - \frac{2\pi}{3}) + \theta_1\right] \\ \sqrt{2}U_1 \sin\left[(\omega t + \frac{2\pi}{3}) + \theta_1\right] \end{bmatrix} \quad (20)$$

Eq. (10) is transformed into $(\alpha-\beta)$ reference frame:

$$\begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} = C_{32} \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \sqrt{3} \begin{bmatrix} \sum_{n=1}^{\infty} U_n \sin(n\omega t + \theta_n) \\ \sum_{n=1}^{\infty} \mp U_n \sin(n\omega t + \theta_n) \end{bmatrix} \quad (21)$$

$$C_{32} = \frac{\sqrt{2}}{\sqrt{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (22)$$

Three-phase positive fundamental current template is constructed:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad (23)$$

Eq. (13) is transformed to $(\alpha-\beta)$ reference frame:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = C_{32} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \sin(\omega t) \\ -\cos(\omega t) \end{bmatrix} \quad (24)$$

According to the instantaneous reactive power theory [14], then:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_\alpha & u_\beta \\ u_\beta & -u_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (25)$$

Where DC and AC components are included:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} \bar{p} + \tilde{p} \\ \bar{q} + \tilde{q} \end{bmatrix} \quad (26)$$

p and q are passed through low pass filter (LPF) and DC component are got:

$$\begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} = \sqrt{3} \begin{bmatrix} U_1 \cos(\theta_1) \\ U_1 \sin(\theta_1) \end{bmatrix} \quad (27)$$

According to (25), transformation is made:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_\alpha & u_\beta \\ u_\beta & -u_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \quad (28)$$

As for DC components of p and q :

$$\begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} = \begin{bmatrix} u_{\alpha f} & u_{\beta f} \\ u_{\beta f} & -u_{\alpha f} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} u_{\alpha f} \\ u_{\beta f} \end{bmatrix} \quad (29)$$

The fundamental voltages in $(\alpha-\beta)$ reference frame are:

$$\begin{bmatrix} u_{\alpha f} \\ u_{\beta f} \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix}^{-1} \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} = \begin{bmatrix} i_\alpha & -i_\beta \\ i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} \quad (30)$$

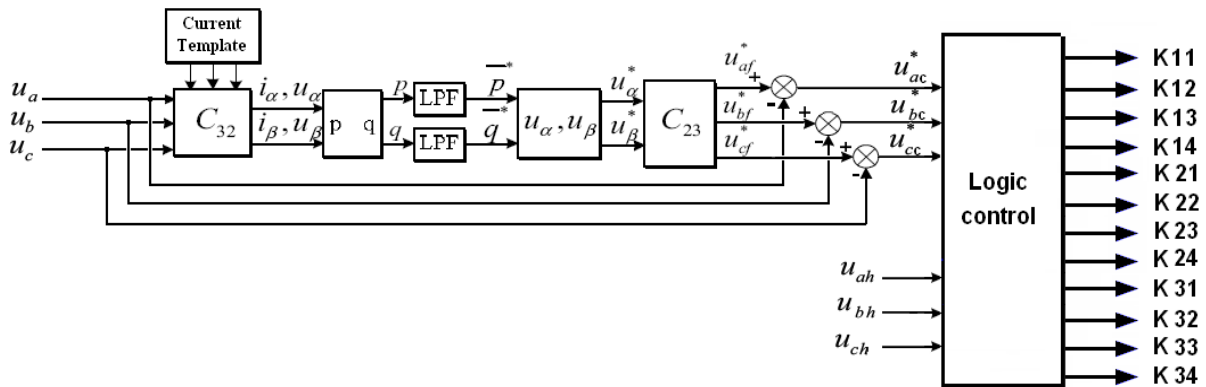


Fig. 6. Series active filter strategy control

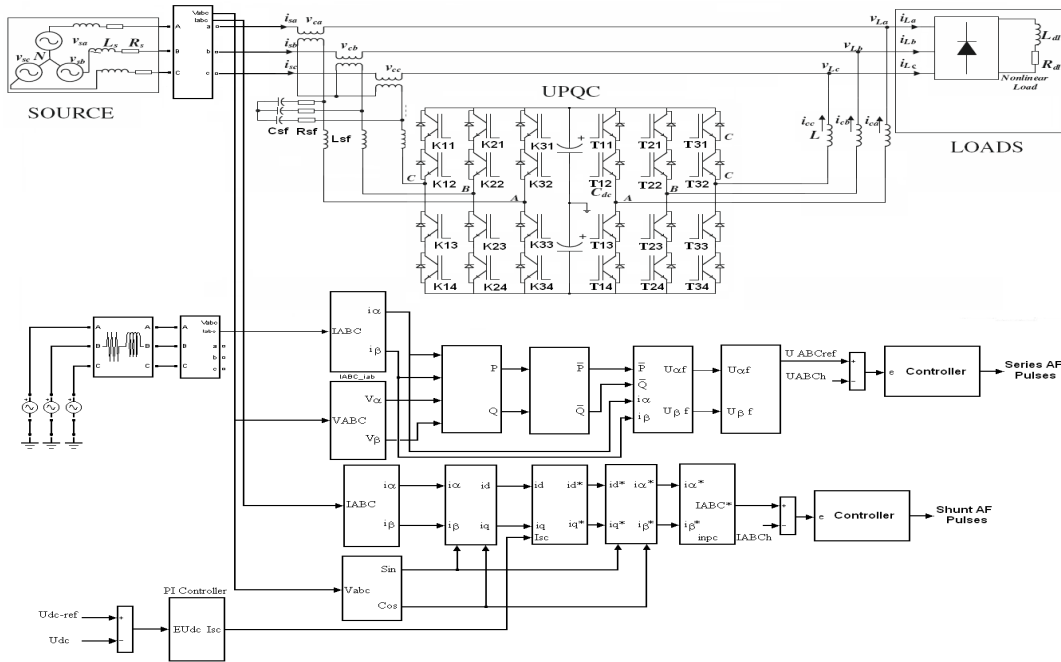
The three-phase fundamental voltages are given by:

$$\begin{bmatrix} U_{af} \\ U_{bf} \\ U_{cf} \end{bmatrix} = C_{23} \begin{bmatrix} u_{\alpha f} \\ u_{\beta f} \end{bmatrix} = \sqrt{2}U_1 \begin{bmatrix} \sin(\omega t + \theta_1) \\ \sin(\omega t + \theta_1 - \frac{2\pi}{3}) \\ \sin(\omega t + \theta_1 + \frac{2\pi}{3}) \end{bmatrix} \quad (31)$$

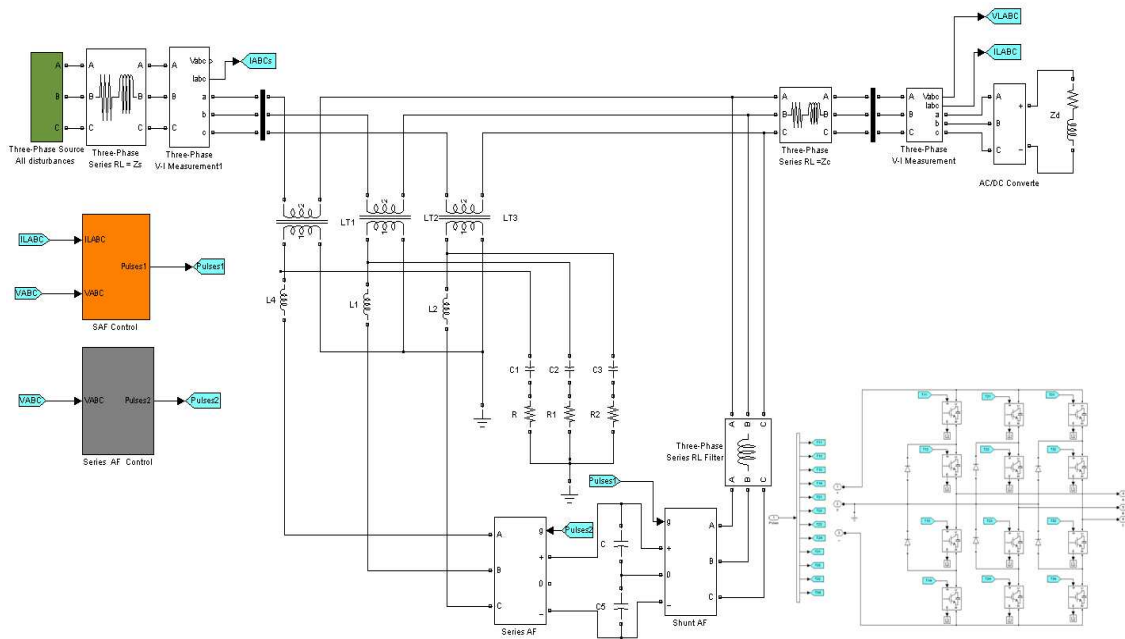
$$C_{23} = \begin{bmatrix} 1 & 0 \\ -1/2 & \frac{\sqrt{3}}{2} \\ -1/2 & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (32)$$

The block diagram of the series active filter control is shown in Fig. 6.

Where:



(a) UPQC block diagram



(b) MATLAB-Simulink Model

Fig. 7. UPQC system based on three-level (NPC) inverter

4. Simulation results and discussion

Fig. 7 shows the block diagram of the proposed UPQC, the simulation is performed using MATLAB-Simulink

software and SimPowerSystem Toolbox. The performances of UPQC are evaluated in terms of voltage and current harmonics mitigation, sags, swells and voltage unbalances compensation. The parameters of the proposed

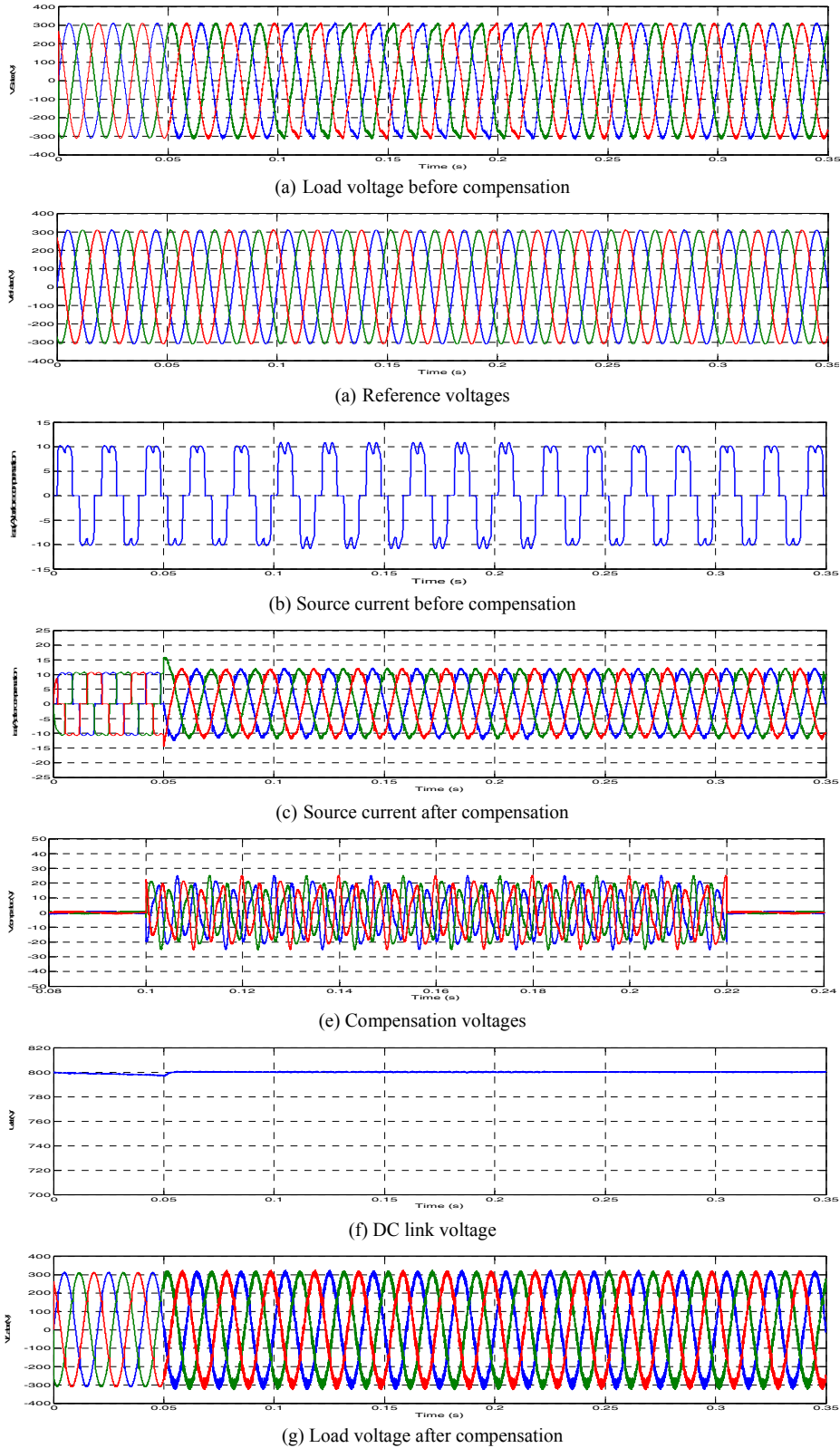


Fig. 8. UPQC performances for current and voltage harmonics compensation

UPQC are: $V_s=220V$, Frequency $F_s=50Hz$, Resistor $R_s=0.1m\Omega$, Inductance $L_s=0.0002mH$, Resistor $R_l=48.6\Omega$, Inductance $L_l=40mH$, $C_{dc}=3000\mu F$, Resistor $R_c=0.27m\Omega$, $L_c=0.8mH$.

4.1 Performances of UPQC for current and voltage harmonics compensation

To visualize the shunt APF and series APF performance individually, both APF's are put into operation at different instants. At time $t_1=0.05$ sec, shunt APF was put in operation first for compensating current harmonics. Before time $t_1=0.05$ sec the source current is highly distorted (THD=26.58%), after this instant it becomes sinusoidal (THD=5.51%) and in phase with utility voltage. The obtained results for current harmonics compensation are shown in Fig. 8.

At time $t_2=0.1$ sec, the series APF starts compensating voltage harmonics immediately by injecting out of phase harmonic voltage, making the load voltage at load

distortion free. The voltage injected by series APF and the dc voltage are shown in Fig. 6(e) and Fig. 6(f) respectively. In this case, the load voltage THDv(%) is improved from 46.93 % to 6.42 %. The harmonic spectrum of the source current and the load voltage before and after compensation are shown in Fig. 9.

4.2 Performances of UPQC for voltage sags compensation

To analyze the performance of UPQC during voltage sag conditions, the voltage source is assumed sinusoidal and no contains any harmonics. The simulation results are shown in Fig. 10. There are three instants; t_1 , t_2 and t_3 . At time $t_1=0.05$ sec, the shunt APF is put into the operation. A sag (25%) is introduced on the system at time $t_2=0.1$ sec, the series APF is put into the operation instantly. This sag lasted till time at $t_3=0.22$ sec, the system is again at normal working condition. During the voltage sag, the series APF is providing the required voltage by injecting in phase

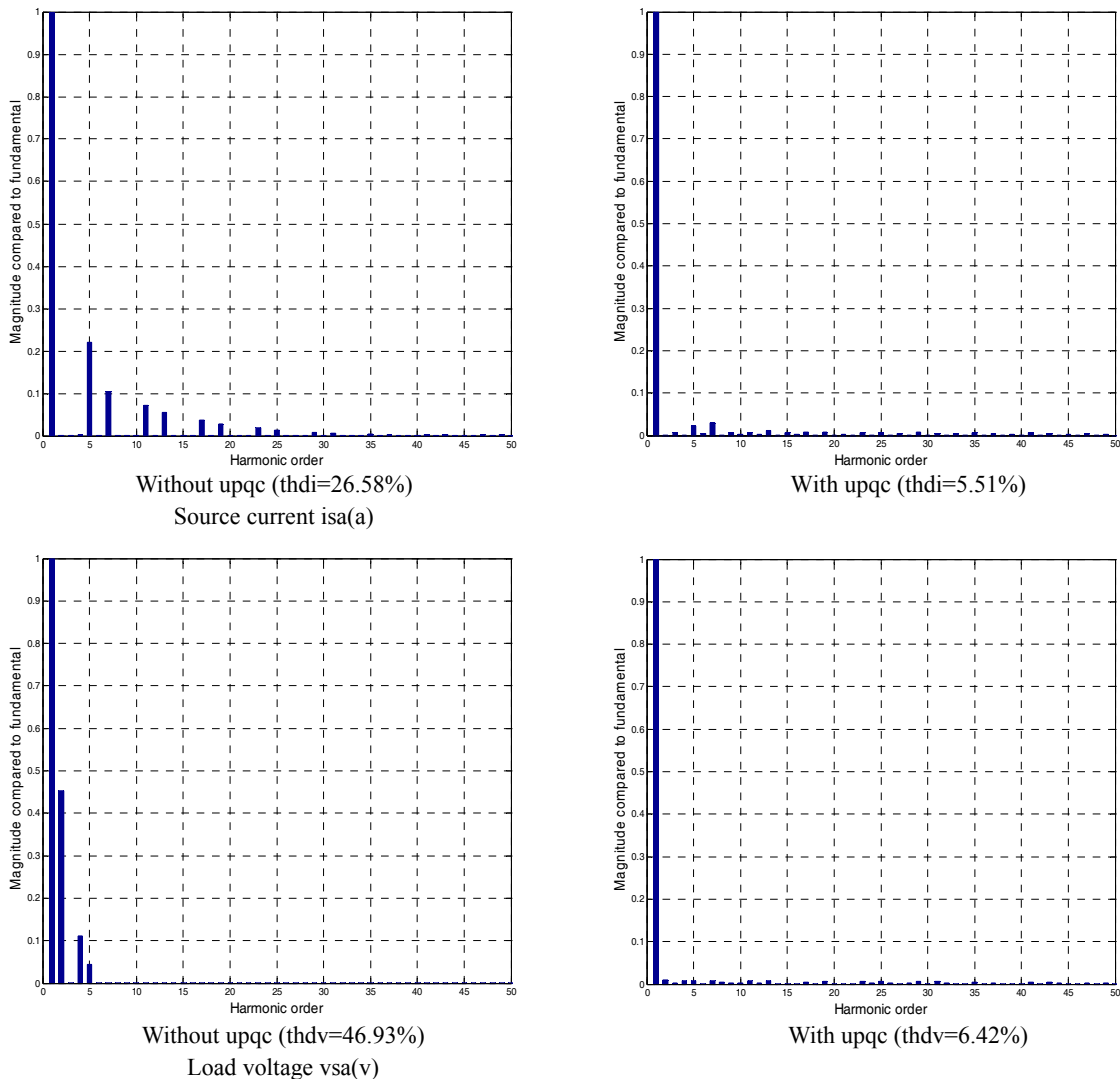


Fig. 9. source current and load voltage harmonic spectrum

compensating voltage (25%) equal to the difference between the reference load voltage and the real load voltage. During the sag voltage disturbance, it is shown that the source current is increased in Fig. 10(d), the UPQC maintain the load voltage at desired constant voltage in Fig. 10(g) and the dc voltage is maintained constant in Fig. 10(f).

4.3 Performances of UPQC for voltage swells compensation

Now a swell (35%) is introduced on the system during the time $t_1=0.1$ sec to $t_2=0.22$ sec, as shown in Fig. 11. Under this condition the series APF injects an out of phase compensating voltage (35%) in the line through series

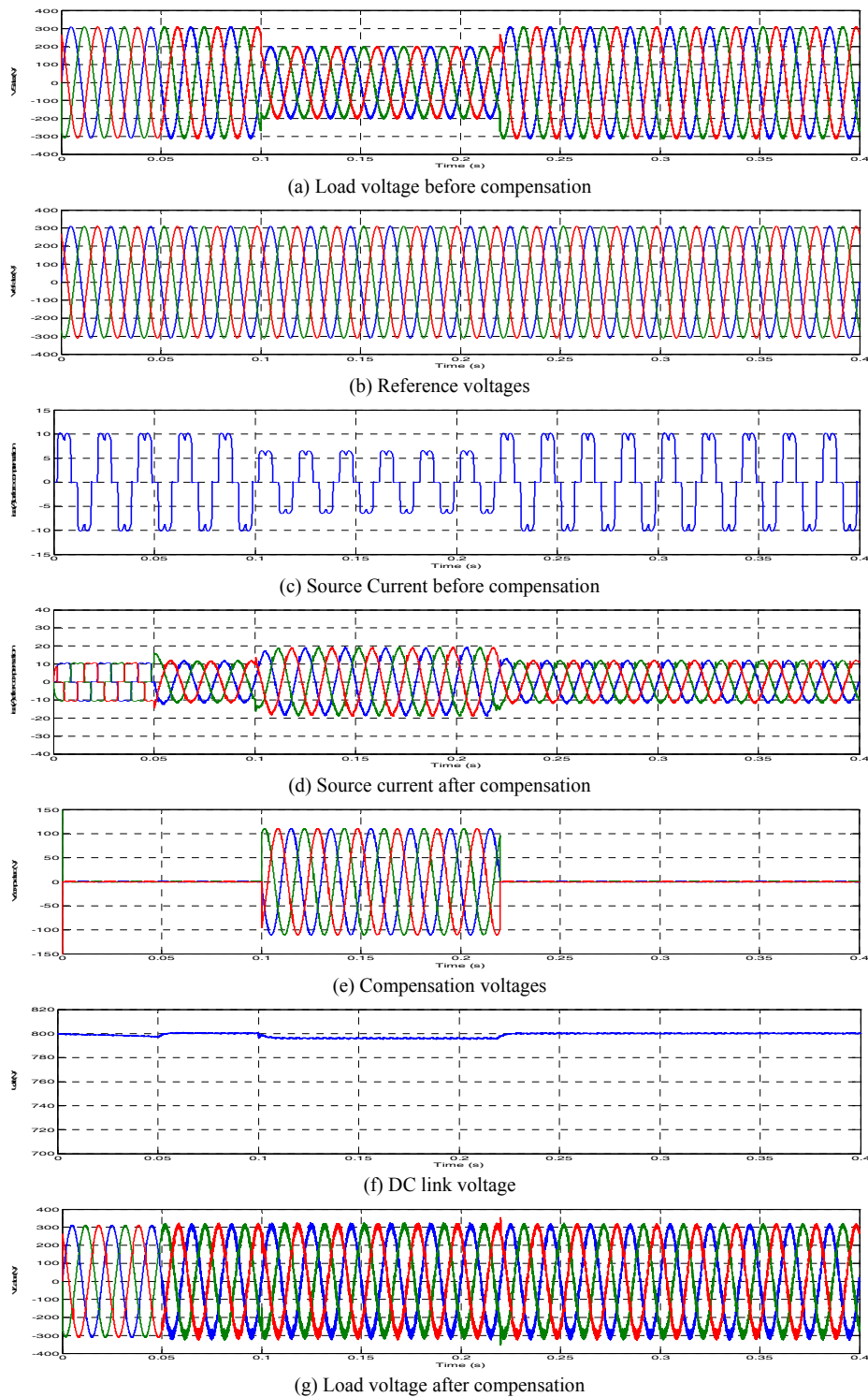


Fig. 10. UPQC performances for voltage sag compensation

transformers, equal to the difference between the reference load voltages.

The load voltage profile in the Fig. 11 (g) shows the UPQC is effectively maintaining the load bus voltage at desired constant level. The UPQC controller acts in such a way that source delivers the reduced current, as shown in

Fig. 11 (e). In other words the extra power due to the voltage swell condition is fed back to the source by taking reduced fundamental source current. The shunt APF maintains the dc link voltage at almost constant level, slightly increases due to the swell on the system as shown in Fig. 11 (f).

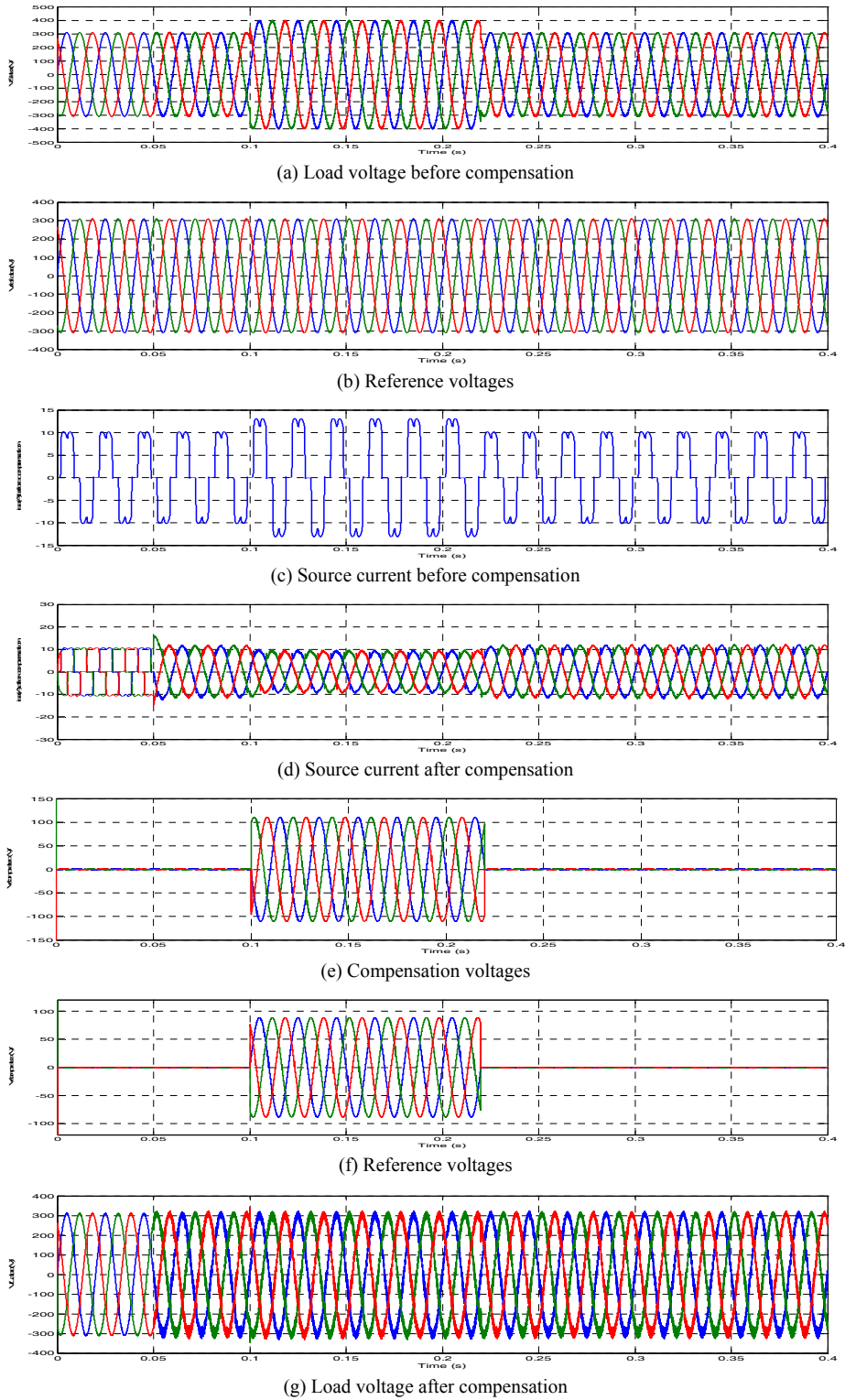


Fig. 11. UPQC performances for voltage swell compensation

4.4 Performances of UPQC for voltage unbalance compensation

An unbalance is now introduced on the system during the time $t_1=0.1$ sec to $t_2=0.22$ sec, as shown in fig. 12. in this case, the three-phase voltages sources not contain harmonic components; their expressions are given in (24):

$$\begin{aligned} v_{sa} &= 311 \sin(\omega t) + 31 \sin(\omega t) \\ v_{sb} &= 311 \sin(\omega t + \frac{4\pi}{3}) + 31 \sin(\omega t + \frac{2\pi}{3}) \\ v_{sc} &= 311 \sin(\omega t + \frac{2\pi}{3}) + 31 \sin(\omega t + \frac{4\pi}{3}) \end{aligned} \quad (24)$$

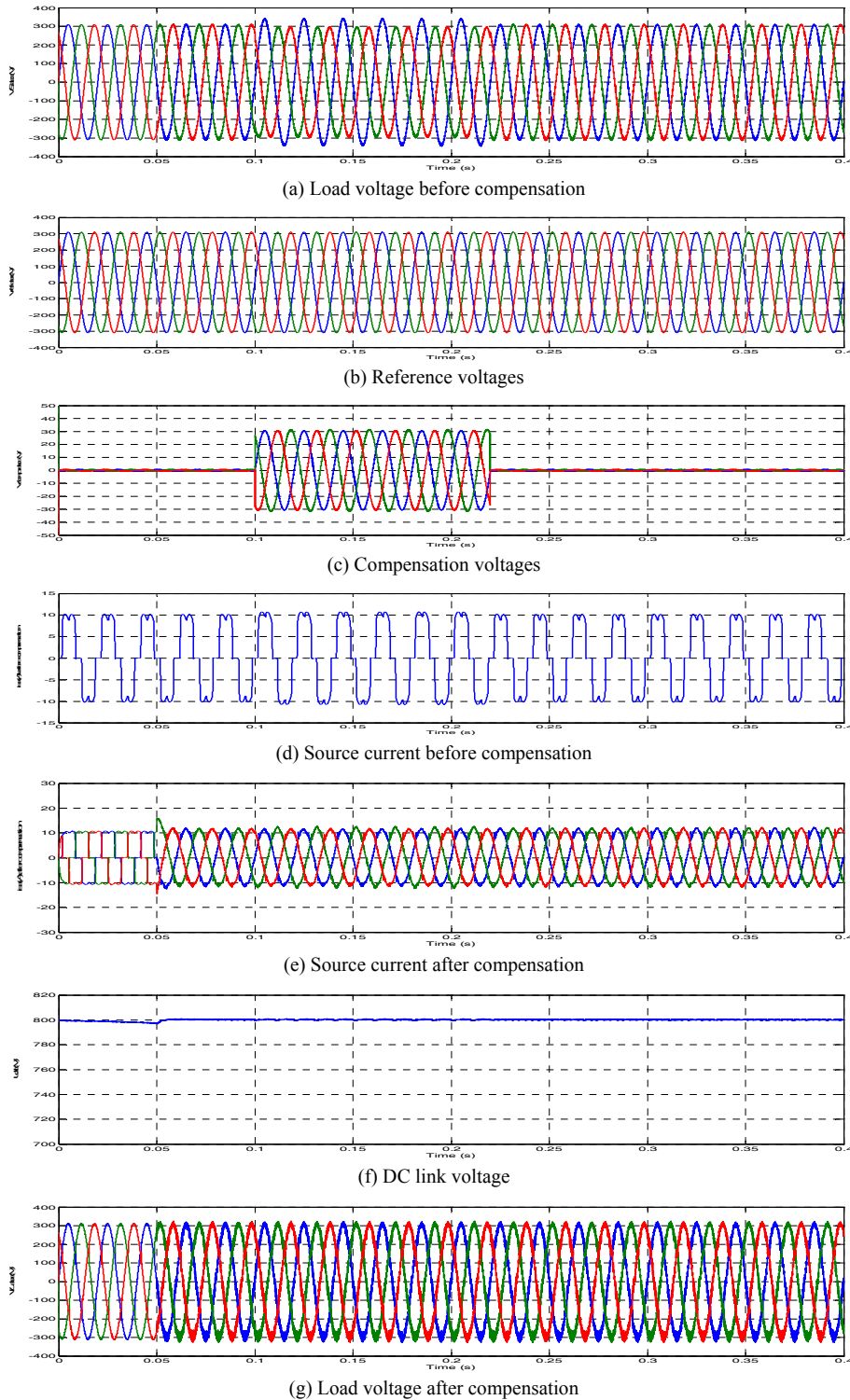


Fig. 12. UPQC performances for voltage unbalance compensation

4.5 Performances of UPQC for all voltage disturbances compensation

The performance of proposed UPQC is also tested under all voltage disturbances simultaneously. The simulation results are shown in Fig. 13. The voltage sags (25%) is introduced voluntarily between $t_1=0.06$ sec and $t_2=0.12$ sec. After that, a voltage swells (35%) is introduced between

$t_2=0.12$ and $t_3=0.18$ sec. The voltage harmonics is introduced between $t_3=0.18$ sec and $t_4=0.24$ sec. The unbalances is introduced between $t_4=0.24$ sec and $t_5=0.3$ sec. After $t_5=0.3$ sec the system is again at normal working condition. It is illustrated that the proposed UPQC is capable to mitigate all voltage disturbances and does not show any significant effect of disturbance type present in the utility voltages on its compensation capability.

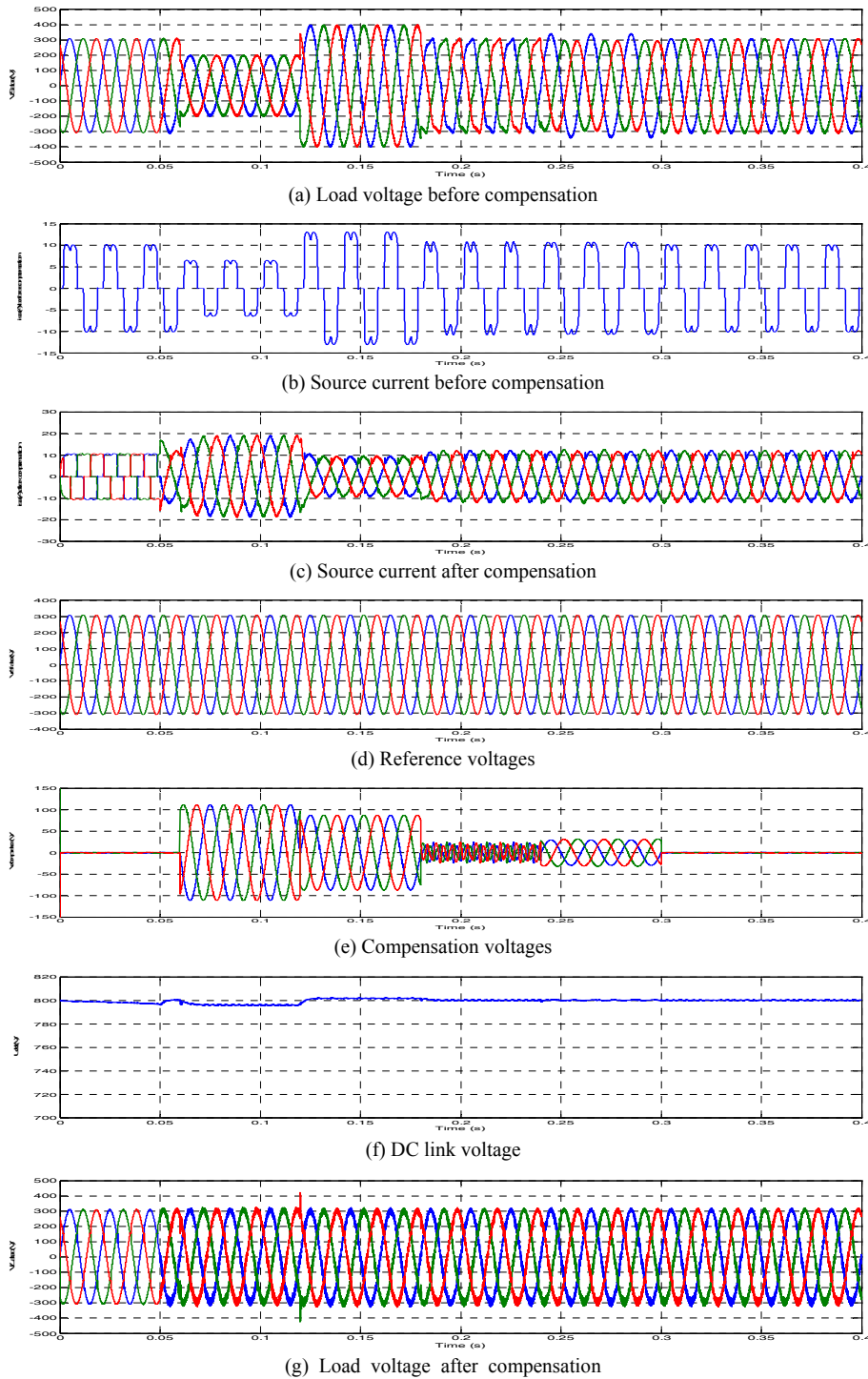


Fig. 13. UPQC performances for all voltage disturbances compensation

4.6 Dynamic performances of UPQC for the sudden change of load

In order to evaluate the performance of the proposed UPQC during transient condition, the load on the system is changed suddenly. The simulation results during this condition are shown in the Fig. 14. Before time $t_1=0.05$ sec, the shunt and series APFs are not working, the source current is highly distorted. After $t_1=0.05$ sec the shunt active filter is only on operation (the source current after compensation is nearly sinusoidal and in phase with the source voltage). The source voltage disturbances: sag, swell, unbalance and harmonic voltages are introduced between $t_2=0.16$ sec and $t_3=0.4$ sec, are effectively improved using the proposed UPQC. When the sudden load current disturbance is introduced voluntarily between $t_4=0.25$ sec and $t_5=0.35$ sec, the UPQC controller acts immediately without any delay, the shunt APF injects a current equals to sum of harmonic. In all the dynamic condition the dc voltage is maintained constant and equal

to the reference value $U_{dc-ref} = 800$ V using proportional integral voltage controller. It is observed that the dc voltage passes through a transitional period of 0.02 sec before stabilization and reaches its reference with moderate peak voltage approximately equal to 5 V. Before Shunt AF application the source current is distorted with poor power factor, after compensation the source current shown in Fig. 14(f) is sinusoidal and in phase with the source voltage for the all voltage disturbances. The effectiveness of the UPQC in reducing the supply current and load voltage harmonics for all disturbances conditions is proved.

The proposed control scheme for UPQC has been validated through simulation results using MATLAB-Simulink software and SimPowerSystem toolbox. Through visualization (Figs. 8, 10, 11, 12, 13 and 14), we are able to conclude that the operation of the proposed unified power quality energy based on three-level (NPC) inverters is successful. Before the application of shunt active power filter, the source current is equal to non-linear load current; highly distorted and rich in harmonic. After compensation,

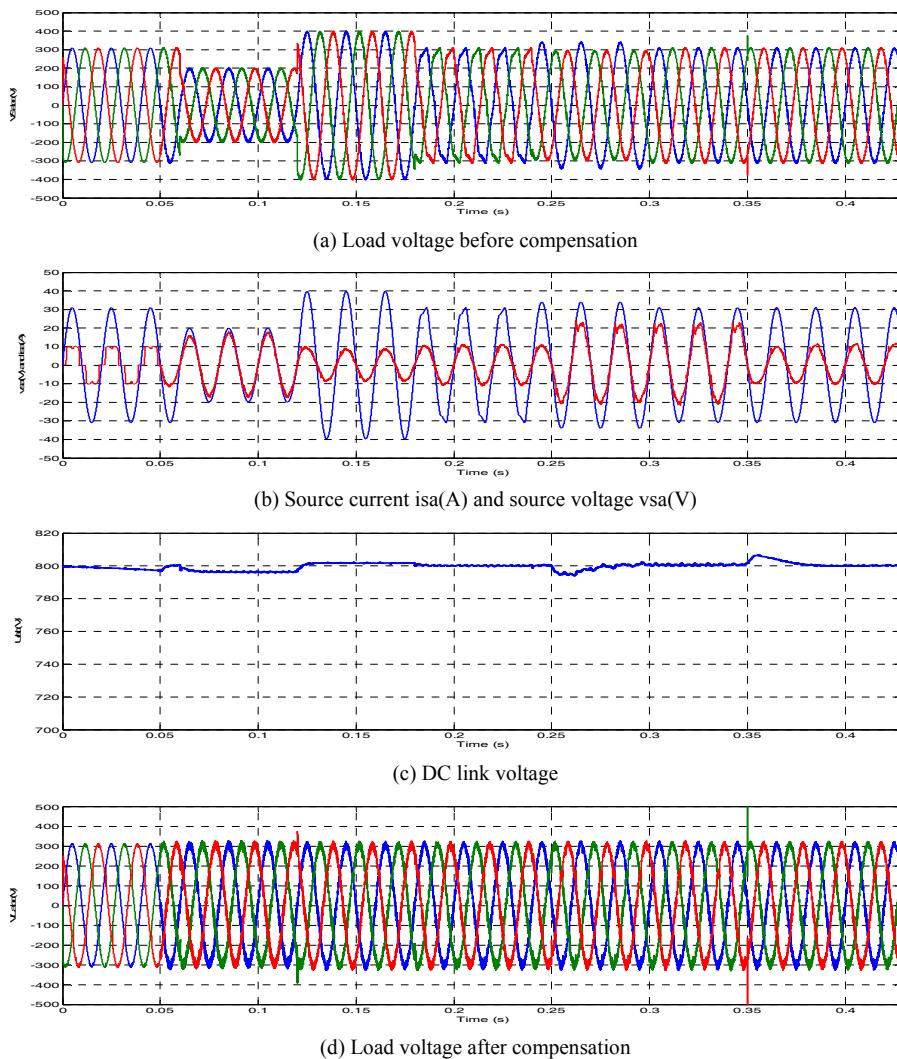


Fig. 14. UPQC: dynamic performances for sudden load change between $t=0.25$ sec and $t=0.35$ sec

the THD is considerably reduced from 26.58% to 5.51%, the load voltage is instantly improved using the proposed UPQC for separate or simultaneously voltage disturbances such as sags, swells, unbalances and harmonics. The dc voltage is maintained at a constant value which is equal to the reference value $U_{dc-ref} = 800$ V by using PI voltage controller. Fig. 14 (c) illustrate the dynamic response of the control loop. It is observed that the dc voltage pass through a transitional period of 0.02 s before stabilization and reaches its reference $U_{dc-ref} = 800$ V with moderate peak voltage approximately equal to 5 V when a step change in load current is introduced between $t_1 = 0.25$ sec and $t_2 = 0.35$ sec. The effectiveness of the proposed UPQC has been demonstrated in maintaining the three-phase load voltages balanced and sinusoidal, moreover the proposed system does not show any significant effect of disturbance type present in the utility voltages on its compensation capability and the load voltage under all voltage is maintained constant, balanced and sinusoidal.

5. Conclusion

To enhance the power quality by reducing the source current harmonics and improve the voltage delivered to sensible and critical loads, a new UPQC configuration based on three-level (NPC) inverter topology has been proposed in this paper. The control strategy adopted is based on the instantaneous power method for the series AF and synchronous reference frame detection method for the shunt AF. The developed model is validating through simulation results using Matlab-Simulink software and SimPowerSystem toolbox. The control algorithm of UPQC has been observed to be satisfactory for various power quality improvements like voltage harmonics mitigation, current harmonic mitigation, voltage sag, swell and unbalance compensation. The source current THDi is improved from 26.58 % to 5.51 %, while the load voltage THDv is improved from 46.93 % to 6.42 %. The UPQC performance during transient conditions has been found satisfactory, the UPQC controller acts immediately without any delay in the operation with fast dynamic response. The result of this study may be useful for potential applications of UPQC under wide practical situations. The performance of UPQC can be further improved by using intelligent controllers.

List of symbols

V_{sabc} :	Source voltages
i_{sabc} :	Source currents
V:	Peak value of phase voltage
$i_{\alpha-\beta}$:	Currents in(α - β) reference frame
$i_{\alpha-ref}$, $i_{\beta-ref}$:	Reference currents in(α - β) reference frame

id-iq:	Currents in(d-q) frame
Icomp-abc:	Shunt AF compensation currents
$U_{\alpha-\beta}$:	voltages in(α - β) reference frame
$U_{af-U\beta f}$:	Fundamental voltages in (α - β) frame
Uf-abc:	Series inject voltage
Udc:	DC link voltage of UPQC system
PQ:	Active and reactive power
C32:	Concordia transformation
C23:	Inverse Concordia transformation
Shunt AF	Shunt Active Filter
Series AF	Series Active Filter
UPQC	Unified Power Quality Conditioner

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