

# High-Efficiency Heterojunction with Intrinsic Thin-Layer Solar Cells: A Review

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**ABSTRACT:** Heterojunction with Intrinsic Thin-layer (HIT) solar cells are currently an important subject in industrial trends for thinner solar cell wafers due to the low-temperature of production processes, which is around 200°C, and due to their high-efficiency of 24.7%, as reported by the Panasonic (Sanyo) group. The use of thinner wafers and the enhancement of cell performance with fabrication at low temperature have been special interests of the researchers. The fundamental understanding of the band bending structures, choice of materials, fabrication process, and nano-scale characterization methods to provide necessary understanding of the interface passivation mechanisms, emitter properties, and requirements for transparent oxide conductive layers is presented in this review. This information should be used for the performance characterization of the developing technologies for HIT solar cells.

**Key words:** Heterojunction, Photovoltaics, High efficiency, c-Si interface, Solar cells

## Nomenclature

a-Si:H/c-Si : hydrogenated amorphous silicon/crystalline silicon

HJ : heterojunction

HIT: Heterojunction with Intrinsic Thin-layer

a-Si:H(i): intrinsic hydrogenated amorphous silicon

BSF: back surface field

$V_{oc}$ : open-circuit voltage

$J_{sc}$ : short-circuit current density

FF: fill factor

$\eta$ : efficiency

J-V: current density-Voltage

TCO: transparent conductive oxide

ATR: attenuated total reflection

MTCE: multi-tunnelling capture-emission

PECVD: plasma enhanced chemical vapour deposition

VHF-PECVD: very high frequency PECVD

HWCVD: hot wire CVD

SKKU: Sungkyunkwan University

ITO: indium tin oxide

IO:H: hydrogenated doped indium oxide

ZnO:Al: aluminium doped zinc oxide

$V_D$ : built-in potentials

$\Phi$ : work function

$D_{it}$ : defect states at the a-Si:H/c-Si interface

$N_{DB}$ : defect states in the a-Si:H bulk

SE: spectroscopic ellipsometry

SHG: second-harmonic generation

XPS: X-ray photospectroscopy

UPS: ultra-violet photospectroscopy

UV-PYS: ultraviolet-excited photoelectron yield photospectroscopy

TEM: transmission electron microscopy

SIMS: secondary ion mass spectroscopy

QSSPC: quasi-steady-state photoconductance

$\mu$ c-Si:H: hydrogenated microcrystalline silicon

a-SiO<sub>x</sub>:H: hydrogenated amorphous silicon oxide

SiN<sub>x</sub>: silicon nitride

ICDL: Information and Communication Device-Lab

AIST: The National institute of Advanced Industrial Science and Technology

HZB: Helmholtz Zentrum Berlin

EPFL: École Polytechnique Fédérale de Lausanne

NREL: National Research Energy Laboratory

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## Subscripts

ITO: indium tin oxide

oc: open-circuit

sc: short-circuit

it: interface states

DB: defect states in a-Si:H bulk

## 1. Introduction

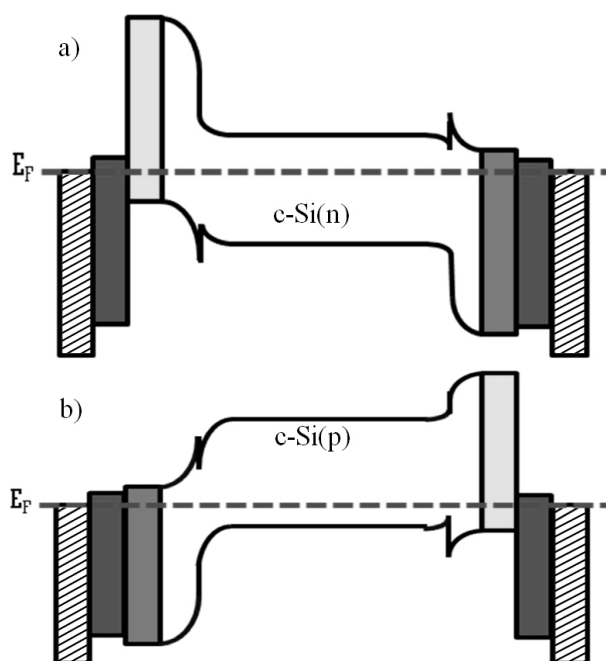
Wafer bowing and breakage caused by high-temperature metal back contact is a great concern due to the current industry trend toward thinner solar cell wafers. The a-Si:H/c-Si HJ solar cell is a good solution to these problems due to the low-temperature of the production process, which is around 200°C. This also limits the thermal budget and allows for inexpensive, lower-quality materials to be used as base materials. A considerable number of studies have been made on the a-Si:H/c-Si heterojunction solar cells in recent years<sup>1-8</sup>. Panasonic's (Sanyo) HIT solar cells hold the word record efficiency of 24.7% based on n-type c-Si wafers, in which stacks of a-Si:H(i) and doped a-Si:H layers help form both the emitter and the BSF<sup>1</sup>. The a-Si:H(i) layer enables very high  $V_{oc}$  due to its excellent passivating properties. Hence, this incorporation of the a-Si:H(i) layer at the hetero-interface has been confirmed to improve solar cell  $\eta$ <sup>2</sup>.

The first investigation of the HJ silicon solar cells, in which an amorphous silicon emitter is deposited on a crystalline substrate, was reported by Fuhs *et al.* in 1974<sup>9</sup>. Then, in 1985, the HJ solar cell was fabricated with SiO<sub>2</sub> depositing on both sides of p-type c-Si substrates by Yablonovitch *et al.*<sup>10</sup>. For maximal performance, Yablonovitch stated that solar cells should resemble semiconductor lasers, i.e., in that they should be constructed in the form of a double HJ. In this configuration, a narrow-band-gap active layer such as a c-Si absorber layer is sandwiched between two wide band-gap layers of opposite doping, which act as a "carrier mirror". Hence, the less recombination at the contact could be achieved. Moreover, it was also stated that in order to achieve high  $V_{oc}$ , the use of higher-quality wafer and lower surface recombination are other key issues<sup>10</sup>. The technical base on a-Si:H/c-Si HJ as an alternative to traditional diffused emitters have been investigated by many research groups using both n- and p-type absorber layers<sup>1,8,12-13</sup>. The mass production of this type of cell was also established as

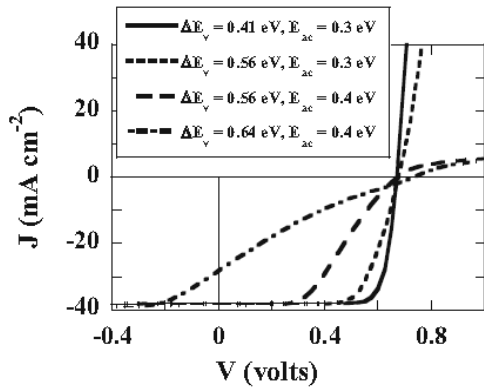
well<sup>14</sup>. A review on the cell fabrication process and cell performance of the a-Si:H/c-Si HJ solar cell has been published by Q. Wang<sup>15</sup>. Instead of focusing on these issues, this review focuses on the physical characteristics, such as the band diagram, carrier transport, and device characterization in order to highlight the key issues in a-Si:H/c-Si HJ solar cells. The recent leading performance of the HIT solar cells fabricated at various companies and institutes all over the world are also reported.

## 2. The construction of the a-Si:H/c-Si HJ band diagram

An energy band diagram of a double-side a-Si:H/c-Si HJ solar cells is shown in Fig. 1. In this figure, the value of the band gap for p-type, n-type, and i-type a-Si:H is assumed to be the same (with a negligible number of states). Since the vacuum level is parallel everywhere to the band edges and is continuous<sup>16</sup>. As a result, the electron affinities and band gap define the band discontinuities at the interface. The band discontinuities at the interface are also called the "band offset". The band offset (valence and conduction) appears at both the front and back side of the HJ. The band offset plays a significant role in the carrier transport in the heterojunction solar cells. At the front side, with



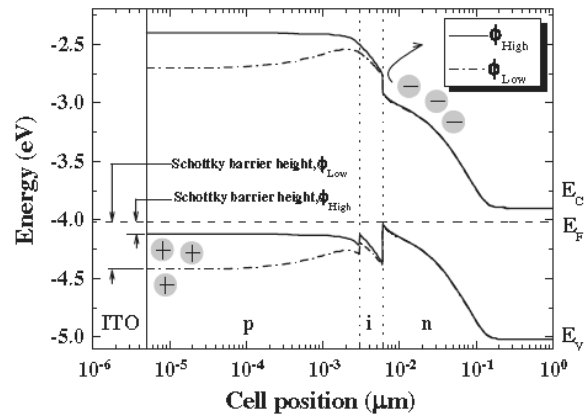
**Fig. 1.** Schematic band diagram of HIT solar cells based on (a) c-Si(n) and (b) c-Si(p) substrates. An indication of the metal contact, ITO, a-Si:H(p), and a-Si:H(n), respectively is given in the band diagram



**Fig. 2.** Variation of the illumination J-V characteristics for different valence band discontinuities and activation energies of the emitter in c-Si(n) double HIT solar cells<sup>6)</sup>

an increasing band offset, the Fermi level position at the HJ shifts towards the valence band (conduction band) edge of c-Si (n/p), this reduces the interface recombination efficiency<sup>17)</sup>. Simultaneously, the built-in potential is also enhanced when the barrier in the band offset becomes larger. This enhances  $V_{oc}$ , thus yielding higher conversion efficiency. However, when the band offset exceeded the value of 0.56 eV, the deformation of J-V characteristics was observed due to free-hole accumulations at the interface<sup>18)</sup>, as shown in Fig. 2. This leads to a deep depletion at the interface. Hence, the hole current is nearly suppressed, eventually resulting in a lower  $J_{sc}$  and low FF. The preferred value of the band offset is around of 0.54 eV, which can be controlled by the energy band gap of the emitter as well as the a-Si:H(i) layer<sup>6,18)</sup>. At the back side, the value of the band offset and behaviour of the carrier transport depend on the doping type of the base wafers. For example, for an n-type substrate, the large valence band offset and thicker a-Si:H(i) layer provide a back surface “mirror” for holes. This a-Si:H(i/n) stack does not affect electron transport much because the offset in the conduction band edges is small<sup>4)</sup>. In contrast, the small conduction band offset provides a much less effective mirror for the minority carrier electrons. Additionally, the larger offset in the valence band edges prevent hole collection, resulting in the accumulation of holes on the back side of the c-Si surface and a consequent reduction in the FF and conversion efficiency<sup>4)</sup>.

The  $\phi_{TCO}$  is also another key issue to take into account in device design, because it can be influence the total built-in potential of the device. Without regard to the doping type of the substrate, if the ITO work function is not appropriate, the built-in potentials ( $V_D$ ) of TCO/a-Si:H contact and a-Si:H/c-Si junction will have opposite directions to each other. With an



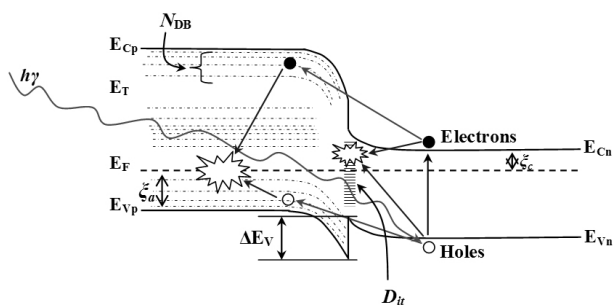
**Fig. 3.** Band diagram of the ITO/a-Si:H(p)/ a-Si:H(i)/c-Si(n) structure with low and high  $\phi_{TCO}$ <sup>23)</sup>

n-type c-Si substrate, for instance, ITO with higher  $\phi$  is preferable, because it determines a higher built-in voltage and therefore higher  $V_{oc}$  and  $\eta$ . ITO with lower  $\phi$  not only determines a lower built-in voltage, but can also induce the formation of an inverted Schottky junction at the interface of the ITO/emitter, which can reduce or even cancel out the device performance<sup>19)</sup>, as shown in Fig. 3. We can apply this understanding of the effects of  $\phi_{TCO}$  to p-type c-Si substrate. In order to obtain a high-efficiency HIT device,  $\phi_{TCO}$  should at least be lower than 4.5 eV or higher than 5.1 eV for p- or n-type c-Si substrates, respectively. A  $\phi_{TCO}$  value of 5.1 eV can be obtained in practice, which may be one reason for Sanyo achieving the world record efficiency of 24.7% on n-type silicon substrate<sup>20-22)</sup>.

### 3. Material choice for c-Si surface passivation and carrier transport in a-Si/c-Si HJ solar cells

#### 3.1 Material choice for c-Si surface passivation

Due to the largest disturbance to the symmetry of the crystal lattice, non-saturated or dangling bonds are formed at the surface. Additional process-related extrinsic surface defects may arise from dislocation or chemical residues and metallic deposition on the surface. Those defects become recombination centers for photogenerated carriers. Thus, surface recombination losses at the c-Si surface will be at tolerable levels if they are well passivated. A low surface recombination of less than 10 cm/s has been achieved in different ways by the use of a dielectric layer such as SiO<sub>2</sub>, SiN<sub>x</sub> or a-Si:H<sup>7,24-26)</sup>. However, a-Si:H is the best choice for a-Si:H/c-Si heterojunctions due to



**Fig. 4.** Schematic band diagram of a-Si:H(p)/ a-Si:H(i)/c-Si(n) HJ including defect states at the a-Si:H/c-Si interface,  $D_{it}$  and the a-Si:H bulk-defect,  $N_{DB}$

its lesser restriction of the carrier transport. A thin layer of high-band-gap material such  $\text{SiO}_2$  or  $\text{SiN}_x$  in place of the a-Si:H layer results in barrier potential and then blocking of the carrier transport, causing an S-shape in the J-V characteristics. By restricting the band gap of  $\text{SiO}_2$  to less than 2 eV, HJ solar cells can succeed in preventing the S-shape in the J-V curve<sup>27)</sup>.

Thus, if the passivation by a-Si:H(i) is good enough and the band offset is suitable, the photogenerated charge carriers in the c-Si absorber can be separated, resulting in less surface recombination and high  $V_{oc}$ . The carriers which survive from the surface recombination process then become the victim of the localized states in the emitter layer and the states in the vicinity of the emitter/buffer layer interface, as shown in Fig. 4. The higher conductivity resulting in the shift of the Fermi level to near the band edge (valence or conduction) leads to enhancement of  $V_{oc}$ . However, the higher doped layers own to larger mid-gap defects than undoped ones. The mid-gap defects are the major source for the absorption of light as well as photogenerated carrier recombination. Hence, the trade-off condition for an emitter layer with lower mid-gap defects and higher conductivity are also important factors for higher HIT cell performance.

### 3.2 Carrier transport in the a-Si/c-Si HJ solar cells

Carrier transport in the a-Si:H/c-Si HJ can be unique and different from the conventional p-n solar cell because the Fermi level can be varied by doping. The MTCE model was first suggested by Matsuura *et al.* to explain the dark forward J-V characteristics of a thick ( $\sim 1 \mu\text{m}$ ) a-Si:H(i)/c-Si(p) HJ<sup>28)</sup>. In concurrence with Matsuura *et al.*, Mimura and Hatanaka confirmed that MTCE dominated in their HJ, which is an undoped thick a-Si:H ( $\sim 1 \mu\text{m}$ ), or slightly B-doped a-Si:H grown on n-type c-Si<sup>29)</sup>. Rubinelli *et al.* supported Matsuura's multitunnelling model in their theoretical evaluation of the a-Si:H(n)/c-Si(p) HJ<sup>30)</sup>.

However, in their investigation at higher voltage ( $V > 0.6 \text{ V}$ ) the other model, which is the diffusion current, is suggested. Two decades after the first HIT cell was made, the first investigation of the mechanisms of carrier transport in HIT solar cells was reported by Taguchi *et al.* They stated that the diffusion model determined the carrier transport properties of their solar cell device in the high-forward-bias region ( $0.4 < V < 0.8 \text{ V}$ ), whereas the multistep tunnelling model determined the current transport in the low-bias region ( $0.1 < V < 0.4 \text{ V}$ )<sup>31)</sup>. Based on the HIT structure, T. F. Schulze *et al.* suggested that the transport mechanism is dependent on the substrate doping type. The most relevant microscopic parameter "the interface passivation quality" mainly impacts the high-forward-bias current, thus determining  $V_{oc}$ . In the low-forward-bias range, while the n-type c-Si based samples exhibit a current dominated by recombination in the space charge region, the p-type c-Si based samples reveal a dominating temperature-independent tunnelling contribution<sup>32)</sup>. Recently, Dao *et al.* revealed that in the low-forward-bias region, a HJ solar cell fabricated on n-type c-Si is dominated by the MTCE mechanism. The diffusion-recombination current is denominated the in high-forward-bias region<sup>7)</sup>. Consequently, the conduction mechanisms in the forward-bias range of the HJ with intrinsic thin layer solar cells have been ambiguous.

## 4. The a-Si/c-Si heterojunction solar cell process

From left to right, in Fig. 1, the most commonly symmetrical HIT solar cell includes a metal grid, transparent conducting oxide (TCO such as ITO,  $\text{ZnO:Al}$ ,  $\text{IO:H}$ ), emitter layer (a-Si:H (p- or n-type)), passivated-layer (a-Si:H(i), a-SiO<sub>x</sub>:H(i)), bulk absorber layer (n or p-type c-Si), passivated-layer (a-Si:H(i), a-SiO<sub>x</sub>:H(i)), BSF layer (a-Si:H(n- or p-type)), TCO, and finally the back metal contact. Photolithography or patterned physical masks could be used for defining an area and front grid formation with approximately 5% area coverage. Commonly, an evaporated multi-layer stack of Ag/Al is used for the top metal contact. A multi-layer stack of Ti/Pd/Ag can also be used. In this stack, Pd is used to prevent Ag from diffusing in or out. Al or Ag/Al, or a stack of Ti/Pd/Ag/Pd is used for bottom contact formation. The screen-printing of silver-paste as fingers for the front electrode and the entire rear surface for the back contact for larger-area cells was applied for industrial cells.

In order to enhance the light trapping, the substrate surface is

textured. By appropriate selective etching microscopic pyramids are created. Mono-Si is available with various surface directions, e. g. the (110), (111), and (100) directions. The removal rate for alkaline etches such as KOH or NaOH is different for different crystal planes. Under appropriate conditions small pyramids can be produced based on this effect.

Before depositing any layer on the c-Si surface, it must be cleaned from organic and inorganic impurities from saw damage and surface impurities. A process using acetone/methanol, DIW rinse, RCA1, DIW rinse, RCA2, and then HF dipping has been well established. A final cleaning with 1-5% HF was applied to the c-Si wafer before loading it into the chamber for cell fabrication.

After wafer cleaning, the wafer was loaded immediately into the chamber. The intrinsic passivated layer and emitter layer are deposited in sequence for front-side fabrication. Turning back the wafers, the intrinsic passivated and back-surface fields are then deposited for back-side formation. The optimized deposition conditions of the intrinsic passivated layer depend on the deposition technique and wafer surface. However, we have to ensure that there is no epitaxial or microcrystalline growth on the c-Si surface. Moreover, a film with fewer voids, and higher hydrogen content is more attractive<sup>7)</sup>. For doped layer deposition condition, a large conductivity and higher thickness in an emitter layer are accompanied by larger light absorption in the blue and near-infrared regions and a middle-band gap defect. Therefore, the trade-off conditions for the emitter layer are sought effective application to solar cell fabrication<sup>33)</sup>.

For all a-Si:H deposition, the most common deposition technique is PECVD<sup>8)</sup>. The VHF-PECVD technique has also appeared as an interesting alternative for conventional PECVD methods. This allows for higher deposition rates and it is less aggressive than the conventional PECVD technique. VHF-PECVD was also achieved by a group at SKKU<sup>34)</sup>. Another technique, HWCVD, also showed suitable a-Si:H layer deposition due to its higher deposition rates and being less aggressive than conventional PECVD<sup>13)</sup>.

Current collection just by the front grid would lead to high losses. The amorphous emitter layer exhibits a low lateral conductance due to the small conductivity and small thickness (~ 7 – 15 nm). Hence, a transparent conductive oxide layer is introduced between the emitter and the metal contact. Achieving the lowest possible electrical resistivity with the optimized highest transparency in the visible range is a requirement for the

unique properties of the TCO layer. ITO is one of the most used materials for TCO contact due to its high band gap of 3.75 eV and low resistivity of  $\sim 10^{-4} \Omega\cdot\text{cm}$ . Magnetron sputtering with a ceramic target is a common method for ITO deposition, in which Ar feed gas and substrate heating to  $\sim 200^\circ\text{C}$  are used during deposition<sup>35)</sup>. ZnO:Al is also another choice for the anti-reflection layer in HJ solar cells. Recently, IO:H has shown some advantages over conventional ITO due to its high conductivity, low carrier concentration and high mobility. The current density of IO:H can be enhanced in a device due to low free-carrier absorption<sup>36)</sup>. For all kinds of TCO, the thickness is fixed approximately 80 nm respect to refractive index of 1.8 at 550 nm of wavelength.

## 5. Characterization methods

An effective a-Si:H/c-Si interface that allows for the efficient transport of charge carriers with minimal recombination loss is a prerequisite for high-performance HJ solar cells, in which a thin a-Si:H(i) layer is generally interposed between the base wafer and heavily doped emitter. Purely hydrogenated intrinsic amorphous silicon, highest hydrogen content, and lowest void fraction are designed properties for the passivated c-Si wafer. The passivation of a silicon surface can be achieved in two ways: by field-effect passivation or by the neutralization of defects of interface states. Infrared absorption techniques, such as ATR can provide information on  $\text{SiH}_n$  ( $n = 1-3$ ) local structures with sensitivity. The higher Si-H bond is utilized for the neutralization of interface defects, whereas a-Si:H(i) contains an Si-H<sub>2</sub>-rich interface, resulting in porous structures and poor surface passivation<sup>37-38)</sup>. Using *in-situ* SE or SHG techniques, the formation of both amorphous silicon and epitaxial films on c-Si can be investigated from a very early stage of film growth. The growing of an epitaxial layer as well as void formation at the interface could be suppress the passivated quality of the films<sup>39)</sup>. The formation of Si thin films has also been studied using *ex-situ* techniques such as TEM and SIMS, which provide detailed information on film structures and composition, but cost, time effectiveness, and sample destruction are known issues. Other *ex-situ* techniques that are non-destructive could be XPS, UPS, and UV-PYS. The recombination rate could be evaluated through the density of band gap states in the a-Si:H layer. The higher density of band gap states results in higher recombination at the a-Si:H/c-Si interface due to the photogenerated carriers

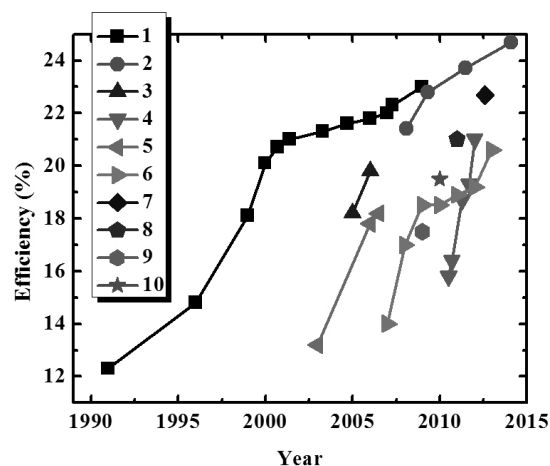
becoming the victim of the localized states within the band gap<sup>8,40</sup>. Finally, the QSSPC technique is an *ex-situ* technique, but it provides a direct and clear value of abruptness of the a-Si:H/c-Si interface. Hence, this method is used as a reference for the evaluation of other techniques.

Accompanying the a-Si:H layer, TCO and the TCO/emitter interface are other key issues for achieving high-efficiency HIT solar cells. The formation of Si-O bonds on the ITO/a-Si:H interface during the initial stages of ITO growth results in the appearance of a thin SiO<sub>x</sub> layer in this region. This can act as a barrier for the carrier transport at the front contact. Moreover, high-energy sputtered atoms, such as In and Sn can penetrate in to the a-Si or Si bulk layer. This leads to the formation of complicated HJ structures near the a-Si:H/c-Si interface region. For all of these phenomena, XPS and SIMS can be used<sup>41-42</sup>.

## 6. Leading research and development of HIT solar cells

The Sanyo research and development group was the first to apply an a-Si:H HJ to a c-Si solar cell in 1991<sup>43</sup>. An efficiency of 12.3% was obtained with their first HJ junction solar cell by directly depositing an a-Si:H(p) layer onto an n-type c-Si wafer. Due to the high defect-state density at the heterointerface, the solar cell shows relatively low  $V_{oc}$  and FF. Inserting of a thin a-Si:H(i) layer between a-Si:H(p) and n-type c-Si wafer lead to better cell performance. This incorporation of a-Si:H(i) lead to passivation of the dangling bonds on the c-Si surface, which lowered the a-Si:H/c-Si interface defect-state density. This lower defect-state density at the HJ interface led to improvement of the  $V_{oc}$  and FF. Using a passivated a-Si:H(i) layer, the highest efficiency of 14.8% was obtained for HIT solar cells<sup>43</sup>. A cell efficiency of 18.1% was achieved with the textured wafer surface for light trapping and the incorporation of a BSF on the back side of the device<sup>43</sup>. The incorporation of a textured wafer surface and the incorporation of a BSF led to a significant increase in  $J_{sc}$ . The performance of the HIT solar cell was further improved by applying double-side passivated a-Si:H(i) to the wafer. At the same time, ITO was also included in the back side between the BSF and metal-grid electrode. This designed structure was called a symmetrical HIT solar cell. This symmetrical HIT structure helps to suppress the thermal and mechanical stress in the wafers, which occur due to the

fabrication process, and also allow illumination of the device from both sides. Consequently, the applied both-side surface passivation and ITO incorporation onto BSF enabled HIT solar cell efficiencies of up to 21.3%<sup>44</sup>. The structure of the HIT solar cell is no longer developed, while the cell efficiency still keeps rising by the optimization of each-layer. By 2008, after applying a new cleaning process, the depositing a high-quality a-Si:H(i) layer, and reducing the plasma and/or thermal damage to c-Si surface during a-Si:H, TCO, and conductive electrode fabrication, an HIT cell open-circuit voltage and efficiencies as high as 725 mV and 22.3% was obtained, respectively<sup>45</sup>. With the same key approach, in 2009, the conversion efficiency of HIT solar cell reached a level of 23% for a 100.4 cm<sup>2</sup> practical-size crystalline silicon substrate ( $V_{oc}$ : 729 mV,  $J_{sc}$ : 39.52 mA/cm<sup>2</sup>, FF: 80.0%). At the same time, Sanyo was also trying to fabricate thinner HIT cells with thickness below 100  $\mu\text{m}$ <sup>45</sup>. With these thinner cells, the  $J_{sc}$  decreases slightly, but  $V_{oc}$  increases significantly, from 729 mV to 743 mV. This achievement is attributed to the extremely low bulk recombination. From this time, they focused on developing technologies for higher conversion efficiency with thin c-Si wafer (98  $\mu\text{m}$ ) with the aim of reducing cost. Since they announced their former record of 23.7%<sup>46</sup>, in 2011, they have continued to reduce recombination losses at the a-Si/c-Si heterointerface along with cutting down resistive losses by improving the silver paste with lower resistivity and optimization of the thickness in a-Si:H layers. Currently, Panasonic (Sanyo) obtained a new world record efficiency of 24.7% ( $V_{oc}$ : 750 mV,  $J_{sc}$ : 39.5 mA/cm<sup>2</sup> and FF: 83.2%) at the research level with a



**Fig. 5.** Development of HIT solar cell efficiency vs. time, all over the world. 1 to 10 indicates the HIT solar cell efficiency of Sanyo (200  $\mu\text{m}$  thick-wafer), Panasonic (Sanyo 98  $\mu\text{m}$  thick-wafer), HZB, EPFL, NREL, SKKU, Kanaka/Imes, Roth & Rau, AIST and INEA, respectively

practical-size of  $101.8 \text{ cm}^2$ <sup>22)</sup>.

Many research groups are following Sanyo's lead to work on HIT solar cells due to their high performance and low-temperature processing. Fig. 5 depicts the performance of the leading HIT solar cells at several companies and institutes all over the world. In 2008, at the Neuchatel PV-lab of EPFL, in order to enhance the carrier extraction, a new highly conductive doped  $\mu\text{-Si:H}$  layer was used as an emitter and BSF for HIT solar cells<sup>24)</sup>. With this approach, the EPFL can obtain a cell efficiency of 19.1% without surface texturing. An efficiency of 17.5% was obtained by AIST<sup>27)</sup> in 2009, for which a new  $\text{a-SiO}_x\text{:H}$  passivated layer for HIT solar cells was used. The thinning of the wafer to below  $100 \mu\text{m}$  was also investigated; but this thinner wafer led to reduction of both  $J_{\text{sc}}$  and  $V_{\text{oc}}$ . This result is contrary to Sanyo's results<sup>22)</sup>. By 2010, Roth et al. with the EPFL used the S-Cubed reactor to demonstrate efficiency of up to 21%, which is the second highest efficiency achieved, at this time<sup>47)</sup>. The ICDL of SKKU introduced a stacked-emitter and LiF-back contact to fabricate HIT solar cells, in order to enhance the carrier collection for both front and back contact. Using this HIT structure approach, the ICDL obtained efficiency as high as 20.6%<sup>48)</sup>. By 2012, a second record efficiency of 22.8% on a six inch semi-square was achieved by Japan's Kanenka Corporation with Belgium-based Imes. Their high efficiency is attributed to electroplated copper contact grid<sup>49)</sup>.

Without using any passivated layer, HZB can obtain efficiency as high as 19.8% based on a textured wafer<sup>8)</sup>. The high efficiency is attributed to the smoothing procedure after textured-surface and hydrogen post-treatment. This smoothing procedure and hydrogen post-treatment led to surface uniformity with less micro-roughness and improved  $\text{a-Si:H}$  film quality. In order to suppress ion bombardment of the surface, the HWCVD method for depositing  $\text{a-Si:H}$  layers was investigated by Wang et al.<sup>15)</sup> An efficiency of 19.1% was reported.

## Conclusions

Based on this, we may conclude the following.

At the front side, a large band offset at the interface results in larger built-in potential, thus yielding higher  $V_{\text{oc}}$  and cell performances. However with the band offset exceeding the value of 0.56 eV, it becomes a blocking layer for the carrier transport, resulting in deformation of the J-V characteristics. At

the back side, the value of the band offset and behaviour of the carrier transport depend on the type of base-wafers. The  $\Phi_{\text{TCO}}$  should at least lower be than 4.5 eV or higher than 5.1 eV for p- or n-type c-Si substrates, respectively.

The carrier transport mechanisms in HIT solar cells tend to be ambiguous. However, it looks like that at the low-forward-bias region ( $V < 0.4 \text{ V}$ ), MTCE dominates; and at the high-forward-bias region ( $V > 0.4 \text{ V}$ ), both the diffusion and recombination mechanisms dominate.

The buffer passivated layers with less crystallinity, highest hydrogen content, lowest void fraction and non-epitaxial growth on the c-Si surface during deposition are designed properties for interface passivation.

Using ATR-FTIR, the hydrogen bonding mode could be well understood. A very early stage of film growth could be observed by SE as well as SHG technique. TEM and SIMS techniques could also provide detailed information on film structures and composition, but cost, time-effectiveness, non in-situ operation and sample destruction remain as issues.

Currently, the world's highest conversion efficiency of 24.7% with a  $98 \mu\text{m}$  wafer of HIT solar cells for a total area of  $101.8 \text{ cm}^2$  is held by the Panasonic (Sanyo) group.

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