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Modeling and Prediction of Electromagnetic Immunity for Integrated Circuits

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Abstract

An equivalent model has been developed to estimate the electromagnetic immunity for integrated circuits under a complex electromagnetic environment. The complete model is based on the characteristics of the equipment and physical configuration of the device under test (DUT) and describes the measurement setup as well as the target integrated circuits under test, the corresponding package, and a specially designed printed circuit board. The advantage of the proposed model is that it can be applied to a SPICE-like simulator and the immunity of the integrated circuits can be easily achieved without costly and time-consuming measurements. After simulation, measurements were performed to verify the accuracy of the equivalent model for immunity prediction. The improvement of measurement accuracy due to the added effect of a bi-directional coupler in the test setup is also addressed.

Key words: Electromagnetic Immunity, Integrated Circuits, Modeling, Direct Power Injection.

Ⅰ. Introduction

Recent annual reports of the International Technology Roadmap for Semiconductor (ITRS) [1] indicate a trend whereby digital and analog integrated circuits (ICs) are becoming increasingly more vulnerable because the integration of the device, the number of interfaces, and the operation frequency is becoming more complicated while the node capacitance and noise margin are decreasing.

This trend, coupled with a complex electromagnetic environment, infers that the noise from direct injection, coupling, and radiated emission could easily affect a semiconductor system, and even damage it.

Noise analysis has attracted substantial attention. For example, Senthinathan and Prince [2] proposed accurate equations for the peak voltage of ground bounce estimation in ICs and demonstrated the influence of simultaneous switching noise (SSN). The effects of conducted and radiated emission for electronic devices were also widely discussed in [3]～[6]. Integrated circuits, in particular, are often considered as the main victim of electromagnetic interference (EMI) [7]. In other words, sufficient levels of radio-frequency (RF) noise can cause errors or malfunctions in digital and analog ICs.

The prediction of electromagnetic immunity is a pivotal issue for high speed and high frequency integrated circuits. The immunity of ICs is crucial for the performance of the related electronic devices, and even for the functioning of the entire operating system. Measurements based on standards have been developed for the estimation of IC immunity. These include direct power injection (DPI), bulk current injection (BCI), and TEM/GTEM cell methods, which are useful approaches for extracting immunity for integrated circuits. However, characterization of the susceptibility of ICs requires a complex test setup and costs both time and money. Designers also want appropriate equivalent modeling and simulation tools to ensure that the designed IC structure will satisfy the susceptibility criteria at the design stage, without the need for costly and time consuming fabrication and validation tests.

The procedural and advantage comparisons between measurement-based and simulation-based methods for immunity prediction are depicted in Fig. 1. Many studies have been published on the modeling and prediction of IC immunity, such as the ICEM [8], PDN-based [9] and power loss [10] models. These were all established based on parameters extracted by vector network analyzer

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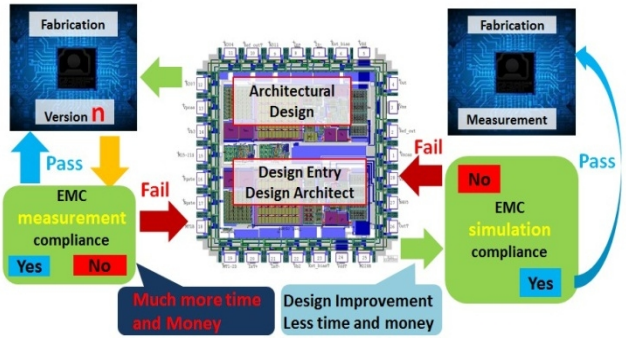

Fig. 1. Comparison between measurement-based and simulation-based immunity prediction algorithms.

measurements. An efficient way to establish an equivalent model is still needed to resolve this problem.

A chip needs to be fixed inside the package and mounted on the printed circuit board (PCB) for application in a real semiconductor system. The co-modeling of a chip-package-PCB thus becomes a substantial challenge for the prediction of IC immunity. This paper proposes an accurate equivalent circuit model for IC immunity prediction. In section Ⅱ, the partial element equivalent circuit and segmentation modeling method are used for co-modeling of a chip-package-PCB, and this is then applied to a SPICE-like simulator. The failure criterion and simulation algorithm for IC immunity prediction is described in section Ⅲ, and then applied to the simulation performance. Section Ⅳ describes the verification with measurements. Here, our established test setup is explained and the results between simulation and measurement are compared. The effect of a bidirectional coupler is also discussed. Finally, the predicted immunity of our integrated circuits is demonstrated.

Ⅱ. Co-modeling of a Chip-package-PCB System

The integrated circuits could not be tested separately; therefore, the package and PCB worked as a fixture during the measurements and real applications. The typical chip-package-PCB system is shown in Fig. 2. In our test, the chip is designed with size 4.5 mm×4.5 mm. A thin quad flat pack package (TQFP) with 80 pins acts as the channel between the chip and an outer, specially designed, 4-layer printed circuit board platform. The complicated physical configuration of the system makes the return paths for the signal/power transmission traces difficult to define and the entire system consists of three separate parts. Thus, the partial element equivalent circuit method and segmentation approach are used to solve the modeling problem. In addition, the power distribution network of an arbitrary and multi-plane PCB can be efficiently computed by a multi-input and multi-output transmission matrix method and this has been applied in this paper.

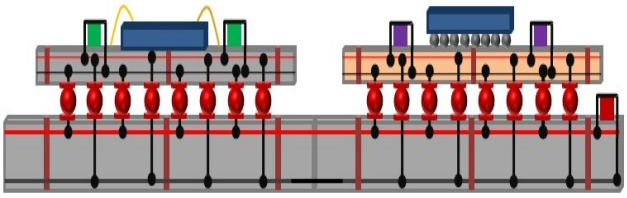

Fig. 2. Typical structure for a chip-package-PCB system.

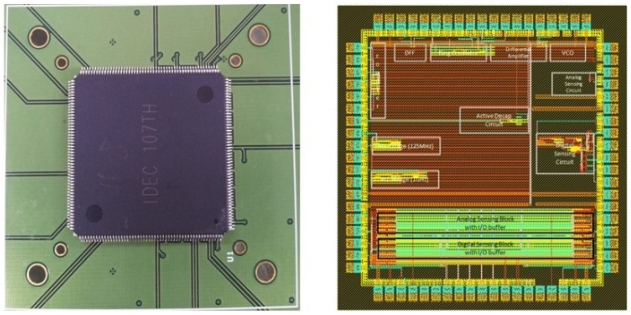

Fig. 3. Target IC for the immunity prediction test.

2-1 Modeling of the On-chip PDN

The target integrated circuits were designed to include phase-locked loop, ring oscillator, interface, and power distribution network function structures, and were fabricated by 0.18 μm CMOS technology, as shown in Fig. 3.

Among a series of measurement standards for predicting the immunity of an integrated circuit, we chose the direct power injection (DPI) method as our test approach since it performs a similar noise injection condition to the practical situation without any shielding closure. The on-chip power distribution network is always the victim under a power pin noise injection. The performance and response of the on-chip power distribution system should be reflected in the immunity prediction analysis. This requirement was satisfied by focusing on the power distribution network and analyzing it from both the structure and function sides.

Based on the power/ground grid structure shown in Fig. 4, we proposed an equivalent model that converts the unit P/G cell into a RLGC circuit by the analytic equivalent circuit approximation method to describe the characteristics of the on-chip PDN. The P/G grid structure has a pitch between the metal 4 and metal 5 layers of 0.8 μm and in the same layer, the distance between the power and ground metal is 50 μm. The equations for the resistance, inductance, and capacitance calculations are given by (1)~(7). In particular, the capaci-

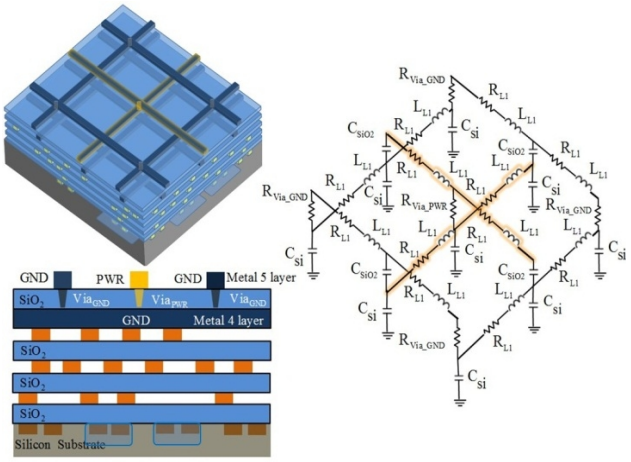

Fig. 4. Grid structure and equivalent circuit for on-chip power distribution network.

tance extraction considers the horizontal and vertical coupling effects between the metals in the same layer and in different layers and refers to [11]. In the equations, p, $F_{cor.}$, l_D are the pitch for the unit cell, a correction factor for the skin effect, and the vertical distance between the metal 4 and metal 5 layers, respectively. The core model was also established for its stable situation using passive elements. At this point, the core and on-chip model could be extracted and applied to the SPICE-like simulator in section Ⅲ.

$$R_L=\frac{p}{\sigma_{Al}tw}\sqrt{1+F_{cor.}\cdot f} \quad [\Omega/\mathrm{p}] \tag{1}$$

$$L_{self}=\frac{\mu_0}{2\pi}l\left(\ln\left(\frac{2l}{w+t}\right)+0.5\text{-}0.00177\right) \quad [\mathrm{H}] \tag{2}$$

$$L_{mutual}=\frac{\mu_0}{2\pi}l\left(\ln\left(\frac{l}{d}+\sqrt{1+\left(\frac{l}{d}\right)^2}\right)-\sqrt{1+\left(\frac{d}{l}\right)^2}+\frac{d}{l}\right) \quad [\mathrm{H}] \tag{3}$$

$$C_{SiO_2}=C_{OV}+2\cdot\left(C_{TT}+C_{VT}\right) \quad [\mathrm{F}] \tag{4}$$

$$C_{OV}=\frac{\varepsilon_{r\_IMD}\cdot\varepsilon_0\cdot w\cdot t}{l_D} \quad [\mathrm{F}] \tag{5}$$

$$C_{TT}=\frac{\varepsilon_{r\_IMD}\cdot\varepsilon_0\cdot[(w/2)+w]w\cdot t}{l_D+t} \quad [\mathrm{F}] \tag{6}$$

$$C_{VT}=\frac{2\cdot\varepsilon_{r\_IMD}\cdot\varepsilon_0\cdot\left(l_D+t+\sqrt{t^2+2\cdot l_D\cdot t}\right)}{\pi l_D}w \quad [\mathrm{F}] \tag{7}$$

2-2 Modeling of the TQFP Package

Between the silicon and PCB, the idea package plays a role as a transparent channel and does not affect the signal integrity (SI) or power integrity (PI) of the system.

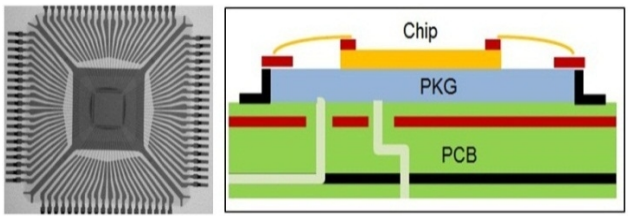

Fig. 5. (a) left: top view and (b) right: side view of the inside structure of the TQFP package.

However, the idea SI/PI characteristics cannot be achieved for the real package. An equivalent circuit for package analysis is demanded to be established. The thin quad flat pack package (TQFP) with 80-pin outputs is used as the carrier of our chip in the test. The inside configuration as determined by an X-Ray scan is shown in Fig. 5(a). From the center to the edge, the package consists of a pad on the chip, bonding wires, and a routed trace for signal propagation; this structure is also depicted in Fig. 5(b).

Traditionally, the package equivalent model is always designed as a simple pi or T type model for simplification. However, the simple model cannot accurately describe the different characteristic of the different parts of package. In other words, the package should be divided based on its configuration and then the parameters should be extracted segment by segment. This segmentation method makes the return path difficult to determine for a complex signal transmission trace, so we chose the analytic equivalent circuit method for parameter extraction. Without defining the return trace for the signal transmission path from the chip to the PCB, the partial inductance and capacitance are calculated based on their physical information. The parameter extraction for the bonding wires and transmission traces are derived from (8)~(12), where r_w, l_w, and d_{wire} are radius, length, pitch of wires and l, w, d_{pad} and t are length, width, distance and thickness of transmission trace, respectively. More details of the mutual inductance calculation are available in [12]. After obtaining the partial element, the equivalent circuit for the package from the chip pad to the lead frame was established based on the partial element equivalent circuit method; this is shown in Fig. 6.

$$L_{\mathrm{self\_wire}}=\frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l_w}{r_w}+\sqrt{\left(\frac{l_w}{r_w}\right)^2+1}\right)-\sqrt{1+\left(\frac{r_w}{l_w}\right)^2}+\frac{r_w}{l_w}\right] [\mathrm{H}] \tag{8}$$

$$L_{\mathrm{mutual\_wire}}=\frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l_w}{d+r_w}+\sqrt{\left(\frac{l_w}{d+r_w}\right)^2+1}\right)-\sqrt{1+\left(\frac{d+r_w}{l_w}\right)^2}+\frac{d+r_w}{l_w}\right] [\mathrm{H}] \tag{9}$$

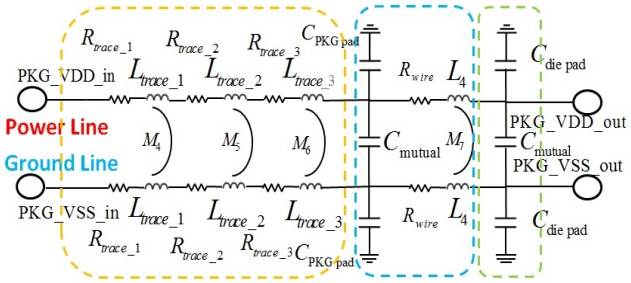

Fig. 6. Proposed equivalent circuit for the TQFP package.

$$L_{\text{self\_trace}}=\frac{\mu_0}{2\pi}\frac{1}{w^2}\left[lw^2\ln\left(\frac{l}{w}+\sqrt{\left(\frac{l}{w}\right)^2+1}\right)+l^2w\ln\left(\frac{w}{l}+\sqrt{\left(\frac{w}{l}\right)^2+1}\right)+\frac{1}{3}\left(l^3+w^3\right)-\frac{1}{3}\left(l^2+w^2\right)^{2/3}+\right]-2\times10^{-7}\frac{t}{w}l\ \text{[H]} \tag{10}$$

$$C_{\text{mutual\_wire}}=l\frac{\pi\varepsilon_r\varepsilon_0\cdot\ln\left[1+\left(\frac{2h}{d_{wire}}\right)^2\right]}{\ln\left(\frac{2h}{r_1}\right)\ln\left(\frac{2h}{r_2}\right)}\ \text{(F)} \tag{11}$$

$$C_{\text{mutual\_pad}}=l\frac{2\pi\varepsilon_r\varepsilon_0}{\ln\left[\pi^2 d_{pad}{}^2\left(\frac{1}{w_1+t}\right)\left(\frac{1}{w_2+t}\right)\right]}\ \text{(F)} \tag{12}$$

2-3 Modeling of the PCB Power Network

We designed a specific 12 cm by 12 cm printed circuit board, shown in Fig. 7, for directing the RF noise into the package pins. Interference from nearby components on the PCB is avoided by locating the chip with the package opposite and separate from other components such as the voltage regulator module and decoupling capacitors. We successfully guided the power path on the PCB, at this beginning stage of immunity prediction, by choosing a transmission power line instead of the traditional power plane. Thus, the noise can be

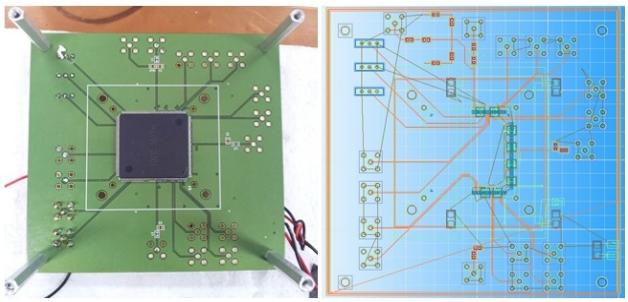

Fig. 7. Two side views of designed PCB for noise injection.

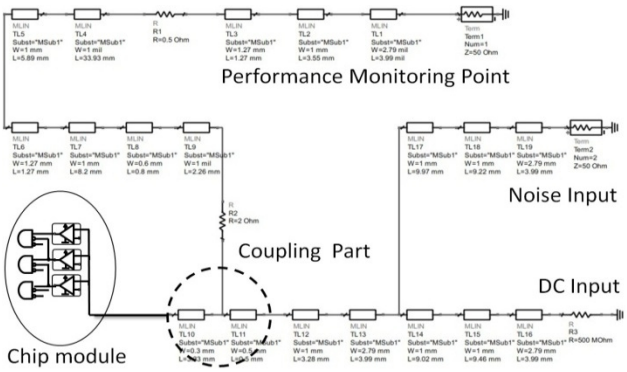

Fig. 8. Equivalent circuit for the power propagation path in a PCB.

injected from the SMA on the PCB edge, and will then propagate along the power line to finally arrive at the package input pins.

The transmission line matrix method for establishment of the power plan equivalent circuit can also be applied to develop the power transmission line structure. The difference is the reduction in the matrix and circuit dimensions for the line structure. The design algorithm for the PCB power network guides the DC power interrupted by the RF noise into the chip PDN. The chip performance can be monitored based on the feedback path that is coupled with the chip PDN. Fig. 8 describes the equivalent circuit for a PCB power network using a SPICE-like simulator. Based on the power transmission line structure, the power line can be represented by a microstrip line module and the parameters are extracted by its physical configuration.

An analytic equivalent circuit method, such as a partial element equivalent circuit, segmentation, and transmission line matrix method, can establish the equivalent model for the chip, TQFP package, and PCB power transmission network, respectively. After extracting the parameters for each part of the system, the complete model can be assembled and applied to the simulation for immunity prediction.

Ⅲ. Failure Criterion, Estimation Algorithm, and Immunity Prediction by Simulation

Whether we estimate the immunity by simulation or measurement, the important step before the immunity prediction is the definition of the failure criterion and the algorithm of the simulation or measurement performance. The limitation criterion for the ICs is the malfunction or broken situation, but we cannot choose this extreme limitation since we need to test the ICs continuously and the chip should be available during the whole period. For the DPI standard, a voltage fluctua-

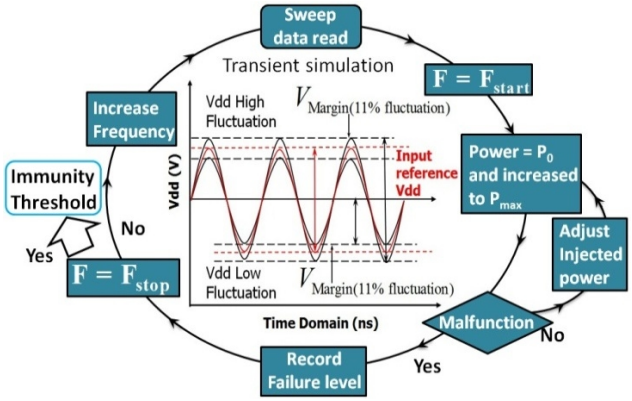

Fig. 9. Failure criterion and estimation algorithm.

tion will be generated on the power distribution network when the noise from outside affects our integrated circuits. Referring to the industry requirement, we chose 11 % fluctuation as our failure criterion. In other words, the integrated circuits are regarded as malfunctioning when the voltage fluctuation of PDN exceeds 11 % of the reference voltage in our immunity prediction shown in Fig. 9.

The loop circle in Fig. 9 also describes the algorithm for immunity estimation. The whole procedure works in both time and frequency domains. For each specific frequency, we perform a transient simulation that linearly increases the amplitude of the generated RF signal until the VDD exceeds the failure criterion. The integrated circuits are considered as defective at the failure point, and at the same moment, the corresponding forwarded power is recorded as a criterion. After completing the estimation at one frequency, this process is repeated at the next frequency until the end of the frequency band is reached. Ultimately, we obtain a continuous immunity threshold by connecting these discrete points.

After extracting the complete equivalent circuit and defining the failure criterion and estimation algorithm, the immunity could be predicted using the SPICE-like simulator. The equivalent model for immunity prediction in an Agilent SPICE-like simulator-the Advanced Design System (ADS) is shown in Fig. 10. The simulation is implemented in the time and frequency domain, so the frequency parameter sweep function is used during the transient simulation to realize the frequency scan. The predicted immunity based on simulation is demonstrated and validated by measurement results in section Ⅳ.

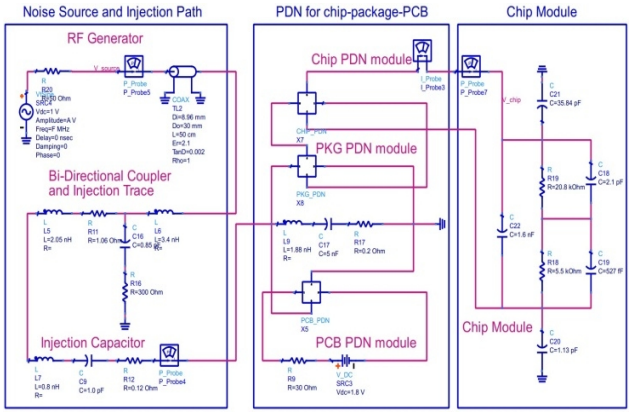

Fig. 10. Equivalent model for immunity prediction in a SPICE-like simulator.

Ⅳ. Measurement Setup and Verification

As we mentioned in section Ⅱ, the DPI method is appropriate for immunity prediction for a power distribution network. The typical measurement setup for the DPI method is depicted in Fig. 11.

As described for the DPI method in the IEC 62132-4 standard [13], a signal synthesizer generates an RF disturbance and then amplifies it by a power amplifier. The RF signal is ultimately injected into the ICs by the designed guide path on the PCB. A bidirectional coupler plays an important role in partitioning and quantifying the power transferred into the ICs. The power transferred into the PCB could be calculated by the coupling ratio of the directional coupler. An oscilloscope and a spectrum analyzer are used to identify the malfunction level for the ICs.

In the electromagnetic immunity estimation process, the forwarded power is regarded as the immunity criterion. The difference between the simulation and the standard test setup is the addition of a component bidirectional coupler in the test only, while in the simulation we have a virtual power probe instead. Comparison of the results from the simulation and measurement is made possible by establishing the bidirectional coupler equivalent circuit in the simulator. The results from simulation and measurement using directional coupler show good agreement with each other and the predicted immunity trend is shown in Fig. 12. Thus, our proposed

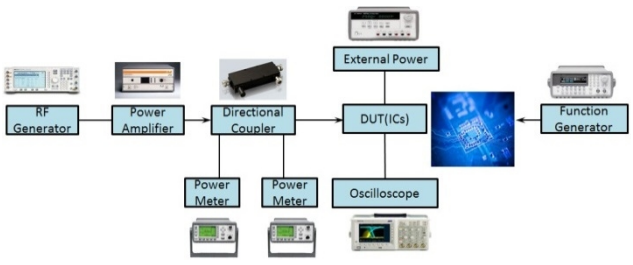

Fig. 11. Typical measurement setup for the direct power injection method for immunity prediction.

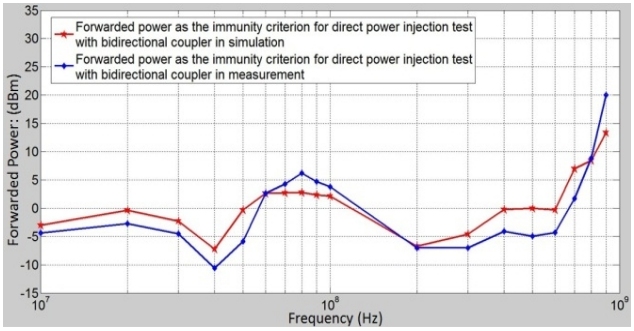

Fig. 12. Comparison of simulation and measurement results based on a DPI test with a bidirectional coupler.

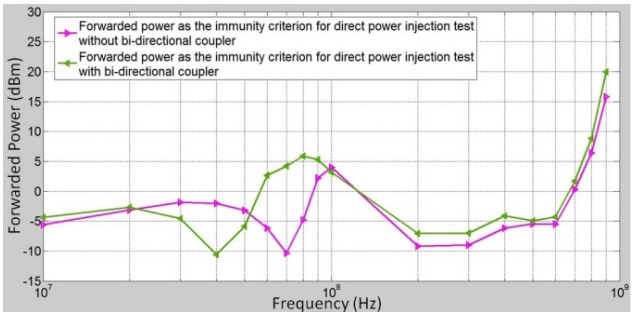

Fig. 13. Comparison of predicted immunity with and without a bidirectional coupler.

equivalent model has been verified through this comparison, and the acceptable discrepancy between simulation and measurement could be explained by the impedance mismatch in the measurements.

However, the use of the coupler could add an extra-effect to the immunity estimation. We gained a better understanding of the influence of the bidirectional coupler on the IC immunity by designing a coupling circuit between the chip PDN and PCB power path that allows direct measurement at the PCB level of the power forwarded into the chip. The comparison of immunity measured by the directional coupler and the coupling circuit is shown in Fig. 13.

The comparison results revealed a resonant point shift for the forwarded power indicator when we removed the bidirectional coupler. This shift arises from the impedance of the bidirectional coupler. Extra impedance from the coupler changes the resonance point of the whole system impedance, and then influences the forwarded power chart. As a result, the use of the bidirectional coupler would affect the accuracy of estimated immunity. We could resolve this extra influence caused by the bidirectional coupler by efficient use of a de-embedding method, which could remove the characteristics of the bidirectional coupler from the final test results. Another way would be to design the sensing circuits to measure the power injected into the core. This method would not require the use of a bidirectional coupler in the DPI test.

Ⅴ. Conclusion

In this paper, we proposed an equivalent circuit model that can be applied to a SPICE-like simulator for electromagnetic immunity prediction of integrated circuits, with special attention to the power distribution network. Each model of the chip, package, and PCB parts has been extracted and established based on the analytic equivalent circuit method. After modeling, the immunity of our designed integrated circuits was predicted by the simulation, and then measurements based on the DPI method were used to verify our estimates. The effect of a bidirectional coupler was also investigated as a way to improve the accuracy of immunity prediction.

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