바이오응용 무선전력전달을 위한
13.56 MHz CMOS 다단 정류기

(A 13.56 MHz CMOS Multi-Stage Rectifier for Wireless Power Transfer in Biomedical Applications)

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요 약

0.18-μm CMOS 반도체 공정을 이용하여 신체에 깊이 이식되어 있는 deep implant 의료 전자기기에서의 무선전력전달을 위한 고효율의 다단 정류기 (multi-stage rectifier)를 구현하였다. 세 개의 단계로 이루어진 정류기는 cross-coupled 된 구조를 이용하여 외부에서 전달되는 작은 AC 입력 신호를 boost하여 1.2-1.5 V의 DC 출력 신호를 implant 전자기기로 전달한다. 설계 된 정류기는 13.56 MHz에서 0.6-Vpp의 작은 RF 입력 신호와 10-kΩ의 load 저항이 연결 된 측정 환경에서 최대 70 %의 전력 변환 효율을 달성하였다.

Abstract

An efficient multi-stage rectifier for wireless power transfer in deep implant medical devices is implemented using 0.18-μm CMOS technology. The presented three-stage rectifier employs a cross-coupled topology to boost a small input AC signal from the external device to produce a 1.2-1.5 V output DC signal for the implant device. The designed rectifier achieves a maximum measured power conversion efficiency of 70% at 13.56 MHz under the conditions of a low 0.6-Vpp RF input signal with a 10-kΩ output load resistance.

Keywords : CMOS rectifier, multi-stage rectifier, gate cross-coupled, wireless power transfer, biomedical implant devices

Ⅰ. Introduction

One of the most important issues in the development of implantable biomedical devices is the consistent provision of a stable and reliable power supply. Wireless inductive links are widely used for this purpose as batteries require a periodic replacement which causes much inconvenience and

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risk to the patient. The transfer efficiency is an important parameter for this wireless power link as the amount of transmitted power can be reduced and/or a longer distance link can be achieved. Deep implant medical devices such as blood flow sensor [1], which is placed deep inside the patient, especially require a highly efficient wireless power transfer system which achieves maximum efficiency and generate large enough output DC voltage at low AC input signal power. Fig. 1 shows the typical wireless power transfer system, consisting of the external power delivery part, inductive coils, rectifier, and a regulator. The overall efficiency of the transfer system can be represented as;
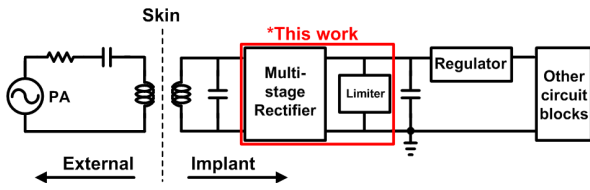
그림 1. 무선 전력 전달 시스템의 전체적인 블록도
Fig. 1. Overall block diagram of the wireless power transfer system.

$$\eta_{Total} = \eta_{PA} \times \eta_{Coil} \times \eta_{Rect} \times \eta_{Reg}s \qquad (1)$$

where η_{PA} represents the power amplifier efficiency, η_{Coil} is the inductive coil link efficiency between the external and internal coils, η_{Rect} is the efficiency of the rectifier, and η_{Reg} represents the regulator efficiency. The efficiency of the rectifier is usually the key factor on the internal side in achieving high overall transfer efficiency since the coil efficiency is limited due to the physical constraints of the implant coil while high regulator efficiency can usually be achieved.

In this paper, we present a CMOS rectifier for wireless power transfer in deep implant applications which uses three cascaded stages to achieve high efficiency at low input signal power and generate a large enough output DC voltage for the implant device. Section II discusses required specifications while Section III describes the conventional solutions and the designed circuit in detail. Section IV presents the experimental results followed by the conclusions in Section V.

II. Specification

The target application for the presented rectifier is an implantable blood flow monitoring system which is to be embedded in a prosthetic graft for early graft failure detection[2]. Prosthetic vascular grafts are frequently applied in vascular surgery for bypass in lower limb ischemia or as a haemodialysis conduit in renal failure. Graft failure can result in deleterious consequences for the patients and therefore the measure of blood flow rates in these grafts can serve as a valuable prediction of subsequent thrombosis
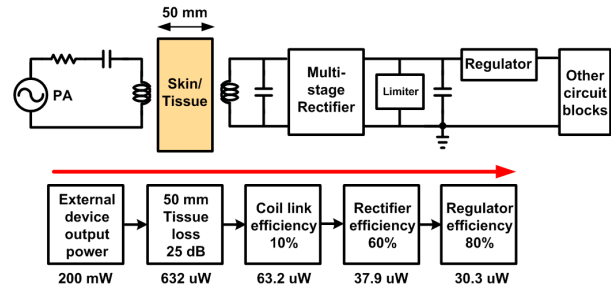

그림 2. 무선 전력 전달 과정
Fig. 2. Power delivery chain.

and failure.

The implant device is to be embedded up to 50 mm deep inside the human body and therefore the wireless power transfer system has to provide a reliable power and supply voltage to the circuits inside the implant. The external device is to supply 200 mW to the implant device. Assuming an industrical, scientific, and medical (ISM) band frequency of 13.56 MHz is used, the tissue loss for 50 mm distance is approximately 25 dB[2].

As the in-body environment constraints the size and space available, the external and internal coupling coils are quite different. The external coil can be as large as 10 cm in diameter, while the internal coil can have up to 6 mm, which critically degrades the coupling efficiency to around 10%. As the implant device requires around 20 μW power for operation, the combined efficiency of the rectifier and the following low-dropout regulator (LDO) has to be over 45%. Assuming the LDO can achieve 80% efficiency, the power conversion efficiency of the rectifier must meet over 60% for the system with some margin. This specification is illustrated in Fig. 2.

Due to the long distance and poor efficiency in the coils, the incoming AC input voltage to the following rectifier input can be as low as 600 mVp-p. As the internal circuit blocks of the monitoring system operate at a low supply voltage of 1-V, the following low-dropout regulator (LDO) after the rectifier in the wireless power transfer chain needs to receive over 1.2 V DC voltage as its input to produce 1 V DC to the rest of the circuit blocks, assuming the LDO efficiency is around 70 to 80%. To summarize the
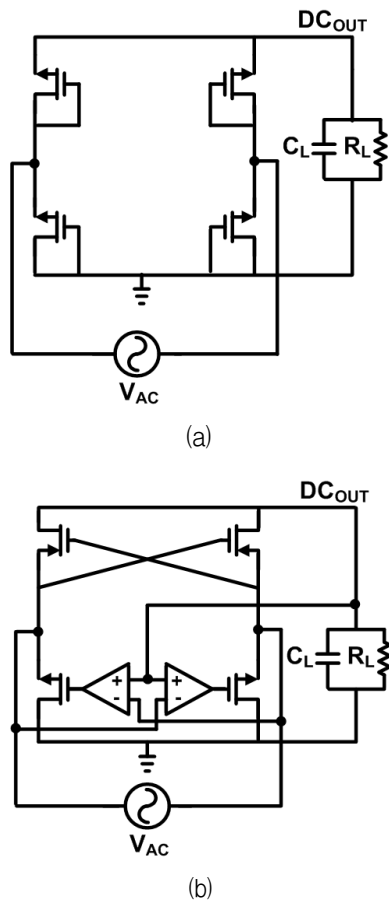
(a)

(b)

그림 3. 기존의 정류기 회로도 (a) full-wave 다이오드
　　　 정류기 (b) 비교기 기반의 정류기
Fig. 3. Schematic of the conventional rectifiers.
　　　　(a) full-wave diode rectifier
　　　　(b) comparator-based rectifier

requirements for the design, the rectifier has to be able to provide at least 1.2-V DC output from a 13.56 MHz input AC voltage signal of 600 mVp-p with an efficiency of over 60%.

III. CMOS Rectifier Design

1. Conventional Rectifiers

There are several rectifiers which are widely used for wireless power transfer in both consumer and biomedical applications. The most typical topology is the full-wave diode-bridge rectifier shown in Fig. 3(a). This topology, however, has a limitation in achieving a high efficiency since it requires two threshold voltage drops across the diodes for operation[3]. Another popular rectifier type is the comparator-based rectifier shown in Fig. 3(b)[4~9].

High efficiencies have been achieved through the usage of comparators in order to maximize the forward current while minimizing the reverse leakage current. The utilization of dynamically powered comparators allows low power consumption while achieving a highly efficient rectifier. The problem of these comparator-based rectifiers is that it requires a large enough input AC signal of over two threshold voltage drops in order for the comparator to start-up. Without the comparator in operation, the rectifier shows a dramatic degradation in efficiency in low input signal region and thus is not appropriate for deep implant applications.

2. Proposed Rectifier Circuit Design

The rectified output DC voltage can be expressed as;

$$V_{outDC} = V_{inAC} - V_{drop} \qquad (2)$$

In order for the rectifier to operate at small input voltage while delivering the required output voltage and achieve high efficiency, the voltage drop has to be minimized. Also, multiple stages are needed so that the small input signal may be boosted to produce a sufficiently large output voltage. A gate cross-coupled circuit topology is employed for this purpose to realize the multi-stage rectifier for the implant system. The advantage of this rectifier is that it has a low on-resistance during operation which enables small voltage drop in comparison to the full-wave diode-bridge rectifier and the comparator-based types. Most importantly, the rectifier can operate at small input swings as low as down to around one threshold voltage due to its structure as shown in Fig. 4. The rectifier consists of NMOS and PMOS transistors operating as switches in which the gates are driven by the differential input RF signal.

In the positive cycle of the operation (when RF+ is high), M_{P1} and M_{N2} will turn on and the current will flow to the load consisting of R_L and C_L to produce the rectified DC voltage. At this cycle, both
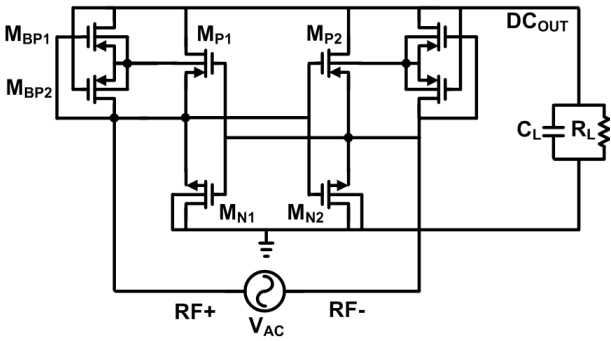
그림 4. 제안 된 CMOS 정류기의 회로도
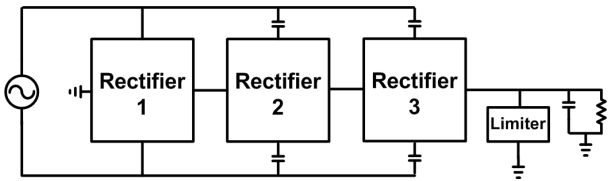Fig. 4. Schematic of the proposed CMOS rectifier.

그림 5. 세 단계 정류기의 블록도
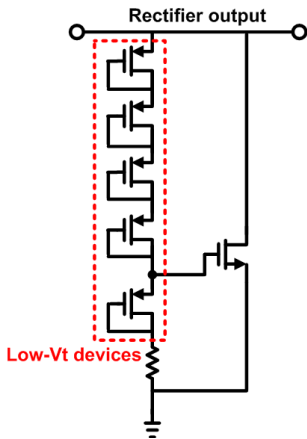Fig. 5. Block diagram of cascaded three-stage rectifier.

그림 6. 정류기 출력에 연결 된 DC limiter의 회로도
Fig. 6. Schematic of DC limiter at the rectifier output.

M_{P2} and M_{N1} will be OFF. In the negative input cycle, the rectifier will operate similarly with M_{P2} and M_{N1}. The sizing of the transistors affects the on-resistance value and therefore is important in deciding the maximum efficiency of the rectifier. The power conversion efficiency (PCE) should be maximized in the minimum input condition so that the minimum amount of power that must be supplied to the implant device is guaranteed in the worst case scenario. With careful simulations considering the minimum input signal level and output load resistance which mimics the amount of current that must be
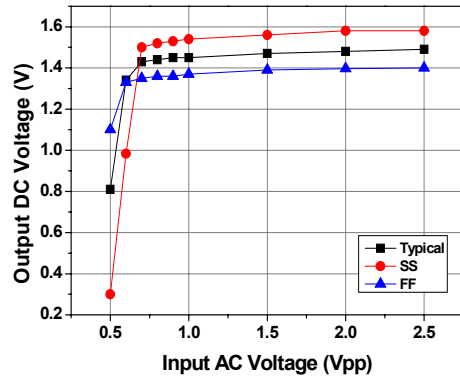

그림 7. 입력 AC 전압 대 출력 DC 전압에 대한 코너 시뮬레이션
Fig. 7. Corner simulation plot of increasing AC input voltage versus DC output voltage.

supplied to the whole internal device, the W/L sizing of the PMOS and NMOS transistors are decided to be $316\mu m/0.18\mu m$ and $68\mu m/0.18\mu m$, respectively. Active body biasing circuit, consisting of M_{BP1} and M_{BP2} transistors, are used to make sure the body nodes of M_{P1} and M_{P2} are always tied to the higher potential of RF input or DC output.

As shown in Fig. 5, three stages of gate cross-coupled rectifiers are cascaded to boost the output voltage up to 1.2 V at 600 mVp-p input condition. Metal-insulator-metal (MIM) capacitors are used at the input of second and third stage rectifier inputs for charge storage for multi-stage boost operation. A DC limiter, shown in Fig. 6, is employed to limit the rectifier output DC voltage at 1.5 V so that the following circuit blocks are protected from the resulting high voltage signal assuming the distance between the external and internal devices get too close to each other. Diode-connected low-threshold PMOS devices are used to realize the limiter.

Fig. 7 shows the process corner simulation results of the input AC signal versus output DC voltage for the designed three-stage rectifier. The simulation is carried out at 13.56 MHz input frequency and at 37.5℃ temperature to mimic in-body temperature with a load of 10-kΩ resistor and 10-μF capacitor.

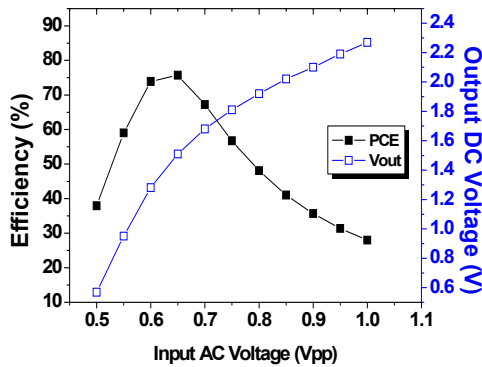The results show that at least 1.2 V is achieved at

그림 8. 입력 AC 전압 대 변환 효율 및 출력 DC 전압
에 대한 시뮬레이션
(출력 단에 DC limiter는 불포함)
Fig. 8. Simulation plot of varying AC input voltage
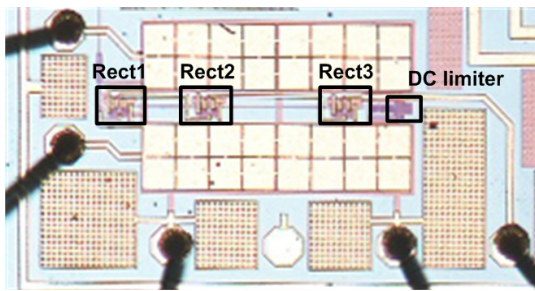versus effciency and output DC voltage.
(DC limiter removed at the output)

그림 9. 정류기의 칩 사진
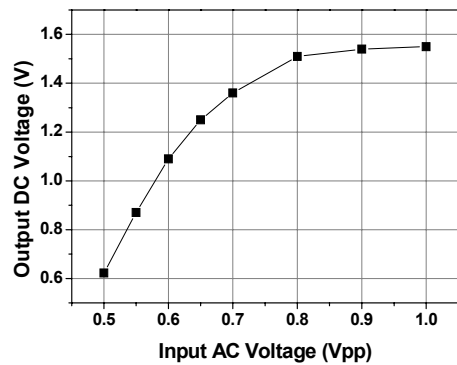Fig. 9. Chip microphotograph of three-stage rectifier.

그림 10. 입력 AC 전압 대 출력 DC 전압의 측정 결과
Fig. 10. Measured output DC voltage versus varying
input AC voltage.

그림 11. 입력 AC 전압 대 변환 효율의 측정 결과
Fig. 11. Measured PCE versus varying input AC voltage.

all process corners with the specified minimum input voltage at 600 mVp-p. Also, the limiter is able to limit the output DC voltage below 1.6 V at different corners. Fig. 8 presents the varying input versus PCE and output DC voltage simulation results under the same condition as the previous simulation. The output DC limiter is disconnected in this simulation. A maximum simulated PCE of 76% is achieved around the low input AC voltage of 590 to 650 mVp-p. A steep increase in the output DC voltage and PCE in the 500 to 600 mVp-p input voltage region is due to the start-up of rectifier transistors for operation.

Ⅳ. Experimental Results

The designed rectifier is fabricated in a one-poly six-metal (1P 6M) 0.18-μm CMOS process. The chip microphotograph is shown in Fig. 9, where the area of the core is 0.125 mm². Most of the layout area is consumed by the MIM interstage input capacitors of the second and third stage rectifier. Much attention is given in the input layout path as parasitic resistance degrades the efficiency. The die is housed in a quad flat nonleaded (QFN16) package for measurement on a FR4 PCB. The default measurements are done at 13.56-MHz input frequency with an output load of 10-kΩ resistor and 10-μF capacitor.

The measured rectified output DC voltage versus varying input AC voltage is shown in Fig. 10. The output DC voltage increases linearly to the input signal until it reaches 1.55 V which is limited by the output limiter circuit.

In order to measure the PCE, which is defined as;

Table 1.   Low-frequency CMOS Rectifier Benchmark for Wireless Power Transfer Applications.

Parameter	[4]	[6]	[7]	This work
Freq. (MHz)	10	13.56	13.56	13.56
Process	0.18μm CMOS	0.35μm CMOS	0.5μm CMOS	0.18μm CMOS
|Vtp|/Vtn (V)	N/A	0.73/ 0.55	0.92/ 0.78	0.49/ 0.42
Input Amplitude (|Vac|)	3	3.5	3.8	0.63
Output DC (V)	3.87	3.2	3.12	1.2
R load (kΩ)	200	1.8	0.1	10
Max.PCE (%)	N/A	87(sim.)	80.2	70
No. of stages	3	1	1	3
Area (mm²)	0.0112	0.0055	0.18	0.125

$$\eta_{Power} = \frac{P_{outDC}}{P_{inAC}} \qquad (4)$$

both the input and output power has to be measured and offline calculate the resulting PCE. To measure the input power, the input current is calculated by placing a small series resistor at the input of therectifier on the PCB and the voltage between the resistor terminals is measured. A maximum PCE of 70% is measured at an input voltage of 650 mV, as shown in Fig. 11.

Table I compares the presented three-stage rectifier with previous low-frequency CMOS rectifiers. Although higher efficiency is achieved in the previous rectifiers using comparators for switching control, a large input signal is required for operation. With regards to the small input signal required for operation, the implemented rectifier compares favorably to the previous works while still achieving a good conversion efficiency and satisfying the required specifications.

V. Conclusions

A highly efficient multi-stage rectifier for deep implant applications is implemented using 0.18μm CMOS process. A cross-coupled topology is utilized to facilitate low-input operation, while three cascaded stages are used to produce a large DC output for the following stages in the implant device. A power conversion efficiency of 70% is achieved at 13.56 MHz under conditions of a 600-mVpp RF input signal with a 10-kΩ output load resistance.

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