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Improved Power Quality IHQRR-BIFRED Converter Fed BLDC Motor Drive

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Abstract

This paper presents an IHQRR (Integrated High Quality Rectifier Regulator) BIFRED (Boost Integrated Flyback Rectifier Energy Storage DC-DC) converter fed BLDC (Brushless DC) motor drive. A reduced sensor topology is derived by utilizing a BIFRED converter to operate in a dual DCM (Discontinuous Conduction Mode) thus utilizing a voltage follower approach for the PFC (Power Factor Correction) and voltage control. A new approach for speed control is proposed using a single voltage sensor. The speed of the BLDC motor drive is controlled by varying the DC link voltage of the front end converter. Moreover, fundamental frequency switching of the VSI's (Voltage Source Inverter) switches is used for the electronic commutation of the BLDC motor which reduces the switching losses in the VSI. The proposed drive is designed for a wide range of speed control with an improved power quality at the AC mains which falls within the recommended limits imposed by international power quality standards such as IEC 61000-3-2.

Key words: BIFRED Converter, BLDC motor, DCM, IHQRR, PFC, Power Quality

I. INTRODUCTION

Research on PFC (Power Factor Corrected) converters for attaining an improved power quality at the AC mains became popular after the stringent limits were imposed by international power quality standards such as IEEE-519 and IEC-61000-3-2 [1], [2]. Power quality indices such as PF (Power Factor), DPF (Displacement Power Factor), THD (Total Harmonic Distortion) and CF (Crest Factor) of the supply current are limited to within certain prescribed value by these standards for different classes of equipment [1], [2]. For drive applications i.e. class-A equipment (under 600 W, <16 A per phase), a power factor above 0.98 and a THD of the supply current below 5% is considered to be an acceptable limit to meet the requirements of IEC-61000-3-2 [2].

BLDC (Brushless DC) motors are becoming popular for the development of low and medium power equipment. They offer many advantages including a high torque and watt per unit of weight, a high efficiency, a high reliability, low noise levels and a long lifetime (since no brush and commutator are used) with the reduced EMI (Electromagnetic Interference) problems [3]-[6]. Hence they find application in many types of household equipment like washing machines, air conditioners, refrigerators, mixers, grinders, etc. Moreover, BLDC motors are also preferred in industrial equipment like power tools, positioning systems and actuators, electrical vehicles and medical equipment due to the above mentioned advantages [3]-[6]. BLDC motors are electronically commutated motors with three phase distributed windings on the stator and permanent magnets on the rotor [7]-[10]. They are powered by a DC source via a three-phase VSI (Voltage Source Inverter) with the switching signals of the switches based on the rotor position as sensed by Hall Effect sensors [10].

A BLDC motor fed by a DBR (Diode Bridge Rectifier) with a high DC link capacitor injects high amount of harmonics at the AC mains. The supply current drawn by such a configuration is peaky in nature, having a high THD (Total Harmonic Distortion), and results in a poor power factor. Many configurations are reported in the literature for the improvement of power quality at the AC mains for single phase and three phase supplies [11], [12]. Two stage converters have been in nominal practice which preferably includes a boost stage for PFC and a buck-boost stage for voltage control [13]. Single stage PFC converters are preferred over multi stage converters because of the requirement of two different controls and the high losses in multi stage converters [11], [12].

An IHQRR (Integrated High Quality Rectifier Regulator)

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combines two converters for attaining an improved power quality at the AC mains [14]-[18]. The major advantages of a single switch in such converters include high efficiency (reduced switching losses) and performance that is similar to a single stage converter. A BIFRED (Boost Integrated Flyback Rectifier Energy Storage DC-DC) converter is an IHQRR which integrates a boost PFC stage with a flyback converter using a single switch. The boost converter working in DCM (Discontinuous Conduction Mode) operates as an inherent power factor corrector [11]. The flyback converter is allowed to work in DCM or CCM (Continuous Conduction Mode) depending upon the requirements. CCM operation requires a current multiplier approach using three sensors (2-voltage and 1-current) whereas a voltage follower approach is used for operation of the converter in DCM using a single voltage sensor [11], [12].

A requirement in the development of a high performance, low cost BLDC drive encourages the use of BIFRED converter as a front end converter for PFC and voltage control. The cost reduction of the drive is considered on account of using a reduced number of sensors. Moreover, reducing the switching losses in the VSI to increase the efficiency of the drive is also a major consideration. Finally, the performance of the proposed drive is analyzed for speed control with improved power quality at the AC mains.

II. PROPOSED BIFRED CONVERTER FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed IHQRR-BIFRED converter based VSI fed BLDC motor drive using a single voltage sensor. A new approach for controlling the speed of the BLDC motor with the DC link voltage control is used [19]. The BIFRED converter is operated in dual DCM to achieve power factor correction and DC link voltage control by utilizing a voltage follower approach [18]. The integrated boost converter operating in DCM acts as an inherent power factor pre-regulator. Moreover, the flyback converter is also designed to work in DCM for voltage control. A high frequency MOSFET (Metal Oxide Semiconductor Field Effect Transistor) with an appropriate rating is used in the front end converter and IGBT's (Insulated Gate Bipolar Transistor) are used in the VSI for low frequency operation. The losses in the VSI are reduced by using fundamental frequency switching of VSI's switches to achieve electronic commutation of the BLDC motor. The proposed drive is designed for a wide range of speed control with an improved power quality at the AC mains.

III. OPERATION AND DESIGN OF THE BIFRED CONVERTER FED BLDC MOTOR DRIVE

An IHQRR-BIFRED converter is designed to operate in dual DCM. The current in the boost inductor L_i and the magnetizing

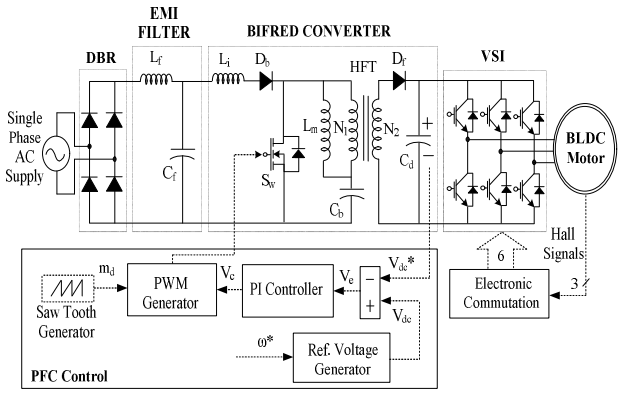


Fig. 1. Proposed BIFRED converter fed BLDC motor drive.

inductance L_m of the HFT (High Frequency Transformer) become discontinuous in a switching period. The value of L_i and L_m are chosen such that the current in L_i becomes discontinuous before the current in L_m reaches zero for the dual DCM operation, as shown in Fig. 2 [18]. The operation of the BIFRED converter is classified into four different modes as shown below [14]-[18].

Mode A: In this mode, switch S_w is turned on such that the input current i_{Li} flows through S_w and diode D_b to energize the boost inductor L_i, as shown in Fig. 3 (a). The energy stored in blocking capacitor C_b is transferred to the magnetizing inductance of transformer L_m. Diode D_f remains reversed biased and DC link capacitor C_d supplies the energy to the load which results in a reduction of the DC link voltage, as shown in Fig. 2.

Mode B: The switch S_w is turned off in this mode and the current flows through the boost inductor L_i and the magnetizing inductance L_m of the HFT, to charge the bulk capacitor C_b as shown in Fig. 3 (b). The energy stored in L_m is transferred to the output side via the HFT with diode D_f which is in the forward biased position to charge the DC link capacitor C_d, hence the DC link voltage begins to increase in this mode, as shown in Fig. 2. At the end of this mode, the inductive energy of the boost inductor is completely discharged and current i_{Li} (or I_{in}) becomes zero.

Mode C: Switch S_w remains in the turn off position and the remaining stored energy of L_m is transferred to the DC link capacitor C_d through the HFT, as shown in Fig. 3 (c). Hence the voltage across the DC link capacitor C_d increases. In this process diode D_b remains reverse biased so that the current cannot flow through the boost inductor L_i. At the end of this mode the energy stored in the magnetizing inductance L_m is completely drained and the bulk capacitor C_b remains at its highest possible voltage.

Mode D: In this mode neither of the diodes D_b nor D_f is conducting, as shown in Fig. 3 (d). The boost inductor L_i and the magnetizing inductance L_m do not have any stored energy.

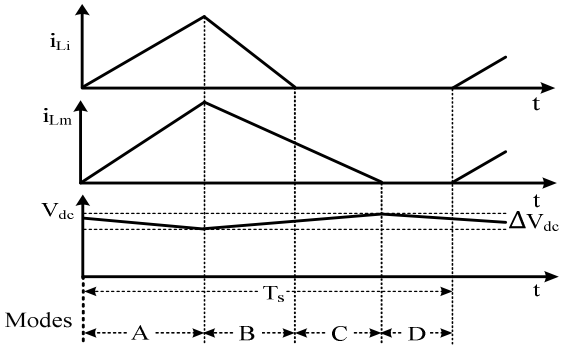


Fig. 2. Waveforms showing different modes in DCM-DCM configuration of BIFRED converter.

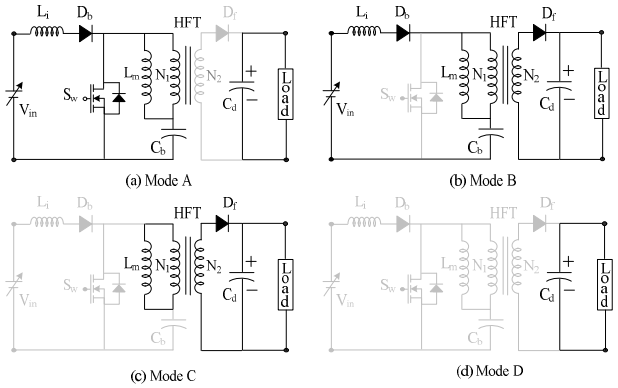


Fig. 3. Different modes of operation of BIFRED converter.

Thus no transfer of energy through the HFT takes place and the required energy to the load is supplied by the DC link capacitor C_d. Hence the voltage across the capacitor starts decreasing, as shown in Fig. 2.

The design of a BIFRED converter consists of designing and the selection of optimal value for the boost inductor L_i, the turns ratio N_1:N_2 and the magnetizing inductance L_m of the HFT, the bulk capacitor C_b and the DC link capacitor C_d. The EMI filter is also designed to eliminate the ill effect of the high switching frequency reflection in the supply system. A BIFRED converter depicts an isolated SEPIC (Single Ended Primary Inductor Converter) but with an extra diode D_b which allows the boost inductor to work independently in DCM as a power factor pre-regulator without disturbing the performance of the flyback converter for voltage control. Therefore, the design of a BIFRED converter is similar to that of an isolated SEPIC but with both L_i and L_m operating in DCM.

A 500W converter system is designed for controlling the DC link voltage from 40V to 130V for speed control. A single phase supply of 220V (V_s), 50Hz (f_L) is applied to the DBR.

The value of V_{in} is expressed and calculated as [13]:

$$V_{in} = \frac{2\sqrt{2}V_S}{\pi} = \frac{2\sqrt{2}x220}{\pi} = 198V \tag{1}$$

For an isolated SEPIC, which is a buck-boost configuration, the DC link voltage V_{dc} relation with the input voltage V_{in} (voltage across the DBR terminals) is given as [12]:

$$V_{dc} = \frac{N_2}{N_1}\frac{D}{(1-D)}V_{in} \tag{2}$$

Using above equation (2), the duty ratio of the rated DC link voltage (i.e. 130V) is calculated for the turn's ratio N_1:N_2= 1:2 (since the desired output voltage is nearly half of the input voltage) as:

$$D = \frac{\left(\frac{N_2}{N_1}\right)V_{dc}}{V_{in}+\left(\frac{N_2}{N_1}\right)V_{dc}} = \frac{\left(\frac{1}{2}\right)x130}{198+\left(\frac{1}{2}\right)x130} = 0.2471$$

The expression for the boost inductor L_i to work in CCM is given as [12]:

$$L_i = \frac{V_{in}D}{f_S\Delta I_{in}} \tag{3}$$

where f_S is the switching frequency and ΔI_{in} is the permitted ripple current in L_i.

At critical conduction mode the current ripple is:

$$\Delta I_{Li} = 2I_{in} \tag{4}$$

Hence the critical value for the inductor to operate at the boundary of CCM and DCM is given and calculated as [12]:

$$L_{iC} = \frac{V_{in}D}{2f_SI_{in}} = \frac{198x0.2471}{2x45000x\left(\frac{500}{198}\right)} = 215.27\mu H \tag{5}$$

Now the value of the boost inductor to operate in DCM is evaluated using:

$$L_i < L_{iC} \tag{6}$$

Hence the value of L_i is selected using equation (6) as 150μH.

The critical value of the magnetizing inductance L_{mC} to operate at the boundary of CCM and DCM is given and calculated as [12]:

$$L_{mC} = \frac{(1-D)^2R_L}{2Df_S\left(\frac{N_2}{N_1}\right)^2} = \frac{(1-0.2471)^2x\left(\frac{130^2}{500}\right)}{2x0.2471x45000x\left(\frac{1}{2}\right)^2} = 3.446mH \tag{7}$$

Hence to operate in a deep DCM, the value of the magnetizing inductance L_m is given as:

$$L_m << L_{mC} \tag{8}$$

The value of L_m is taken to be around 1/10th of L_{mC} to guarantee a DCM over a wide range of the DC link voltage control [20]. The selected value of L_m using equation (8) is as 350μH.

The expression and calculation of the bulk capacitor C_b for ΔV_{Cb} (permitted ripple voltage in the bulk capacitor) taken as

5% of the peak input voltage is given as is given as [12]:

$$C_b = \frac{V_{dc} D\left(\frac{N_2}{N_1}\right)}{R_L f_S \Delta V_{Cb}} = \frac{130x0.2471x\left(\frac{1}{2}\right)}{\left(\frac{130^2}{500}\right)x45000x(.05x311)} = 679.08nF \quad (9)$$

Hence the selected value for the bulk capacitor is 750nF.

The value of the DC link capacitor C_d for the DC link current I_{dc} and the permitted ripple voltage ΔV_{dc} as 2% of the desired DC link voltage V_{dc} is given and calculated as [12]:

$$C_d = \frac{I_{dc}}{2\omega_L \Delta V_o} = \frac{\left(\frac{500}{130}\right)}{2x2\pi x50x0.02x130} = 2354.36\mu F \quad (10)$$

Hence the value of the DC link capacitor is selected as 4000 μF (to limit the DC link voltage ripple so that it is even less than 2%).

The input LC filter of the PFC converter is designed as given by Vlatkovic et.al. [21]. The maximum value of the filter capacitance C_{max} is given and calculated as [21]:

$$C_{max} = \frac{I_{peak}}{\omega_L V_{peak}} \tan(\theta) = \frac{\left(500\sqrt{2}/220\right)}{314x311} \tan(1') = 574.5nF \quad (11)$$

where I_{peak} is the peak input current, V_{peak} is the peak input voltage and θ is the displacement angle.

The value of the filter capacitance C_f is selected such that C_f is lower than C_{max}. Hence the value of C_f is selected as 330nF.

The expression for the calculation of the filter inductance L_f is given as [21]:

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} = \frac{1}{4\pi^2 \left(45000/10\right)^2 x\,330x10^{-9}} = 3.79mH \quad (12)$$

where f_c is the cut-off frequency such that $f_c=f_s/10$ [21]. Hence the filter inductance is selected as 4mH.

IV. Control of the BIFRED Converter Fed BLDC Motor Drive

The function of the control unit of the BIFRED converter is to generate the PWM (Pulse Width Modulated) signals for switch S_w to control the DC link voltage at a desired value. An inherent power factor correction is achieved since the converter is designed to operate in DCM utilizing a voltage follower approach. The control scheme of the proposed BIFRED converter based VSI fed BLDC motor drive consists of a reference voltage generator, a voltage error generator, a voltage controller and a PWM generator, as shown in Fig. 1.

A. Reference Voltage Generator

The reference DC link voltage V_{dc}* is generated by multiplying the reference speed N* with the motor's voltage constant k_v as:

$$V_{dc}^* = k_v N^* \quad (13)$$

B. Voltage Error Generator

The reference DC link voltage V_{dc}* is compared with the sensed DC link voltage Vdc to generate a voltage error signal V_e. This voltage error signal is then given to the PI (Proportional-Integral) controller for the necessary control action. The error voltage V_e is given as:

$$V_e = V_{dc}^* - V_{dc} \quad (14)$$

C. Voltage Controller

A voltage PI controller produces a controlled output V_c from the voltage error V_e for the necessary control action. The controller output V_c at any sampling instant k is given as:

$$V_c(k) = V_c(k-1) + K_p\{V_e(k) - V_e(k-1)\} + K_i V_e(k) \quad (15)$$

where K_p and K_i represent the proportional and integral gains of the voltage PI controller, respectively.

D. PWM Generator

A PWM signal is generated by comparing the voltage controller output V_c with a high frequency saw-tooth waveform $m_d(t)$. This PWM signal is given to the MOSFET of the BIFRED converter. The switching function is defined as:

$$\text{If } m_d(t) < V_c(t) \text{ then } S_w = 1 \text{ else } S_w = 0 \quad (16)$$

where '1' and '0' represent the 'on' and 'off' conditions of the switch, respectively.

V. Modeling of the BIFRED Converter Fed BLDC Motor Drive

The modeling of the BLDC motor drive is classified into modeling of the BLDC motor, the VSI and the electronic commutation for the operation of the BLDC motor. The speed and current derivative equations of the BLDC motor are obtained to derive its mathematical model. The section "VSI" describes the voltage applied by the VSI to the BLDC motor in different switching states. Moreover, the switching sequence of the different switches of the VSI depending upon the rotor position as sensed by Hall sensors is given in the section "Electronic Commutation". Fig. 4 shows the VSI fed BLDC motor drive.

A. BLDC Motor

For a three phase star connected BLDC motor, the per phase voltages (V_{an}, V_{bn} and V_{cn}) of the BLDC motor are given as [7, 22]:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = R_s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} p \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} \quad (17)$$

where i_{an}, i_{bn} and i_{cn} are the phase currents, e_{an}, e_{bn} and e_{cn} are

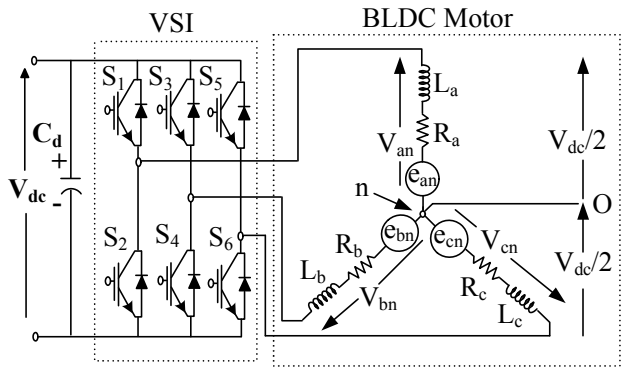


Fig. 4. A BLDC motor fed by a VSI.

the per phase back emf's, R_s is the per phase resistance, L and M are the self and mutual inductance of the stator's winding, respectively, and p is the differential operator.

For a three phase star connected BLDC motor:

$$i_{an}+ i_{bn}+ i_{cn}=0 \tag{18}$$

The V-A relation obtained after substituting equation (18) into equation (17) is:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = R_s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix} p \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} + \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} \tag{19}$$

Using equation (19), the currents derivative are obtained as:

$$p\begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} = \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix}^{-1} \left(\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} - \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix} - R_s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{an} \\ i_{bn} \\ i_{cn} \end{bmatrix} \right) \tag{20}$$

The electromagnetic torque Te is given as [7, 22]:

$$T_e = \frac{\sum (e_{xn} i_{xn})}{\omega_r} \tag{21}$$

where ω_r represents the rotor speed, x represent phase a, b or c and n represents the neutral terminal. This expression faces computational difficulty at zero speed. Hence to overcome this, e_{xn} is defined as [7, 22]:

$$e_{xn} = f_{xn}(\theta)\lambda_x \omega_r \tag{22}$$

where λ_x represents the flux and the functions $f_{xn}(\theta)$ have the same shape as the back emf. Substituting equation (22) into equation (21):

$$T_e = \lambda_x \sum f_{xn}(\theta) i_{xn} \tag{23}$$

The torque balance equation is given as [7, 22]:

$$T_e - T_l = J\frac{d\omega_r}{dt} + B\omega_r \tag{24}$$

where T_l is load torque, J is the moment of inertia of the motor and B is the frictional constant.

Using equation (24), the speed derivative is expressed as:

TABLE I

SWITCHING SEQUENCE OF BLDC MOTOR FOR ELECTRONIC COMMUTATION BASED ON THE VIRTUAL HALL SIGNAL

θ (^{0})	Hall Signal			Switching Sequence					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

$$p\omega_r = \frac{(T_e - T_l - B\omega_r)}{J} \tag{25}$$

And finally, as shown in Fig. 4, the neutral voltage V_{no} with respect to point 'o' is given as [22]:

$$V_{no} = \{V_{ao} + V_{bo} + V_{co} - (e_{an} + e_{an} + e_{an})\}/3 \tag{26}$$

Equations (17)-(26) shown above describes the dynamic model of the BLDC motor:

B. Voltage Source Inverter

From Fig. 4, the output voltage of the inverter of phase 'a' with respect to the potential at point 'o' is given as:

$V_{ao} = V_{dc}/2$ for S_1=1 (27)

$V_{ao} = -V_{dc}/2$ for S_2=1 (28)

$V_{ao} = 0$ for S_1=0, S_2=0 (29)

where '1' and '0' represent the 'on' and 'off' conditions of the IGBT's, respectively.

C. Electronic Commutation

The switching sequence of the VSI is the state of the switches for a particular rotor position of the BLDC motor as sensed by the Hall Effect position sensor. The turn on and turn off conditions of the IGBT's are represented as '1' or '0', respectively. The switching sequence of the VSI for different positions of the rotor is shown in Table-I.

VI. PERFORMANCE EVALUATION

The performance of the proposed drive system is evaluated on the basis of various mechanical and electrical parameters of the BLDC motor and the front end BIFRED converter. The speed (N), the electromagnetic torque (T_e) and the stator current (i_a) of the BLDC motor are estimated for determining the performance of the BLDC motor. Whereas, the electrical parameters such as the DC link voltage (V_{dc}), the boost inductor current (i_{Li}), the magnetizing current of the HFT (i_{Lm}) and the voltage across the bulk capacitor (v_{Cb}) are shown for the satisfactory performance of the BIFRED converter. Moreover, the supply voltage (v_s) and the supply current (i_s)

determine the performance in terms of the power quality of the drive. Parameters such as the THD (Total Harmonic Distortion), the DPF (Displacement Power Factor), the PF (Power Factor) and the CF (Crest Factor) of the supply current are used for the power quality assessment. The switch voltage (v_{sw}) and the switch current (i_{sw}) are also determined for deciding the rating of the MOSFET to be used for designing the BIFRED converter.

Fig. 5 shows the performance of the proposed drive at the rated DC link voltage and the rated load. The supply current obtained is sinusoidal and in phase with the supply voltage. The currents i_{Li} and i_{Lm} are discontinuous, as shown in Fig. 5, thus verifying the dual DCM operation of the BIFRED converter. The switch peak voltage and the peak current are around 700V and 22A, respectively. These are both quite acceptable for designing a 500W system. Table-II shows the performance of the proposed drive under speed control from 30V to 130V. The THD of supply current is found below 5% and the power factor is above 0.99 over the entire range of speed control. This is under the acceptable limits imposed by IEC 61000-3-2.

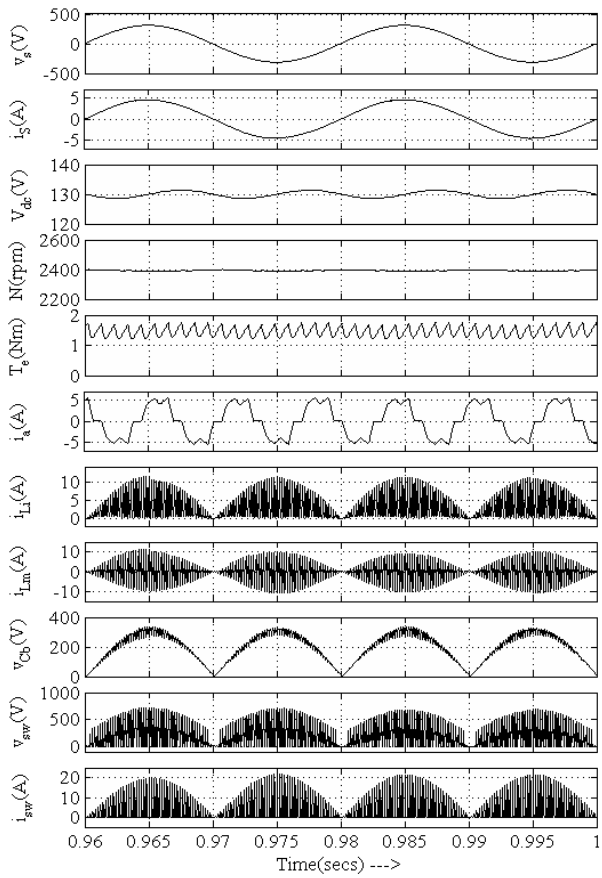


Fig. 5. Performance of BIFRED converter fed BLDC motor drive at rated DC link voltage and rated load.

Performance of the proposed drive system is also evaluated for dynamic conditions. Fig. 6 shows the performance during

TABLE II

PERFORMANCE OF BIFRED CONVERTER FED BLDC MOTOR DRIVE FOR SPEED CONTROL

V_{dc} (V)	Speed (rpm)	THD of I_s (%)	DPF	PF	I_s (A)
30	230	3.28	0.9977	0.9972	1.006
40	460	3.08	0.9986	0.9981	1.222
50	690	2.86	0.9991	0.9987	1.431
60	910	2.62	0.9995	0.9992	1.635
70	1125	2.29	0.9997	0.9994	1.839
80	1340	1.84	0.9998	0.9996	2.046
90	1550	1.49	0.9999	0.9998	2.262
100	1770	1.38	1	0.9999	2.485
110	1980	1.3	1	0.9999	2.715
120	2190	1.27	1	0.9999	2.95
130	2420	1.25	0.9999	0.9998	3.236

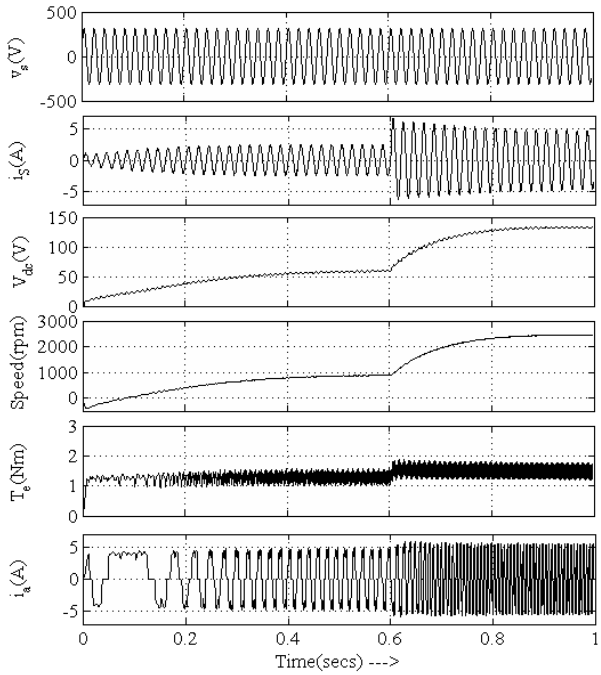


Fig. 6. Dynamic performance during starting and speed change of BIFRED converter fed BLDC motor drive.

start-up and speed control, which is obtained quite satisfactory with smooth control. Fig. 7 shows the supply current and its harmonic spectrum at the rated voltage and the rated loading condition. The performance of drive is also evaluated while varying supply voltage from 170V-270V to demonstrate the satisfactory performance under practical situations and it is tabulated in Table-III.

The switch peak voltage (v_{sw}), the switch peak current (i_{peak}) and the switch rms current (i_{rms}) are tabulated in Table-IV for different loadings on the BLDC motor. The peak voltage and the peak current on the switch are used for determining the rating of the switch and the rms current flowing through the switch which decides the thermal rating of the heat sink to be

TABLE III

POWER QUALITY PARAMETERS OF PROPOSED SYSTEM WITH INPUT AC VOLTAGE VARIATION

V_s (V)	THD of I_s (%)	DPF	PF	I_s (A)	CF
170	0.82	0.9982	0.9982	4.12	1.414
180	0.88	0.9992	0.9992	3.912	1.414
190	0.97	0.9995	0.9995	3.7	1.414
200	0.99	0.9997	0.9997	3.509	1.414
210	1.14	0.9999	0.9998	3.339	1.414
220	1.25	0.9999	0.9998	3.236	1.414
230	1.27	1	0.9999	3.046	1.414
240	1.28	1	0.9999	2.916	1.414
250	1.4	1	0.9999	2.8	1.414
260	1.45	0.9999	0.9998	2.689	1.414
270	1.58	0.9998	0.9997	2.59	1.414

TABLE IV

VOLTAGE AND CURRENT STRESS ON SWITCH ON DIFFERENT LOADING CONDITION

Load	V_p (V)	I_p (A)	I_{rms} (A)
10	680	13	0.48
20	680	14	0.54
30	680	15	0.62
40	690	16	0.76
50	690	17	0.812
60	690	18	0.919
70	690	19	1.06
80	700	20	1.14
90	700	21	1.27
100	700	22	1.485

designed. Fig. 8 shows the variation of the THD of the supply current and the power factor with the DC link voltage (Fig. 8 (a)) and the supply voltage (Fig. 8 (b)), respectively. The characteristics obtained show that the power quality indices are within the recommended limits by IEC 61000-3-2. Thus an improved power quality is achieved for a wide range of speed control and supply voltage variations.

VII. CONCLUSION

A BIFRED converter of an IHQRR family has been used for improved power quality operation of a BLDC motor drive. A BIFRED converter fed VSI based BLDC motor drive has been proposed for speed control using a single voltage sensor. A BIFRED converter operating in dual DCM has been utilized as a front end converter for power factor correction and DC link voltage control. The electronic commutation of the BLDC motor, which utilizes fundamental frequency switching of the VSI, has been used for obtaining reduced switching losses in the VSI. Improved power quality operation for a wide range of speed control has been obtained. It is under the recommended limits by international power quality standards such as IEC 61000-3-2. Satisfactory performance of the drive has also been obtained for varying supply voltages to demonstrate the behavior in practical situations. Moreover, the switch stress has also been analyzed for determining the switch rating and the size of heat sink. The proposed converter topology has been found to be suitable for the design of a high performance BLDC motor drive with improved power quality at the AC mains.

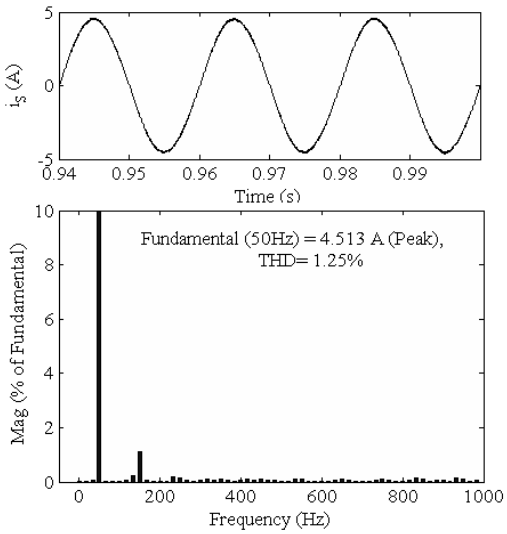
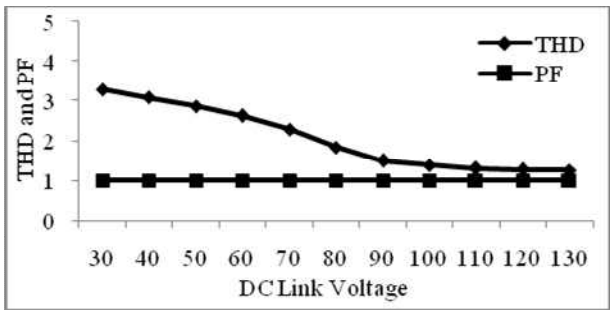
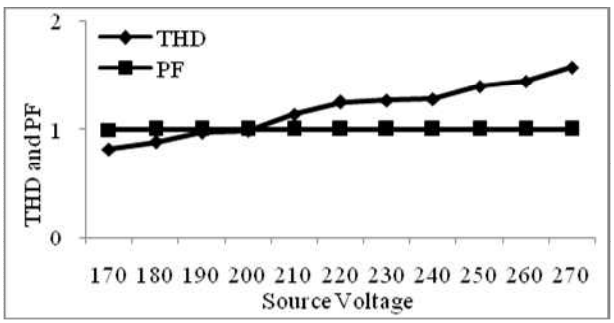


Fig. 7. AC mains current and its harmonic spectrum at rated voltage.



(a)



(b)

Fig. 8. THD of AC mains current and PF with varying DC link voltage (Fig. 8(a)) and varying supply voltage (Fig. 8(b)).

APPENDIX

BLDC Motor Rating: 4 pole, P_{rated} (Rated Power) = 0.5 HP (377 W), V_{rated} (Rated DC link Voltage) = 130 V, T_{rated} (Rated Torque) = 1.2 Nm, ω_{rated} (Rated Speed) = 3000 rpm, K_b (Back EMF Constant) = 34 V/krpm, K_t (Torque Constant) = 0.32 Nm/A, R_{ph} (Phase Resistance) = 2.68 Ω, L_{ph} (Phase Inductance) = 5.31 mH, J (Moment of Inertia) = 1.3 kg-cm^2.

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