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# Improvement of the Performance of the Cascaded Multilevel Inverters Using Power Cells with Two Series Legs

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**Abstract**

A modular three-phase multilevel inverter especially suitable for electrical drive applications has been previously presented. This topology is based on series connection of power cells in which each cell comprised of two inverter legs in series. In this paper, in order to generate the maximum number of voltage levels with reduced number of switches, three algorithms are proposed for determination of the magnitudes of dc voltage sources. In addition, a new hybrid multilevel inverter is proposed that is composed of series connection of the previously presented multilevel inverter and some H-bridges. The proposed topology has been compared with some other presented multilevel inverters. The performance of the proposed multilevel inverter has been verified by simulation and experimental results of a single-phase 39-level multilevel inverter.

**Key words:** Cascaded multilevel inverter, Cells with two series legs, Hybrid multilevel inverter

## I. INTRODUCTION

In general, multilevel inverters are divided into three main categories: the diode-clamped [2], the flying capacitor [3], and the cascaded H-bridge (CHB) multilevel inverters [4]. Among these inverters, the diode-clamped multilevel inverters need to use complex PWM control methods and a large number of diodes and capacitors. In flying capacitor multilevel inverters, less elements are needed but demands more large size capacitors. The CHB multilevel inverters are composed of series connections of single-phase H-bridge power cells. There is a good attention to CHB multilevel inverters due to their simple control and modularity topology. The CHB multilevel inverter is a popular topology and is utilized in various applications such as high-power medium-voltage drives [5] and reactive power compensation [6] due to low electromagnetic interference and high efficiency with low-frequency switching control method. The main disadvantage of the cascaded multilevel inverters is their need for the large number of switches.

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Some of the cascaded multilevel inverters have been developed to use unequal dc bus voltages [7] or a single dc voltage source [8]. This shows the possibility of different implementations for this topology. In recent years, new topologies of multilevel inverters have been presented [9]-[11].

Standard cascaded multilevel inverters require $n$ dc voltage sources for $2n+1$ levels. In [12], a CHB multilevel inverter has been presented which uses only one dc voltage source. This topology is referred as a hybrid cascaded H-bridge multilevel inverter (HCMLI). A HCMLI uses only a single dc voltage source for each phase. This feature is useful for high-power motor drive applications as it significantly decreases the number of required dc source. Due to the usage of the fundamental frequency control method, HCMLI has the high conversion efficiency and low thermal stress.

A new topology of cascaded multilevel inverter with a reduced number of switches and insulated gate driver circuits has been presented in [9]. It is important to mention that the presented topology in [9] needs four high rating switches for the output side of the H-bridge inverter.

An alternative three-phase cascaded multilevel inverter topology has been presented in [13]. It has been used power cells connected in cascade using two inverter legs in series, instead of two parallel inverter legs, as conventionally found in CHB power cells. Also another new cascaded hybrid

H-bridges (CHHB) has been presented in [13]. It has been used cascaded multilevel inverter with half bridge and full bridge cells in series. The large number of dc voltage sources and switches are disadvantages for those structures that increases the total cost of the inverter.

A new cascade multilevel inverter topology has been presented in [14]. It has been based on the series connection of half and full bridge inverter cells and has been provided even-level. This topology cannot produce all voltage levels (odd and even) at the output of the multilevel inverter and this is the main disadvantage of this topology

A new three-phase multilevel inverter especially suited for electrical drive applications has been presented in [1]. Unlike the CHB inverters, this topology is based on cascaded power cells where each cell utilizes two series inverter legs. The high number of dc voltage sources in presented topology in [1] is a disadvantage because it increases the total cost of the inverter.

In this paper, an overview is taken over the presented structure in [1] and in order to generate the maximum number of voltage levels at the output with the minimum number of dc voltage sources and switches, three algorithms are proposed for determination of the magnitudes of dc voltage sources. In addition, a new topology is proposed that is composed of the presented multilevel in [1] and the cascaded H-bridges. Finally, the paper includes the simulation and experimental results of a single-phase 39-level multilevel inverter to prove the feasibility of the proposed multilevel inverter.

## II. Review on the Recommended Topology

Fig. 1 shows the cell that has been used in the topology presented in [1]. This cell consists of two inverter legs that are connected in series. In this topology, there is no need for bidirectional switches from viewpoint of voltage blocking. Therefore, an insulated-gate bipolar transistor (IGBT) with anti-parallel diode can be used as a power switch. The leg voltage magnitudes in the multicell presented in [1] are as follows:

$$V_{cell\,1,1} = V_{cell\,1,2} = V_{dc} \tag{1}$$

The output voltage of the power cell shown in Fig. 1, includes three levels $+V_{dc}$, 0, and $-V_{dc}$. When the switches $S_1$ and $S_2$ are turned on, $+V_{dc}$ is produced at the output ($v_o(t)$). In a similar manner, when $S_1'$ and $S_2'$ are turned on, $-V_{dc}$ is generated at the power cell output. Considering Fig. 1, the upper leg generates $-V_{dc}$ and the lower leg produces $+V_{dc}$. The zero level can be generated by two methods in the structure shown in Fig. 1. When the switches $S_1$ and $S_2'$ or $S_1'$ and $S_2$ are turned on, the zero level is produced at the output. Table I shows the permitted states of the switches for different levels of output voltage.

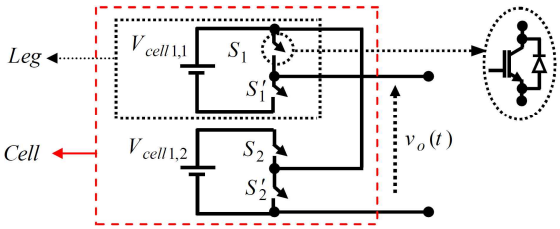


Fig. 1. Power cell presented in [1] with three-level output voltage.

TABLE I

Permitted States of the Switches for Different Values of Output Voltage for Power Cell Shown in Fig. 1

| States | Switches states | | | | $v_o$ |
|---|---|---|---|---|---|
| | $S_1$ | $S_1'$ | $S_2$ | $S_2'$ | |
| 1 | on | off | on | off | $+V_{dc}$ |
| 2 | off | on | off | on | $-V_{dc}$ |
| 3 | on | off | off | on | 0 |
| 4 | off | on | on | off | 0 |

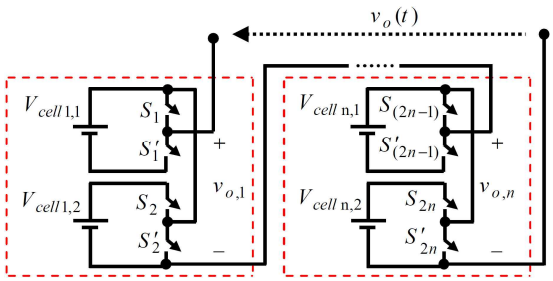


Fig. 2. $2n+1$-level inverter composed of $n$ series cell.

A $2n+1$ multilevel inverter can be composed of $n$ power cells as shown in Fig. 2. As seen in Fig. 2, each cell includes two dc voltage sources and four IGBTs. The number of voltage levels at the output ($N_{step}$), number of dc voltage source ($N_{source}$), and number of IGBTs ($N_{IGBT}$) can be calculated as follows, respectively:

$$N_{step} = 2n+1 \tag{2}$$

$$N_{source} = 2n \tag{3}$$

$$N_{IGBT} = 4n \tag{4}$$

where $n$ is the number of cells.

## III. Proposed Algorithms for Determination of Magnitudes of DC Voltage Sources

In order to produce more voltage levels and also all voltage levels (odd and even) at the output of multilevel inverter

presented in [1] with the minimum number of switches, three algorithms for determination of magnitudes of dc voltage sources are proposed. In all of the proposed algorithms, the magnitude of $V_{cell\,1,1}$ is considered as the base value ($1\,pu$) for the per-unit system.

*A. First Proposed Algorithm*

According to the first proposed algorithm, the magnitudes of the dc voltage sources in each cell are chosen as follows:

**Cell 1:**

$$V_{cell\,1,1}=V_{cell\,1,2}=1 \tag{5}$$

**Cell 2:**

$$V_{cell\,2,1}=V_{cell\,2,2}=2 \tag{6}$$

**Cell 3:**

$$V_{cell\,3,1}=V_{cell\,3,2}=4 \tag{7}$$

**Cell n:**

$$V_{cell\,n,1}=V_{cell\,n,2}=(2^{n-1}) \tag{8}$$

Table II shows the number of voltage levels, the number of required dc voltage sources and IGBTs for the topology shown in Fig. 2 where the magnitudes of the dc voltage sources have been chosen according to the first proposed algorithm. Considering Table II, the number of voltage levels for $n$ cells can be calculated as follows:

$$N_{step}=2^{n+1}-1 \tag{9}$$

*B. Second Proposed Algorithm*

In order to have unequal values for $v_o$ in Fig. 2 and to be produced at all levels, the values of the dc voltage sources in each cell are recommended according to the following algorithm:

**Cell 1:**

$$V_{cell\,1,1}=V_{cell\,1,2}=1 \tag{10}$$

**Cell 2:**

$$V_{cell\,2,1}=V_{cell\,2,2}=3 \tag{11}$$

**Cell 3:**

$$V_{cell\,3,1}=V_{cell\,3,2}=9 \tag{12}$$

**Cell n:**

$$V_{cell\,n,1}=V_{cell\,n,2}=(3^{n-1}) \tag{13}$$

Table III shows the number of voltage levels, number of required dc voltage sources, and IGBTs for the topology shown in Fig. 2 so that the magnitudes of the dc voltage sources have been chosen according to the second proposed algorithm. Considering Table III, the number of voltage levels for $n$ cells can be calculated as follows:

$$N_{step}=3^{n} \tag{14}$$

TABLE II

THE NUMBER OF LEVELS, REQUIRED DC VOLTAGE SOURCES, AND IGBTS FOR FIRST PROPOSED ALGORITHM

| $n$ | $N_{step}$ | $N_{source}$ | $N_{IGBT}$ |
|---|---|---|---|
| 1 | 3 | 2 | 4 |
| 2 | 7 | 4 | 8 |
| 3 | 15 | 6 | 12 |
| 4 | 31 | 8 | 16 |
| ⋮ | ⋮ | ⋮ | ⋮ |
| $n$ | $2^{n+1}-1$ | $2n$ | $4n$ |

TABLE III

THE NUMBER OF LEVELS, REQUIRED DC VOLTAGE SOURCES, AND IGBTS FOR SECOND PROPOSED ALGORITHM

| $n$ | $N_{step}$ | $N_{source}$ | $N_{IGBT}$ |
|---|---|---|---|
| 1 | 3 | 2 | 4 |
| 2 | 9 | 4 | 8 |
| 3 | 27 | 6 | 12 |
| 4 | 81 | 8 | 16 |
| ⋮ | ⋮ | ⋮ | ⋮ |
| $n$ | $3^{n}$ | $2n$ | $4n$ |

*C. Third Proposed Algorithm*

Considering Fig. 1, the upper leg produces $-V_{dc}$, and the lower leg produces $+V_{dc}$. In order to produce the maximum number of voltage levels at the output of topology shown in Fig. 2, by the minimum number of IGBTs, the magnitudes of the dc voltage sources can be determined according to the third proposed algorithm. In this algorithm, by using trial and error method, the magnitude of the dc voltage sources for the first and second cells are determined $1^{pu}$, $2^{pu}$, $5^{pu}$, and $4^{pu}$, respectively. The generated levels by these two cells are: $0$, $\pm1$, $\pm2$, $\pm3$, $\pm4$, $\pm5$, and $\pm6$.

For calculating the magnitudes of the other dc voltage sources, the following definitions are considered:

$$\text{Upper leg's dc voltege source for the new cell in per unit} = V_{new,1} \tag{15}$$

$$\text{Lower leg's dc voltage source for the new cell in per unit} = V_{new,2} \tag{16}$$

$$\text{The number of positive levels generated by previous cells} = L_{\max} \tag{17}$$

$$\text{The first generated level in per unit after the joining of the new cell} = B \tag{18}$$

It is clear that the following equation is satisfied between $L_{max}$ and $B$ :

$$B = L_{\max} + 1 \tag{19}$$

In order to produce the all voltage levels (odd and even) at the output of the multilevel inverter shown in Fig. 2, the calculation of the magnitudes of dc voltage sources for the other cells ( $n \geq 3$ ) are expressed as follows:

*1) First Method:* In order to obtain the magnitude of lower leg's dc voltage source for new cell, the following equation is considered:

$$V_{new,2} - L_{\max} = B \tag{20}$$

Considering (19) and (20), the following equation is obtained:

$$V_{new,2} = 2L_{\max} + 1 \tag{21}$$

As mentioned previously, the upper leg of the cell produces negative voltage level. It means that, the upper leg of the new cell produces $-V_{new,1}$. In order to obtain the magnitude of upper leg's dc voltage source for new cell, the following equation is considered:

$$-V_{new,1} + L_{\max} = -B \tag{22}$$

Considering (19) and (22), the following equation is obtained:

$$V_{cell\,new,1} = 2L_{\max} + 1 \tag{23}$$

From (21) and (23), we can write:

$$V_{new,1} = V_{new,2} \tag{24}$$

For examples, in the third cell $L_{\max} = 6$ and $B = 7$. According to (21), the magnitude of lower leg's dc voltage source for new cell can be obtained as follows:

$$V_{new,2} = 13 \tag{25}$$

According to (24), the magnitude of upper leg's dc voltage source for new cell can be calculated as follows:

$$V_{new,1} = V_{new,2} = 13 \tag{26}$$

Therefore, $V_{new,1}$ and $V_{new,2}$ for the third cell is obtained $13^{pu}$. The equations (21) and (24) can be used for the determination of the magnitudes of dc voltage sources in other cells.

*2) Second Method:* If the summation of the lower legs' dc voltage sources magnitudes is shown by $V_m$, the following equation is satisfied:

$$V_m = L_{\max} \tag{27}$$

To determine the number of output voltage levels, the following definitions are considered:

$$\text{The number of voltage levels for the first cell} = N_{step}(1) \tag{28}$$

$$\text{The number of voltage levels for other cells } (n \geq 2) = N_{step}(n) \tag{29}$$

The number of output voltage levels for the first cell is

$$N_{step}(1) = 3 \tag{30}$$

The number of output voltage levels for the other cells $(n \geq 2)$ can be calculated by

$$N_{step}(n) = 2V_m + 1 \tag{31}$$

Considering (27), (21) can be rewritten as follows:

$$V_{new,2} = 2V_m + 1 \tag{32}$$

As can be seen, the right sides of (31) and (32) are equal to each other. Therefore,

$$V_{new,2} = N_{step}(n) \tag{33}$$

The equation (33) means that $V_{new,2}$ is equal to the number of output voltage levels obtained from previous cells. For example, for two cells the summation of the lower legs' dc voltage sources magnitudes is

$$V_m = 6 \tag{34}$$

From (31), the number of voltage levels is 13.

$$N_{step}(2) = 13 \tag{35}$$

From (33) and (24), the values of the dc voltage sources for the next cell (i.e. third cell) are given as follows:

$$V_{new,1} = V_{new,2} = 13 \tag{36}$$

In order to calculate $V_{new,2}$, (21) or (33) can be used. In addition, $V_{new,1}$ is obtained from (24). Table IV shows the number of voltage levels, the number of required dc voltage sources, and IGBTs for the topology shown in Fig. 2 so that the magnitudes of the dc voltage sources have been chosen according to the third proposed algorithm. The number of output voltage levels can be calculated as follows:

$$N_{step} = 13 \times 3^{n-2} \tag{37}$$

The above equation is true for $n \geq 2$, where $n$ shows the number of cells.

Considering the previous discussion, the magnitudes of dc voltage sources for $n \geq 3$ can be calculated as follows:

$$V_{cell\,n,1} = V_{cell\,n,2} = 13 \times 3^{n-3} \tag{38}$$

The above equation is true for $n \geq 3$.

TABLE IV

THE NUMBER OF LEVELS, REQUIRED DC VOLTAGE SOURCES, AND IGBTS FOR THIRD PROPOSED ALGORITHM

| $n$ | $N_{step}$ | $N_{source}$ | $N_{IGBT}$ |
|---|---|---|---|
| 1 | 3 | 2 | 4 |
| 2 | 13 | 4 | 8 |
| 3 | 39 | 6 | 12 |
| 4 | 117 | 8 | 16 |
| 5 | 351 | 10 | 20 |
| ⋮ | ⋮ | ⋮ | ⋮ |
| $n$ | $13\times3^{n-2}$ | $2n$ | $4n$ |

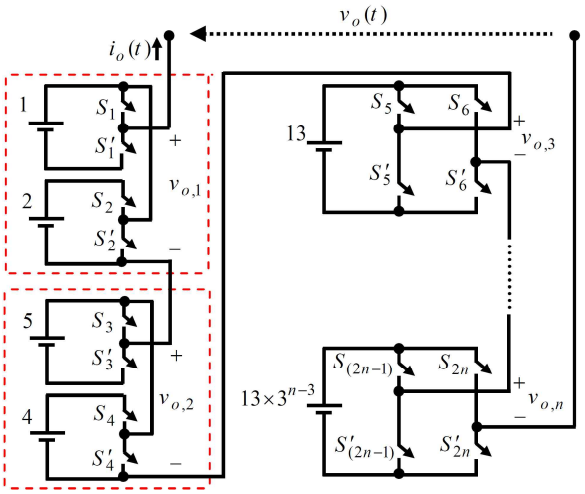


Fig. 3. $13\times3^{n-2}$-level proposed hybrid inverter based on third proposed algorithm.

## IV. PROPOSED TOPOLOGY

Considering (24), the required magnitudes of dc voltage sources for each cell legs' in $n \geq 3$ are equal. Hence, it is possible to used H-bridge inverters instead of power cells. The advantage of this method is that while the number of output voltage levels remains constant, the number of voltage sources is reduced. Fig. 3 shows the proposed hybrid topology. Table V shows the number of voltage levels, the number of required dc voltage sources, and the number of IGBTs for the proposed topology shown in Fig. 3. The magnitudes of the dc voltage sources have been chosen according to the third proposed algorithm. The number of output voltage levels can be calculated from (37).

## V. COMPARISON OF THE PROPOSED TOPOLOGY WITH SOME CONVENTIONAL TOPOLOGIES

In order to show the capabilities of the proposed algorithms and topology, the proposed topology and algorithms are compared with the symmetrical CHB multilevel inverter (CHB1), asymmetrical CHB multilevel

TABLE V

THE NUMBER OF LEVELS, REQUIRED DC VOLTAGE SOURCES, AND IGBTS FOR PROPOSED HYBRID INVERTER BASED ON THIRD PROPOSED ALGORITHM

| $n$ | $N_{step}$ | $N_{source}$ | $N_{IGBT}$ |
|---|---|---|---|
| 1cell | 3 | 2 | 4 |
| 2cell | 13 | 4 | 8 |
| 2cell+1H-bridge | 39 | 5 | 12 |
| 2cell+2H-bridges | 117 | 6 | 16 |
| 2cell+3H-bridges | 351 | 7 | 20 |
| 2cell+4H-bridges | 1053 | 8 | 24 |
| ⋮ | ⋮ | ⋮ | ⋮ |
| 2cell+($n-2$)H-bridges | $13\times3^{n-2}$ | $n+2$ | $4n$ |

inverters (magnitudes of dc voltage sources increase with multiples of 2 and 3 that are shown with CHB2 and CHB3, respectively), and recommended topologies in [1], [13]-[16]. Each switch in the proposed topology [13], [14] and CHB multilevel inverters are composed of one IGBT and one anti-parallel diode. Each switch in the presented topologies in [15] (Fig. 4(a)) and [16] (Fig. 4(b)) is based on bi-directional switches. Fig. 5 shows the comparison results of the number of IGBTs. As this figure shows, the proposed topology needs fewer IGBTs for realizing $N_{step}$ voltage for output. Therefore, the cost of the proposed topology is less than the presented topologies in [1] and [13]-[16] for generating $N_{step}$ voltages at output. It should be noted that the proposed topology as shown in Fig. 3 is the same with the third proposed algorithm and they are identical with each other. Also the second proposed algorithm and third proposed algorithm are the same with CHB2 and CHB3, respectively. The presented topologies in [1], [13], [14], and CHB1 are the identical with each other and they use the same $N_{IGBT}$ to produce realized $N_{step}$. It is important to mention that the structures given in [1], [13], [14] and CHB1 have symmetrical structure. Current and voltage ratings of the switches in a multilevel inverter play important roles in the cost and realization of the multilevel inverter. In the proposed topology, the currents of all switches are equal with the rated current of the load. This is, however, not the case for the voltage. Suppose that peak inverse voltage of all switches ($V_{switch}$) is represented by:

$$V_{switch} = \sum_{j=1} V_{switch,j} \tag{39}$$

In this equation, $V_{switch,j}$ represents the peak voltage of the switches in cell $j$.

Therefore, (39) can be considered as a criterion for the

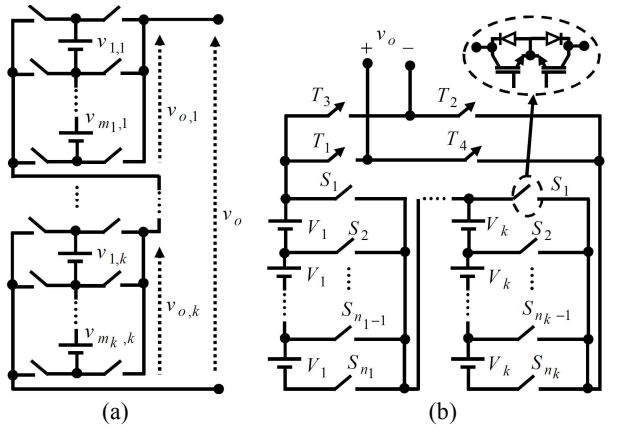


Fig. 4. (a) Recommended topology in [15]; (b) Recommended topology in [16].

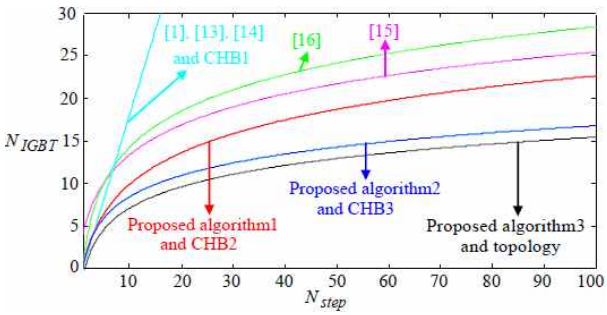


Fig. 5. Variation of $N_{step}$ versus $N_{IGBT}$.

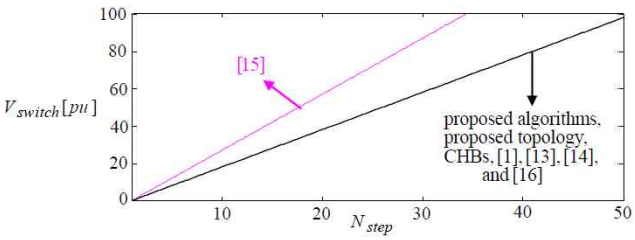


Fig. 6. Variation of $V_{switch}$ versus $N_{step}$.

comparison of different topologies from the maximum voltage standing on the switches [15]. In the proposed multilevel inverter, the voltage standing on switches (in per unit) in Fig. 3 is given by the following equation:

$$V_{switch} = 2(N_{step} - 1) \quad (40)$$

The above equation is true for $n \geq 2$ ($N_{step} \geq 13$).

Fig. 6 compares the standing voltage on switches in the proposed topology with the presented topology in [1], and [13]-[16]. As this figure shows, the standing voltage on switches in the proposed topology is less than that recommended in [15] for realizing $N_{step}$ voltage for $v_o$. Also this figure shows the standing voltage on switches in the proposed topology, symmetrical CHB multilevel inverter, and asymmetrical CHB multilevel inverters, which are recommended topologies in [1], [13], [14] and [16] and are identical with each other.

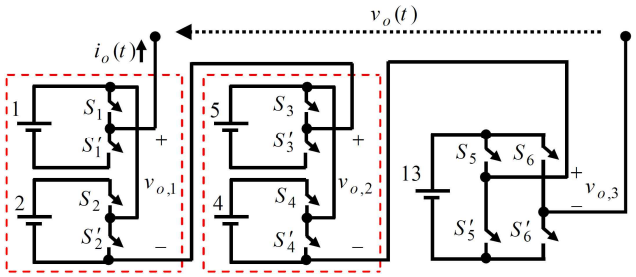

Fig. 7. 39-Level multilevel inverter (according to third method).

## VI. Simulation and Experimental Results

To examine the performance of the proposed topology in the generation of a desired output voltage waveform, a multilevel based on the third proposed algorithm and the proposed hybrid topology is simulated. The PSCAD/EMTDC software has been used for simulation. In the simulation, the switches have been assumed ideal. A typical single-phase proposed hybrid multilevel inverter based on the third proposed algorithm (Fig. 7) with 39 voltage levels and a peak value of $285V$ has been simulated. In this simulation, the base value ($1\,pu$) of voltage source is $15V$ and the number of IGBTs and voltage sources are 12 and 5, respectively.

Also to examine the performance of the proposed multilevel inverter, a single-phase 39-level multilevel inverter prototype is implemented based on the proposed topology shown in Fig. 7. The IGBTs of the prototype are BUP306D with internal anti-parallel diodes. The 89C52 microcontroller by ATMEL has been used to generate the switching patterns. The inverter is fed by independent dc voltage sources with a variable output voltage to adjust the applied input voltages to the converter. For synthesizing dc voltage sources with high magnitudes, multiple small dc voltage sources have been used in series.

The simulation and experimental results are studied in four cases. The first case studies the performance of the proposed topology with R-L load at the output. The second case studies the performance of the proposed topology with the inductive load. The third case studies the performance of the proposed topology with nonlinear load and the fourth case studies the performance of the proposed topology with sudden load change.

### A. First Case Study

The load is a series R-L with the specification of $60\Omega$ and $40mH$, respectively. There are several modulation strategies for multilevel inverters [12], [17], and [18]. In this work, the fundamental frequency switching technique has been used. The benefit of the fundamental frequency switching method is its low switching frequency in comparison with the other control methods. The main idea in the control strategy is to deliver to the load a voltage that minimizes the error with respect to the reference voltage. It is important to note that the calculation of optimal switching

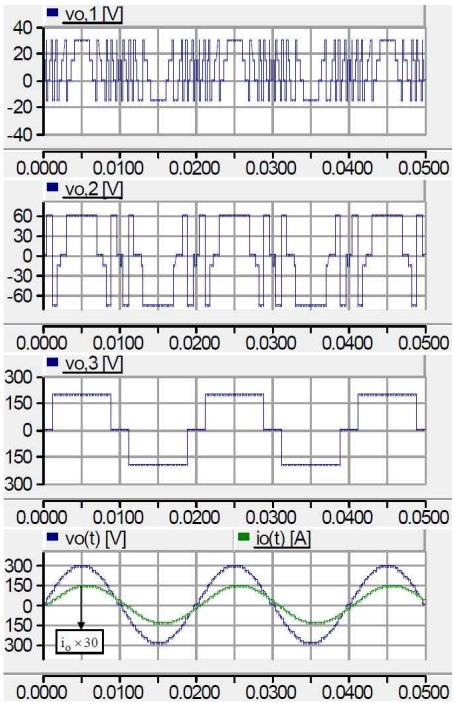


Fig. 8. Simulation results, from top to bottom: the output voltage of each cell, total output voltage and current.

angles for different goals such as elimination of the selected harmonics and minimizing total harmonic distortion (THD) are not the objective of this work. In this paper the fundamental frequency is $50Hz$ . Fig. 8 shows the output voltage of each cell, total output voltage, and output current. The amplitude of the output current is 4.7 A. As can be seen from the waveforms, the output current is almost sinusoidal. Since the load of the converters is almost a low pass filter (R-L), the output current contains less high order harmonics than the output voltages. For this example, the THDs of the output voltage and current based on the simulation are 1.80% and 1.04%, respectively. To generate a desired output with the best quality waveform, the number of the voltage steps should be increased. Fig. 9 shows the experimental results. The experimental results show a good agreement with simulation results. There is a small difference between the amplitudes of the simulation and experimental results due to the voltage drops on switches of the prototype.

### *B. Second Case Study*

The industrial loads are extremely inductive. Hence, the performance of proposed topology is studied for inductive load in this section to show the performance of the proposed topology for all kinds of loads. Fig. 10 shows the experimental results of output voltage and current wave form for an inductive load with $L = 200mH$ . As can be seen in Fig. 10 in which the output current lagging the output voltage by 90 degrees. Fig. 11 verifies the performance of the proposed topology.

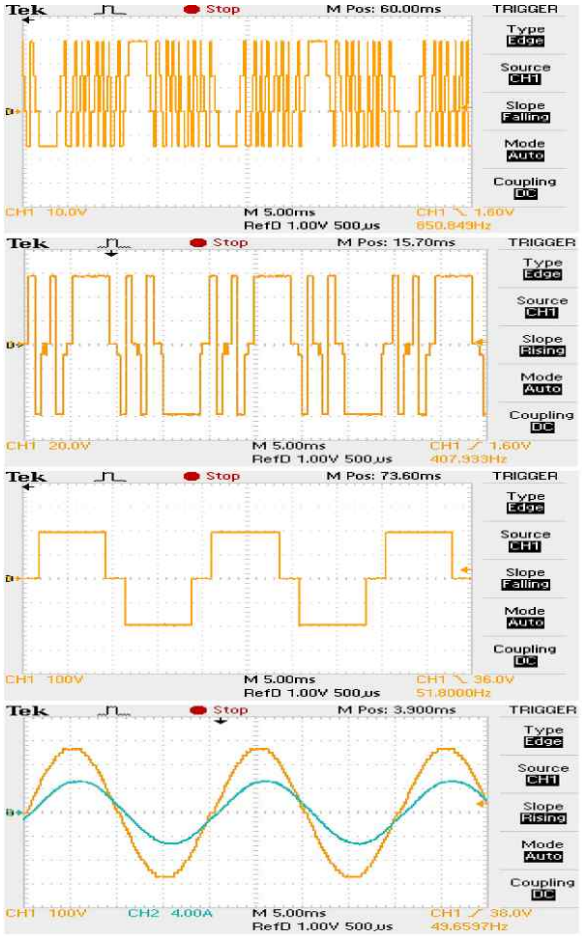


Fig. 9. Experimental results, from top to bottom: output voltage of each cell and output voltage and current.

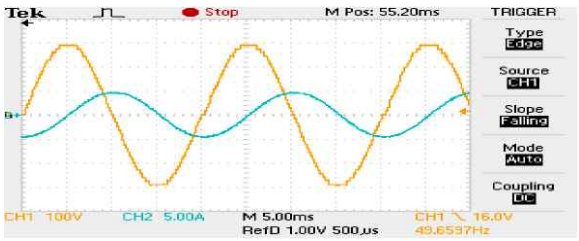


Fig. 10. Experimental results of total output voltage and output current for the inductive load.

### *C. Third Case Study*

The loads that are studied in Sections I and II are linear loads. The nonlinear load is studied to show the performance of the proposed topology in this section. Fig. 11 shows the experimental output voltage and current wave form for a nonlinear load (single-phase half-wave diode rectifier with series $67\Omega - 33mH$ load). As can be seen, the output voltage is the same as the output voltage that is shown in Fig. 8. Fig.12 proves the performance of the proposed topology for nonlinear loads.

### *D. Fourth Case Study*

The performance of the proposed topology is studied for

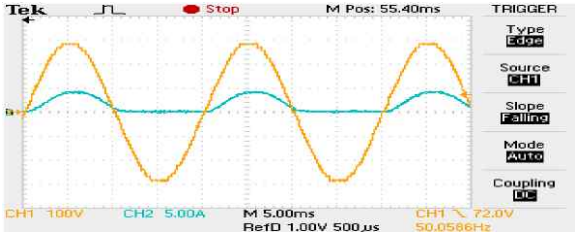


Fig. 11. Experimental results of output voltage and current for the nonlinear load.

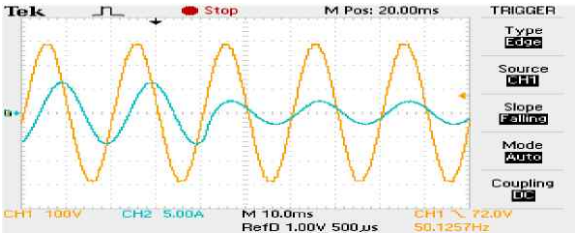


Fig. 12. Experimental results of output current for sudden load changing.

linear and nonlinear loads. The performance of the proposed topology is studied for sudden load changes in this section to show the performance during load perturbation. At first the load is a series of $28\Omega-122mH$ and then the load is changed to a series of $100\Omega-104mH$ . Fig. 12 shows experimental results of the output voltage and current for sudden load changes. As can be seen in Fig. 12 when the load changes, the minor current distortion is observed. However, the system immediately reaches to its steady state. Fig.13 verifies the performance of the proposed topology for sudden load changes.

## VII. Conclusion

In this paper, three new algorithms for determination of the magnitudes of dc voltage source were proposed for the topology recommended in [1]. These algorithms can provide all steps (odd and even) at the output voltage. A new configuration of the multilevel inverter was proposed. The proposed hybrid topology is composed of the multicell inverter presented in [1] and the H-bridge in series. The magnitudes of dc voltage sources in this proposed topology are chosen according to the third proposed algorithm. The proposed algorithms and topology have been compared with those given in [13]-[16] and CHB multilevel inverters. It was found that the proposed topology provides 351 voltage steps, using 20 IGBTs, where the structure given in [13] produces 11 voltage steps using 20 IGBTs and the structure given in [14] produces 12 voltage steps using 22 IGBTs. As mentioned previously, the structures given in [13] and [14] have symmetrical structure. Also the structure given in [15] produces 53 voltage steps using 22 IGBTs and the structure given in [16] generates 49 voltage steps using 24 IGBTs. The operation and the performance of the third proposed algorithm and proposed topology on a single-phase 39-level multilevel inverter prototype have been studied separately for the $R-L$ , inductive, nonlinear and sudden load changes. The simulation and experimental results verified the proposed algorithm and topology.

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