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Implementation of a ZVS Three-Level Converter with Series-Connected Transformers

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Abstract

This paper studies a soft switching DC/DC converter to achieve zero voltage switching (ZVS) for all switches under a wide range of load condition and input voltage. Two three-level PWM circuits with the same power switches are adopted to reduce the voltage stress of MOSFETs at $V_{in}/2$ and achieve load current sharing. Thus, the current stress and power rating of power semiconductors at the secondary side are reduced. The series-connected transformers are adopted in each three-level circuit. Each transformer can be operated as an inductor to smooth the output current or a transformer to achieve the electric isolation and power transfer from the input side to the output side. Therefore, no output inductor is needed at the secondary side. Two center-tapped rectifiers connected in parallel are used at the secondary side to achieve load current sharing. Due to the resonant behavior by the resonant inductance and resonant capacitance at the transition interval, all switches are turned on at ZVS. Experiments based on a 1*k*W prototype are provided to verify the performance of proposed converter.

Key words: DC/DC converter, Soft Switching

I. INTRODUCTION

Recently, high efficiency DC/DC converters have been widely used and developed for the cloud server power units and telecommunication applications. For the medium/high power applications, three-phase power factor correctors (PFC) are generally used in the front stage of the high efficiency power converters to supply a constant DC bus voltage for the rear stage DC/DC converter. Usually, the DC bus voltage of a three-phase PFC is greater than 500V-800V. Thus, MOSFETs with 500V or 600V voltage stress cannot be adopted in the second stage such as half-bridge or full-bridge circuit topology. High voltage IGBT can be used in the rear DC/DC converters. But the low switching frequency is the main drawback of IGBT for high power density applications. Although MOSFETs with 900V voltage stress can be adopted in the rear DC/DC converters to overcome this problem, the main drawbacks of the high voltage MOSFETs are high cost and large turn-on resistance which will reduce the circuit efficiency. Three-level or multi-level converters/inverters [1]-[4] have been proposed to use low voltage stress of power switches for high voltage applications. These topologies are based on the neutral point diode clamp, flying clamp or series full-bridge topology to reduce the voltage stress of each power switches at one-half of DC bus voltage. Therefore MOSFETs with 600V voltage stress can be used in the rear DC/DC converter for high input voltage applications. Soft switching techniques [5]-[12] such as active clamp techniques, asymmetric half-bridge converters, series resonant techniques and phase-shift pulse-width modulation (PWM) have been proposed in order to meet the demand of modern switching converters with high efficiency, small volume and light weight. Thus, power switches can be turned off at zero current switching (ZCS) or turned on at zero voltage switching (ZVS). However, these soft switching topologies are mainly based on the two-level PWM scheme such that they cannot be used for high voltage applications. Three-level soft switching DC/DC converters [13]-[16] have been proposed to have the features of low voltage stress of power semiconductors and high circuit efficiency. In these techniques, the leakage inductance of the transformer (or external inductance) and the output capacitance of power switches are resonant at the transition interval. The drain-to-source voltage of MOSFETs can be decreased to zero voltage before the MOSFETs are turned on. In order to reduce the output inductance variation due to the different load condition, the output filter inductance is deleted and two

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series transformers [17], [18] are used in the primary side to have the almost constant magnetizing inductance.

This paper presents a soft switching DC/DC converter with two three-level DC/DC circuits with the same power switches. The main features of the proposed converter are low switching losses, ZVS turn-on and low voltage stress on MOSFETs. Two three-level PWM circuits with the same power switches are presented in order to decrease the switch count, achieve the load current sharing, reduce the current stress of the transformer windings, rectifier diodes and output filter inductors and clamp the voltage stress of active switches at $V_{in}/2$. Two center-tapped rectifiers are adopted to reduce the current rating of passive components at the secondary side. For each three-level PWM circuit, the series-connected two transformers are used to smooth load current. One transformer works as a forward-type transformer to transfer the input power to output load, and the other transformer works as an inductor to smooth the load current. Thus no output inductor is needed at the secondary side. Based on the resonant behavior by the output capacitance of MOSFETs and the resonant inductance at the transition interval, all MOSFETs can be turned on at ZVS with a wide range of load current. Experiments with a 1kW prototype are provided to verify the theoretical analysis and demonstrate the effectiveness of the proposed converter.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed converter is shown in Fig. 1. Input capacitances C_{in1} and C_{in2} are equal and large enough to share the input voltage v_{Cin1}=v_{Cin2}=$V_{in}/2$. Switches S_1-S_4 are MOSFETs with the voltage stresses $V_{in}/2$. C_{r1}-C_{r4} are output capacitances of S_1-S_4, respectively. D_a and D_b are the clamped diodes. C_f is the flying capacitor and its voltage is equal to $V_{in}/2$. C_1 and C_2 are the DC blocking capacitances with the average voltages V_{C1}=V_{C2}=$V_{in}/2$. L_{r1} and L_{r2} are the resonant inductances. L_{m1}-L_{m4} are the magnetizing inductances of the transformers T_1-T_4, respectively. D_1-D_4 are the rectifier diodes. R_o and C_o denote the load resistance and output capacitance. Phase-shift PWM scheme is used to regulate the output voltage. S_1 and S_4 are the leading switches and S_2 and S_3 are the lagging switches. Two three-level PWM circuits with the same MOSFETs are adopted in the proposed converter. The components of the circuit 1 include C_{in1}, C_{in2}, D_a, D_b, C_f, S_1-S_4, C_{r1}-C_{r4}, C_1, L_{r1}, T_1, T_2, D_1 and D_2. The circuit 2 includes the components of C_{in1}, C_{in2}, D_a, D_b, C_f, S_1-S_4, C_{r1}-C_{r4}, C_2, L_{r2}, T_3, T_4, D_3 and D_4. Circuit 1 and circuit 2 are operated by the phase shift of one-half of switching cycle. Three voltage levels V_{in}, $V_{in}/2$ and 0 are generated on v_{ab} and v_{bc}. Since the average voltages V_{C1}=V_{C2}=$V_{in}/2$, three voltage levels $V_{in}/2$, 0 and -$V_{in}/2$ are generated on v_{p1} and v_{p2}. However, the voltages v_{p1}=-v_{p2}. Two series transformers are used in each circuit. Each transformer can be operated as

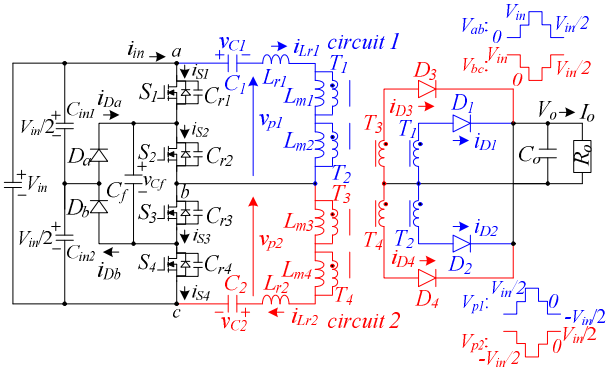


Fig. 1. Proposed new ZVS DC/DC converter.

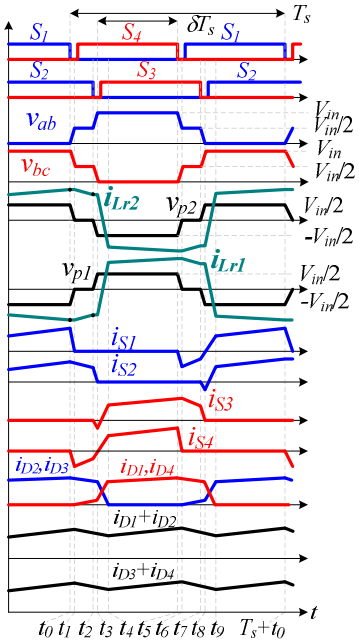


Fig. 2. Key waveforms of the proposed converter.

transformers to achieve electric isolation and power transfer or operated as inductors to smooth output current. Thus, no inductor is needed in the output side.

III. OPERATION PRINCIPLE

The theoretical PWM waveforms of the proposed converter in a switching cycle are given in Fig. 2. Before the discussion the operation principle, some assumptions are made to simplify the system analysis of the proposed converter. (1) Power semiconductors S_1-S_4, D_1-D_4 and D_a-D_b are ideal. (2) Four transformers are identical (L_{m1}=L_{m2}=L_{m3}=L_{m4}=L_m). (3) Resonant inductances are identical L_{r1}=L_{r2}=L_r<<L_m. (4) C_{in1}=C_{in2} are large enough to be considered as two voltage sources V_{Cin1}=V_{Cin2}=$V_{in}/2$. (5) Switch output capacitances C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r. (6) C_1, C_2 and C_f are large enough to be treated as three constant voltages V_{C1}=V_{C2}=V_{Cf}=$V_{in}/2$. (7) The output voltage is constant. Based on the on/off states of S_1-S_4, D_a-D_b and D_1-D_4,

there are ten operation modes in the proposed converter during a switching period. The duty cycle of each switch is equal to 0.5. The PWM signals of S_2 and S_3 are phase-shifted with respective to the PWM signals of S_1 and S_4. Fig. 3 shows the equivalent circuits of ten operation modes in a switching period. Prior to time t_0, S_1, S_2, D_2 and D_3 are conducting.

***Mode 1* [$t_0 \le t < t_1$]:** At t_0, S_1 is turned off. Since $i_{Lr1}(t_0)<0$ and $i_{Lr2}(t_0)>0$, C_{r1} is charged linearly from zero voltage and C_{r4} is discharged linearly from $V_{in}/2$ via the flying capacitor C_f. The rising slope of the drain-to-source voltage of S_1 (or v_{Cr1}) is limited by C_{r1} and C_{r4}. Thus, S_1 is turned off at ZVS. If the energy stored in L_{m1} and L_{m4} is greater than the energy stored in C_{r1} and C_{r4}, then C_{r4} can be discharged to zero voltage. Thus, the ZVS turn-on condition of S_4 is given as:

$$(L_r + L_m)[i_{Lr1}^2(t_0) + i_{Lr2}^2(t_0)] \ge \frac{C_r V_{in}^2}{2} \tag{1}$$

At t_1, $v_{Cr1}=V_{in}/2$ and $v_{Cr4}=0$. The time interval of mode 1 is expressed as:

$$\Delta t_{01} = t_1 - t_0 = \frac{C_r V_{in}}{i_{Lr2}(t_0) - i_{Lr1}(t_0)} \tag{2}$$

The time delay t_d between S_1 and S_4 must be greater than Δt_{01} in order to achieve ZVS turn-on of S_4.

***Mode 2* [$t_1 \le t < t_2$]:** At t_1, $v_{Cr1}=V_{in}/2$ such that D_a is conducting and $v_{Cr4}=0$. Since $i_{Lr1}(t_1)<0$ and $i_{Lr2}(t_1)>0$, the switch current i_{S4} is negative and the anti-parallel diode of S_4 is conducting. Thus, S_4 can be turned on at this moment to achieve ZVS. In this mode, $v_{ab}=v_{bc}=V_{in}/2$ and $v_{p1} \approx v_{Lm1}+v_{Lm2}=v_{Lm3}+v_{Lm4}=0$. Thus, D_1-D_4 are all conducting. The magnetizing voltages of T_1-T_4 are $v_{Lm1}=v_{Lm3}=nV_o$ and $v_{Lm2}=v_{Lm4}=-nV_o$. Diode currents i_{D1} and i_{D4} increase, and i_{D2} and i_{D3} decrease. If the voltage drop on diode D_a and switch S_2 are considered, the primary side currents i_{Lr1} and i_{Lr2} can be expressed as:

$$i_{Lr1}(t) = i_{Lr1}(t_1) + \frac{V_{S2,drop} + V_{Da,drop}}{L_r}(t - t_1) \tag{3}$$

$$i_{Lr2}(t) = i_{Lr2}(t_1) - \frac{V_{S2,drop} + V_{Da,drop}}{L_r}(t - t_1) \tag{4}$$

where $V_{S2,drop}$ and $V_{Da,drop}$ are the voltage drop on switch S_2 and diode D_a, respectively. The slopes of the diode currents are given as:

$$\frac{di_{D1}(t)}{dt} = \frac{di_{D4}(t)}{dt} = \frac{n(V_{S2,drop} + V_{Da,drop})}{2L_r} \tag{5}$$

$$\frac{di_{D2}(t)}{dt} = \frac{di_{D3}(t)}{dt} = -\frac{n(V_{S2,drop} + V_{Da,drop})}{2L_r} \tag{6}$$

where $n=n_p/n_s$ is the turns ratio of T_1-T_4. If the voltage drop on S_2 and diode D_a can be neglected, then the primary currents i_{Lr1} and i_{Lr2} and diode currents i_{D1}-i_{D4} are unchanged in this mode. At time t_2, S_2 is turned off.

***Mode 3* [$t_2 \le t < t_3$]:** S_2 is turned off at t_2. Since $i_{Lr1}(t_2)<0$ and $i_{Lr2}(t_2)>0$, C_{r2} is charged linearly from zero voltage and C_{r3} is discharged linearly from $V_{in}/2$ via the flying capacitor C_f. The rising slope of v_{Cr2} is limited by C_{r2} and C_{r3}. Thus, S_2 is turned off at ZVS. Since D_1-D_4 are still conducting in this mode, the magnetizing voltages $v_{Lm1}=v_{Lm3}=nV_o$ and $v_{Lm2}=v_{Lm4}=-nV_o$. If the energy stored in L_{r1} and L_{r2} is greater than the energy stored in C_{r2} and C_{r3}, then C_{r3} can be discharged to zero voltage. Thus, the ZVS turn-on condition of S_3 is given as:

$$L_r[i_{Lr1}^2(t_2) + i_{Lr2}^2(t_2)] \ge C_r V_{in}^2 / 2 \tag{7}$$

At time t_3, $v_{Cr3}=0$. The time interval in mode 3 is expressed as:

$$\Delta t_{23} = t_3 - t_2 = \frac{C_r V_{in}}{i_{Lr2}(t_2) - i_{Lr1}(t_2)} \tag{8}$$

The time delay t_d between S_2 and S_3 must be greater than Δt_{23} in order to achieve ZVS turn-on of S_3.

***Mode 4* [$t_3 \le t < t_4$]:** At t_3, $v_{Cr3}=0$. Since $i_{S3}(t_3)=i_{Lr1}(t_3)-i_{Lr2}(t_3)<0$, the anti-parallel diode of S_3 is conducting. Thus, S_3 can be turned on at this moment to achieve ZVS. In this mode, the voltages $v_{ab}=V_{in}$, $v_{bc}=0$, $v_{p1}=V_{in}/2$ and $v_{p2}=-V_{in}/2$. Since D_1-D_4 are still conducting, the primary side voltages $v_{Lm1}+v_{Lm2}=0$ and $v_{Lm3}+v_{Lm4}=0$. Thus, the inductor voltages $v_{Lr1}=V_{in}/2$ and $v_{Lr2}=-V_{in}/2$. The primary side currents are illustrated as:

$$i_{Lr1}(t) = i_{Lr1}(t_3) + \frac{V_{in}}{2L_r}(t - t_3) \tag{9}$$

$$i_{Lr2}(t) = i_{Lr2}(t_3) - \frac{V_{in}}{2L_r}(t - t_3) \tag{10}$$

The inductor current i_{Lr1} increases and i_{Lr2} decreases in this mode. The slopes of the diode currents are given as:

$$\frac{di_{D1}(t)}{dt} = \frac{di_{D4}(t)}{dt} = \frac{nV_{in}}{4L_r} \tag{11}$$

$$\frac{di_{D2}(t)}{dt} = \frac{di_{D3}(t)}{dt} = -\frac{nV_{in}}{4L_r} \tag{12}$$

At time t_4, diode currents i_{D2} and i_{D3} are decreased to zero. In this mode, no power is transferred from input voltage source V_{in} to output load R_o. Thus, the duty loss in mode 4 is expressed as:

$$\delta_{loss,4} = \frac{\Delta t_{34}}{T_s} \approx \frac{2L_r I_o f_s}{nV_{in}} \tag{13}$$

where T_s and f_s are the switching period and switching frequency, respectively.

***Mode 5* [$t_4 \le t < t_5$]:** At t_4, $i_{D2}=i_{D3}=0$. T_1 and T_4 are working as the forward type transformers and T_2 and T_3 are working as the inductors to smooth the load current. The voltages $v_{p1}=V_{in}/2$ and $v_{p2}=-V_{in}/2$ in mode 5. Thus, the primary current i_{Lr1} increases linearly with the applied $V_{in}/2$ and i_{Lr2} decreases linearly with the applied voltage $-V_{in}/2$ in this mode.

$$i_{Lr1}(t) \approx i_{Lr1}(t_4) + \frac{V_{in}/2 - nV_o}{L_r + L_m}(t - t_4) \tag{14}$$

$$i_{Lr2}(t) \approx i_{Lr2}(t_4) - \frac{V_{in}/2 - nV_o}{L_r + L_m}(t - t_4) \tag{15}$$

Power is delivered from input voltage source V_{in} to output load R_o in this mode.

***Mode 6* [$t_5 \le t < t_6$]:** At t_5, S_4 is turned off. Since $i_{Lr1}(t_5)>0$ and

$i_{Lr2}(t_5)<0$, C_{r1} and C_{r4} are discharged and charged, respectively, via capacitor C_f. The rising slope of the drain-to-source voltage of S_4 is limited by C_{r1} and C_{r4}. Therefore, S_4 is turned off at ZVS. If the energy stored in L_{m2} and L_{m3} is greater than the energy stored in C_{r1} and C_{r4}, then C_{r1} can be discharged to zero voltage. Thus, the ZVS turn-on condition of S_1 is given as:

$$(L_r + L_m)[i_{Lr1}^2(t_5) + i_{Lr2}^2(t_5)] \geq C_r V_{in}^2 / 2 \quad (16)$$

At time t_6, $v_{Cr1}=0$ and $v_{Cr4}=V_{in}/2$. The time interval in mode 6 is given as:

$$\Delta t_{56} = t_6 - t_5 = \frac{C_r V_{in}}{i_{Lr1}(t_5) - i_{Lr2}(t_5)} \quad (17)$$

The time delay t_d between S_1 and S_4 should be greater than Δt_{56} in order to achieve ZVS turn-on of S_1.

***Mode 7* [$t_6 \leq t < t_7$]:** At time t_6, $v_{Cr4}=V_{in}/2$ such that D_b is conducting and $v_{Cr1}=0$. Since $i_{Lr1}(t_6)>0$ and $i_{Lr2}(t_6)<0$, the switch current i_{S1} is negative and the anti-parallel diode of S_1 is conducting. Thus, S_1 can be turned on at this moment to achieve ZVS. In this mode, the voltages $v_{ab}=v_{bc}=V_{in}/2$ and $v_{p1} \approx v_{Lm1}+v_{Lm2}=v_{Lm3}+v_{Lm4}=0$. Thus, D_1-D_4 are conducting. The primary side currents are expressed as:

$$i_{Lr1}(t) = i_{Lr1}(t_6) - \frac{V_{S3,drop} + V_{Db,drop}}{L_r}(t - t_6) \quad (18)$$

$$i_{Lr2}(t) = i_{Lr2}(t_6) + \frac{V_{S3,drop} + V_{Db,drop}}{L_r}(t - t_6) \quad (19)$$

where $V_{S3,drop}$ and $V_{Db,drop}$ are the voltage drop on switch S_3 and diode D_b, respectively. The slopes of the diode currents are given as:

$$\frac{di_{D1}(t)}{dt} = \frac{di_{D4}(t)}{dt} = -\frac{n(V_{S3,drop} + V_{Db,drop})}{2L_r} \quad (20)$$

$$\frac{di_{D2}(t)}{dt} = \frac{di_{D3}(t)}{dt} = \frac{n(V_{S3,drop} + V_{Db,drop})}{2L_r} \quad (21)$$

Diode currents i_{D1} and i_{D4} decrease and i_{D2} and i_{D3} increase. At time t_7, S_3 is turned off.

***Mode 8* [$t_7 \leq t < t_8$]:** At t_7, S_3 is turned off. C_{r2} and C_{r3} are discharged and charged, respectively. Since the rising slope of v_{Cr3} is limited by C_{r2} and C_{r3}, S_3 is turned off at ZVS. D_1-D_4 are all conducting in this mode, the magnetizing voltages $v_{Lm1}=v_{Lm3}=nV_o$ and $v_{Lm2}=v_{Lm4}=-nV_o$. If the energy stored in L_{r1} and L_{r2} is greater than the energy stored in C_{r2} and C_{r3}, then C_{r2} can be discharged to zero voltage. Thus, the ZVS turn-on condition of S_2 is given as:

$$L_r[i_{Lr1}^2(t_7) + i_{Lr2}^2(t_7)] \geq C_r V_{in}^2 / 2 \quad (22)$$

At time t_8, $v_{Cr2}=0$ and $v_{Cr3}=V_{in}/2$. The time interval of mode 8 is expressed as:

$$\Delta t_{78} = t_8 - t_7 = \frac{C_r V_{in}}{i_{Lr1}(t_7) - i_{Lr2}(t_7)} \quad (23)$$

The time delay t_d between S_2 and S_3 should be greater than Δt_{78} in order to achieve ZVS turn-on of S_2.

***Mode 9* [$t_8 \leq t < t_9$]:** At t_8, $v_{Cr2}=0$. Since $i_{S2}(t_8)=i_{Lr2}(t_8)-i_{Lr1}(t_8)<0$, the anti-parallel diode of S_2 is conducting. Thus, S_2 can be turned on at this moment to achieve ZVS. In mode 9, the voltages $v_{ab}=0$, $v_{bc}=V_{in}$, $v_{p1}=-V_{in}/2$ and $v_{p2}=V_{in}/2$. Since D_1-D_4 are still conducting and $v_{Lm1}+v_{Lm2}=v_{Lm3}+v_{Lm4}=0$, the inductor voltages $v_{Lr1}=-V_{in}/2$ and $v_{Lr2}=V_{in}/2$. The primary side currents and the slopes of the diode currents are given as:

$$i_{Lr1}(t) = i_{Lr1}(t_8) - \frac{V_{in}}{2L_r}(t - t_8) \quad (24)$$

$$i_{Lr2}(t) = i_{Lr2}(t_8) + \frac{V_{in}}{2L_r}(t - t_8) \quad (25)$$

$$\frac{di_{D1}(t)}{dt} = \frac{di_{D4}(t)}{dt} = -\frac{nV_{in}}{4L_r} \quad (26)$$

$$\frac{di_{D2}(t)}{dt} = \frac{di_{D3}(t)}{dt} = \frac{nV_{in}}{4L_r} \quad (27)$$

At t_9, the diode currents i_{D1} and i_{D4} are decreased to zero. The duty loss in mode 9 is expressed as:

$$\delta_{loss,9} = \frac{\Delta t_{89}}{T_s} \approx \frac{2L_r I_o f_s}{nV_{in}} = \delta_{loss,4} \quad (28)$$

***Mode 10* [$t_9 \leq t < t_0+T_s$]:** At t_9, $i_{D1}=i_{D4}=0$. T_2 and T_3 are working as the forward type transformers and T_1 and T_4 are working as the inductors to smooth the load current. The voltages $v_{p1}=-V_{in}/2$ and $v_{p2}=V_{in}/2$ in mode 10. Thus, the primary current i_{Lr1} decreases linearly with the applied $-V_{in}/2$ and i_{Lr2} increases linearly with the applied voltage $V_{in}/2$ in this mode.

$$i_{Lr1}(t) = i_{Lr1}(t_9) - \frac{V_{in}/2 - nV_o}{L_r + L_m}(t - t_9) \quad (29)$$

$$i_{Lr2}(t) = i_{Lr2}(t_9) + \frac{V_{in}/2 - nV_o}{L_r + L_m}(t - t_9) \quad (30)$$

This mode ends at t_0+T_s when S_1 is turned off. The circuit operations of the proposed converter in a switching period are completed.

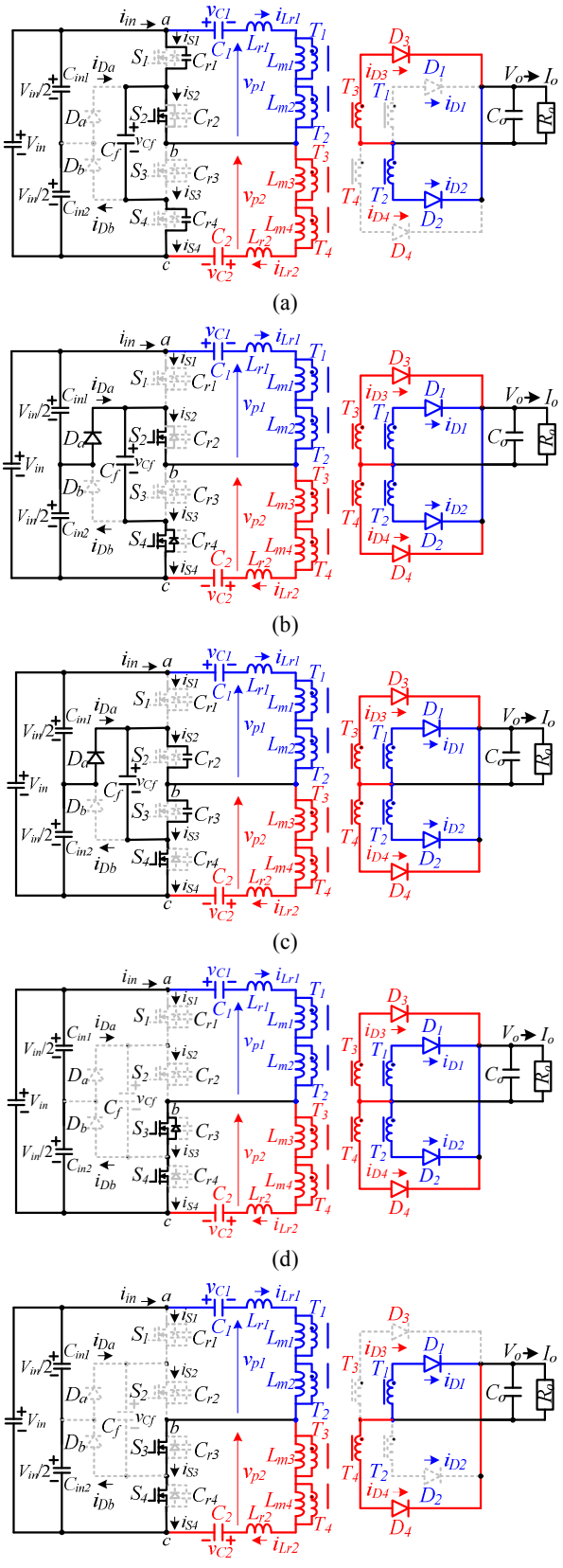
IV. DESIGN CONSIDERATIONS

We neglect the effects of circuit in modes 1, 3, 6 and 8. Only modes 2, 4, 5, 7, 9 and 10 are discussed in this section. The average flying capacitor voltage V_{Cf} is equal to $V_{in}/2$ in modes 2 and 7. Based on the volt-second balance on L_{r1}, L_{m1} and L_{m2}, the average capacitor voltage V_{C1} is also equal to $V_{in}/2$. Similarly, the average capacitor voltage V_{C2} is obtained as $V_{in}/2$. Based on the volt-second balance on L_{m1}, the output voltage can be obtained as:

$$V_o = \frac{V_{in}}{2n}(\delta - \delta_{loss,4}) - V_D = \frac{V_{in}}{2n}(\delta - \frac{2L_r I_o f_s}{nV_{in}}) - V_D \quad (31)$$

where V_D is the voltage drop on diode D_1-D_4, and δ is the duty ratio of the proposed converter when S_1 and S_2 are both in the on-state. The output voltage V_o is related to duty cycle δ, input voltage V_{in}, switching frequency f_s, resonant inductance L_r, turns ratio n and load current I_o. In steady state, the average output diode currents $I_{D1}=I_{D2}=I_{D3}=I_{D4}=I_o/4$. If the

ripple magnetizing current Δi_{Lm1} in mode 10 is less than the diode current reflected to primary side i_{D2}/n, then the ripple inductor current Δi_{Lr1} in mode 10 can be expressed as:



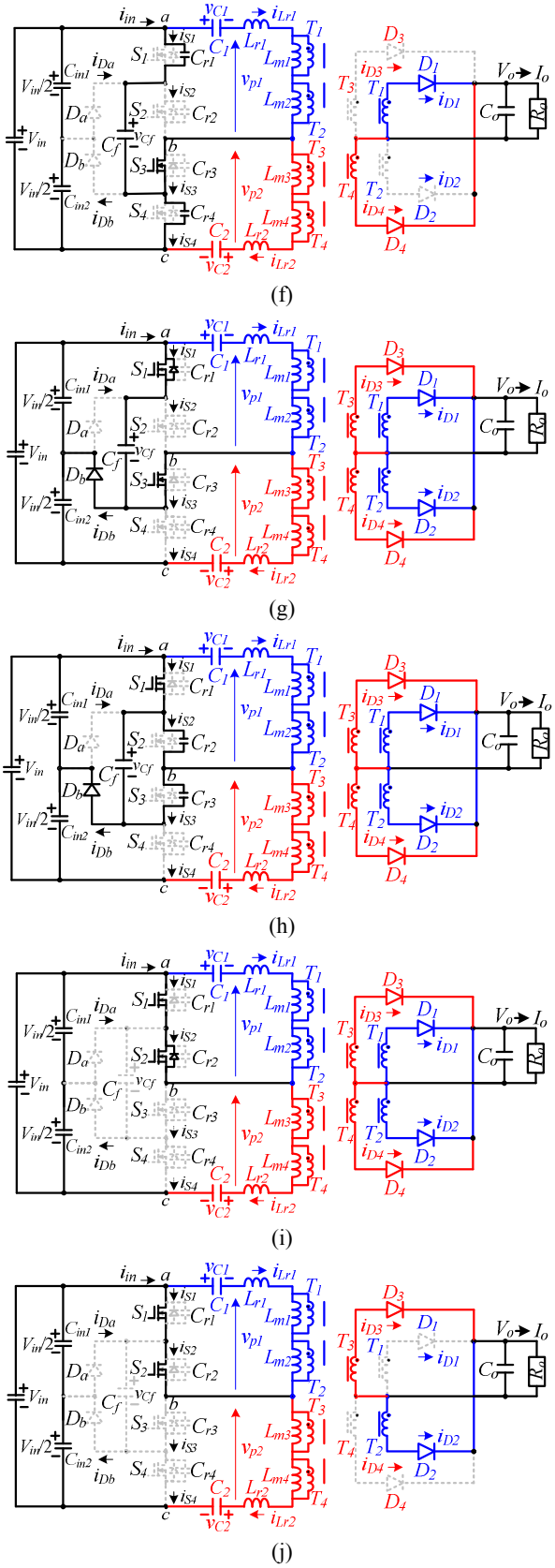


Fig. 3. Operation modes of the proposed converter during one switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8 (i) mode 9 (j) mode 10.

$$\Delta i_{Lr1} \approx \frac{V_{in}-2n(V_o+V_D)}{2L_m}(\delta-\frac{2L_rI_of_s}{nV_{in}})T_s \approx rI_o/(2n) \quad (32)$$

where r is the ripple current ratio of load current. From (31) and (32), the magnetizing inductance L_m of T_1-T_4 is given as:

$$L_m \approx \frac{2n^2(V_o+V_D)(1-\delta+\frac{2L_rI_of_s}{nV_{in}})}{rI_of_s} \quad (33)$$

The maximum diode currents are expressed as:

$$i_{D1,\max}=i_{D2,\max}=i_{D3,\max}=i_{D4,\max} \approx \frac{I_o}{2}+\frac{n^2(V_o+V_D)}{2L_mf_s}(1-\delta+\frac{2L_rI_of_s}{nV_{in}}) \quad (34)$$

Since the average currents on capacitances C_1 and C_2 are zero, the average magnetizing currents I_{Lm1}-I_{Lm4} equal zero. In modes 5 and 10, we can obtain the voltage stresses of D_1-D_4.

$$v_{D1,\text{stress}}=v_{D2,\text{stress}}=v_{D3,\text{stress}}=v_{D4,\text{stress}} \approx V_{in}/(2n) \quad (35)$$

The peak currents of switches S_1-S_4 are given as:

$$i_{S2,\max}=i_{S3,\max}=i_{S4,\max}=i_{S1,\max} \approx \frac{I_o}{n}+\frac{n(V_o+V_D)}{L_mf_s}(1-\delta+\frac{2L_rI_of_s}{nV_{in}}) \quad (36)$$

In Fig. 3, power is delivered from input source voltage to output load in modes 5 and 10. Thus, the root-mean-square (*rms*) currents of S_1-S_4 can be expressed as:

$$i_{S1,rms}=i_{S2,rms}=i_{S3,rms}=i_{S4,rms} \approx \frac{I_o}{n\sqrt{2}} \quad (37)$$

The voltage stresses of S_1-S_4 are expressed as:

$$V_{S1,stress}=V_{S2,stress}=V_{S3,stress}=V_{S4,stress}=V_{in}/2 \quad (38)$$

In mode 10, the inductor currents $i_{Lr1}(t_0)$ (or $i_{Lr1}(T_s+t_0)$) and $i_{Lr2}(t_0)$ (or $i_{Lr2}(T_s+t_0)$) are expressed as:

$$i_{Lr1}(t_0) \approx -\frac{I_o}{2n}-\frac{n(V_o+V_D)}{2L_mf_s}(1-\delta+\frac{2L_rI_of_s}{nV_{in}}) \quad (39)$$

$$i_{Lr2}(t_0) \approx \frac{I_o}{2n}+\frac{n(V_o+V_D)}{2L_mf_s}(1-\delta+\frac{2L_rI_of_s}{nV_{in}}) \quad (40)$$

In mode 2, the inductor currents $i_{Lr1}(t_2)$ and $i_{Lr2}(t_2)$ are given as:

$$i_{Lr1}(t_2) \approx i_{Lr1}(t_0)+\frac{(V_{S2,drop}+V_{Da,drop})}{L_rf_s}(0.5-\delta)=-\frac{I_o}{2n} -\frac{n(V_o+V_D)}{2L_mf_s}(1-\delta+\frac{2L_rI_of_s}{nV_{in}})+\frac{(V_{S2,drop}+V_{Da,drop})}{L_rf_s}(0.5-\delta) \quad (41)$$

$$i_{Lr2}(t_2) \approx i_{Lr2}(t_0)-\frac{(V_{S2,drop}+V_{Da,drop})}{L_rf_s}(0.5-\delta)=\frac{I_o}{2n} +\frac{n(V_o+V_D)}{2L_mf_s}(1-\delta+\frac{2L_rI_of_s}{nV_{in}})-\frac{(V_{S2,drop}+V_{Da,drop})}{L_rf_s}(0.5-\delta) \quad (42)$$

From (1) and (16), the necessary resonant inductance L_r for ZVS turn-on of S_1 and S_4 is given as:

$$L_r \geq \frac{C_rV_{in}^2}{2[i_{Lr1}^2(t_0)+i_{Lr2}^2(t_0)]}-L_m \quad (43)$$

From (7) and (22), the necessary inductance L_r to achieve ZVS turn-on of S_2 and S_3 is given as:

$$L_r \geq \frac{C_rV_{in}^2}{2[i_{Lr1}^2(t_2)+i_{Lr2}^2(t_2)]} \quad (44)$$

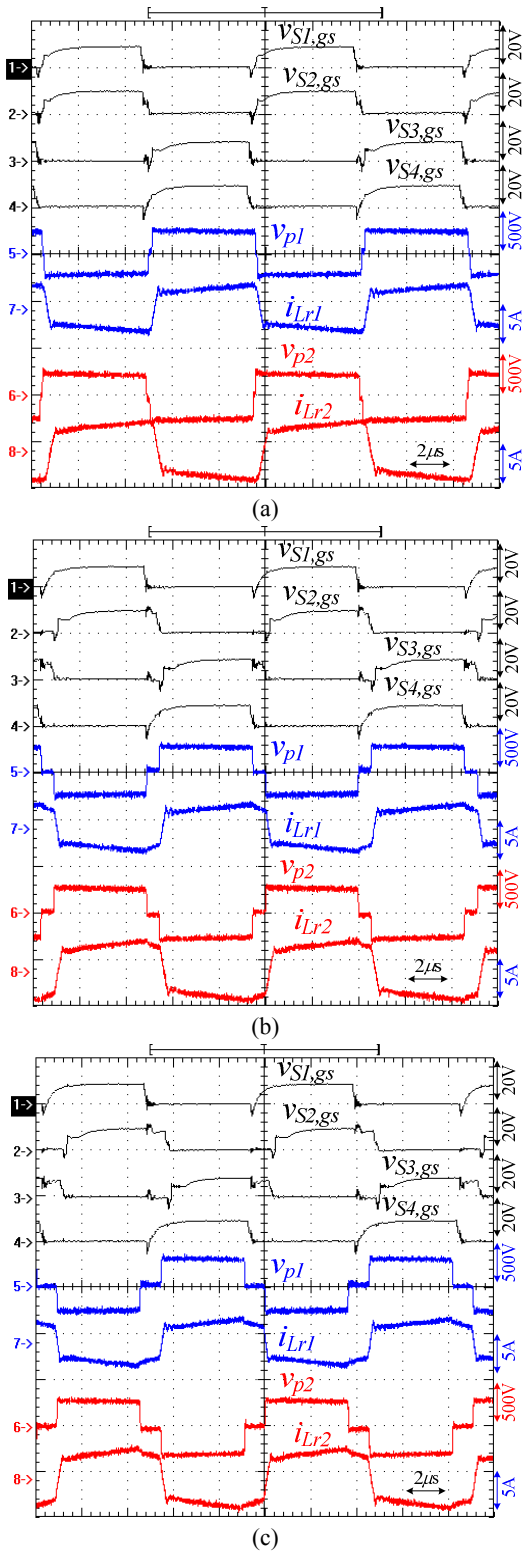


Fig. 4. Measured results of the gate voltages of S_1-S_4, the primary side voltages and currents at full load and (a) V_{in}=480V (b) V_{in}=530V (c) V_{in}=580V.

V. EXPERIMENTAL RESULTS

Experiments with a laboratory prototype are provided to verify the theoretical analysis and demonstrate the

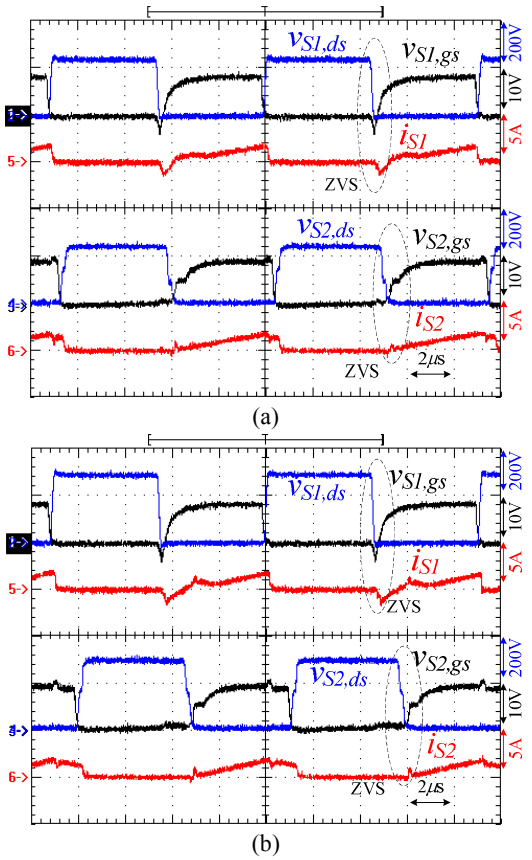


Fig. 5. Measured waveforms of the gate voltage, drain voltage and switch current of switches S_1 and S_2 at 20% load and (a) V_{in}=480V (b) V_{in}=580V.

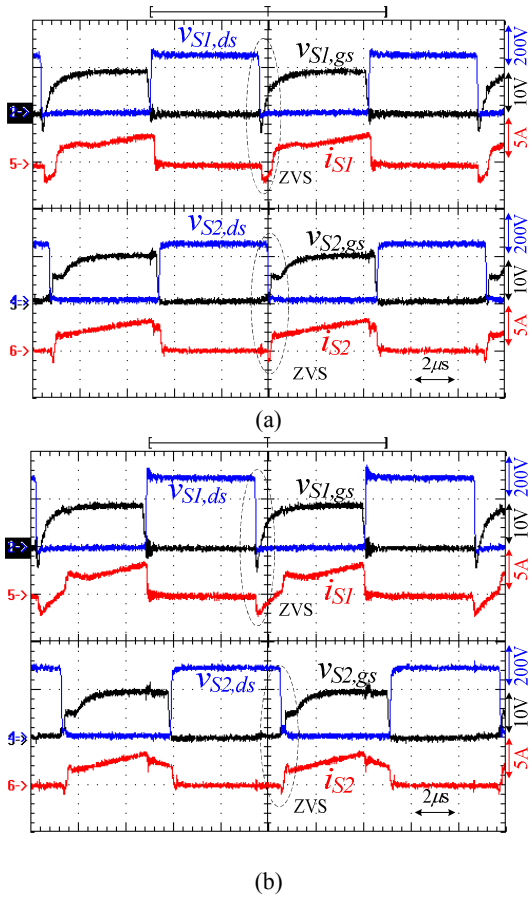


Fig. 6. Measured results of gate voltage, drain voltage and switch current of S_1 and S_2 at 50% load and (a) V_{in}=480V (b) V_{in}=580V.

effectiveness of the proposed converter. The specifications and circuit parameters of the proposed converter are: V_{in}=480-580V, V_o=24V, P_o=1kW, f_s=100kHz, C_o=6600μF, C_1=C_2=C_f=0.47μF, C_{in1}=C_{in2}=0.68μF, T_1-T_4:n_p/n_s=36T/8T, L_{m1}-L_{m4}:620μH, L_{r1}=L_{r2}=20μH, D_1-D_4:FST3160, S_1-S_4:IRFP460 and D_a-D_b:30ETH06. The lagging switches S_2 and S_3 are designed to have ZVS turn-on at least from 20% to 100% load. Fig. 4 gives the measured waveforms of the gate voltages of S_1-S_4, the primary side voltages v_{p1} and v_{p2} and the primary side currents at full load and the different input voltages. Three voltage levels are generated on v_{p1} and v_{p2}. The primary side voltages v_{p1} and v_{p2} are phase-shifted by one-half of switching cycle (complementary each other). If S_1 and S_2 are both in the on-state, the primary side current i_{Lr1} decreases and i_{Lr2} increases. On the other hand, i_{Lr1} increases and i_{Lr2} decreases if S_1 and S_2 are both in the off-state. It is also clear that the phase shift between S_1 and S_2 at V_{in}=580V is greater than the phase shift at V_{in}=480V. Therefore, the primary side voltages v_{p1} and v_{p2} at V_{in}=580V have less duty cycle to transfer power form input voltage to output load. Fig. 5 gives the measured results of the gate voltage, drain voltage and switch current of the leading switch S_1 and the lagging switch S_2 at 20% load for low and high input voltages. It is clear in Fig. 5 that the leading and lagging switches S_1 and S_2 achieve ZVS turn-on at 20% for low and high input voltages. Similarly, Figs. 6 and 7 give the measured results of the gate voltage, drain voltage and switch current of S_1 and S_2 at 50% and 100% load, respectively, for both low and high input voltages. The leading and lagging switches are also turned on at ZVS at 50% and 100% loads shown in Figs. 6 and 7. The voltage stress of both switches S_1 and S_2 is equal to V_{in}/2. Since the operation behaviors of S_3 and S_4 are identical with respective to S_2 and S_1, it is clear that S_3 and S_4 realize ZVS turn-on from 20% load to 100% load. Fig. 8 gives the experimental waveforms of the DC blocking voltages v_{C1} and v_{C2} and the flying capacitor voltage v_{Cf} at full load for both low and high input voltages. The average voltages of C_1, C_2 and C_f are equal to V_{in}/2. Fig. 9 shows the experimental waveforms of the gate voltage $v_{S1,gs}$ and the secondary side diode currents at full load for both low and high input voltages. If switches S_1 and S_2 are in the on-state (or off-state), D_2 and D_3 (or D_1 and D_4) are conducting. The output currents i_{D1}+i_{D2} and i_{D3}+i_{D4} of two three-level PWM circuits are balanced to supply one-half of load current. Fig. 10 shows the measured efficiencies of the proposed converter from 10% load to full load at different input voltages.

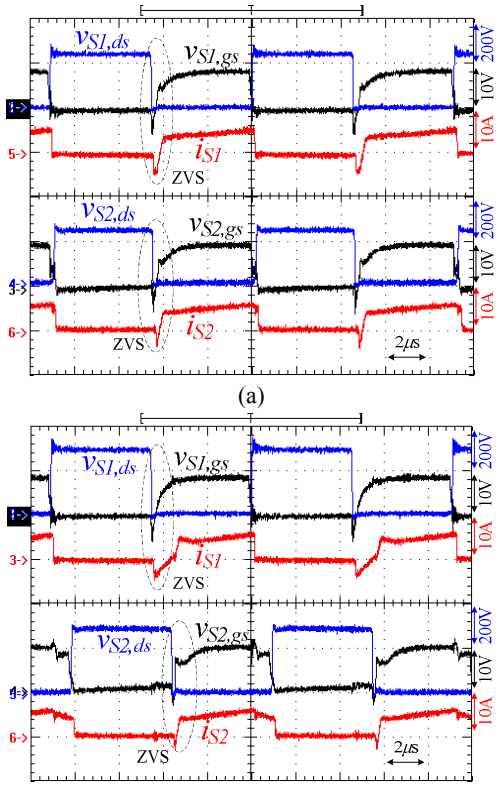


Fig. 7. Measured waveforms of the gate voltage, drain voltage and switch current of switches S_1 and S_2 at 100% load and (a) V_{in}=480V (b) V_{in}=580V.

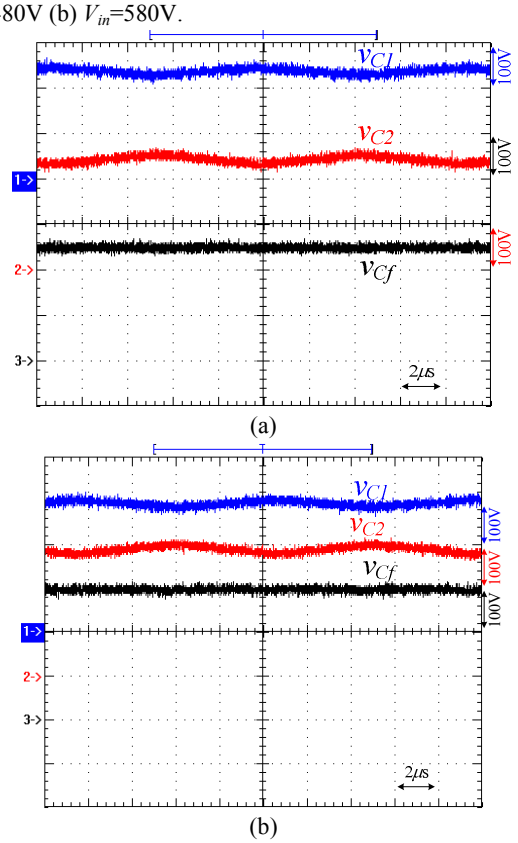


Fig. 8. Measured waveforms of the DC blocking voltages v_{C1} and v_{C2} and the flying capacitor voltage v_{Cf} at full load and (a) V_{in}=480V (b) V_{in}=580V.

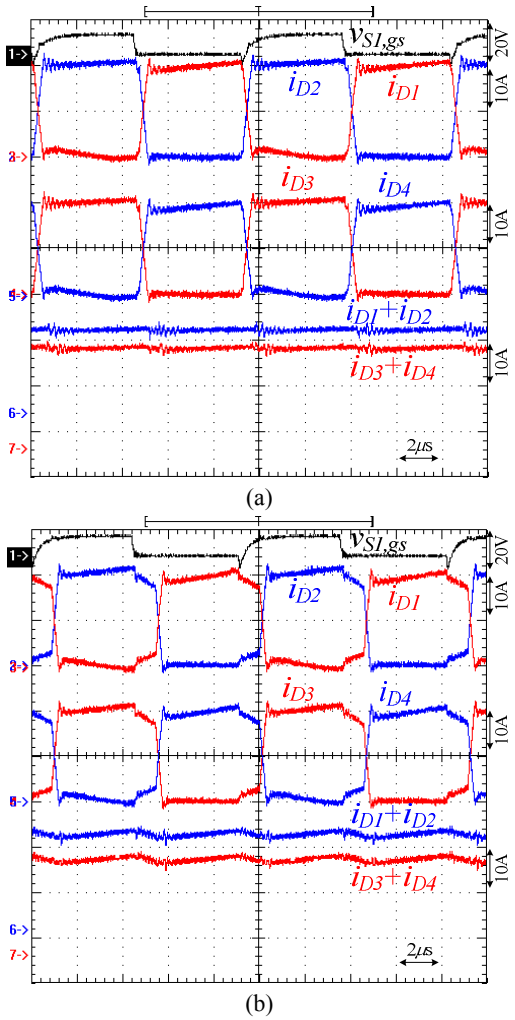


Fig. 9. Measured waveforms of the rectifier diode currents at full load and (a) V_{in}=480V (b) V_{in}=580V.

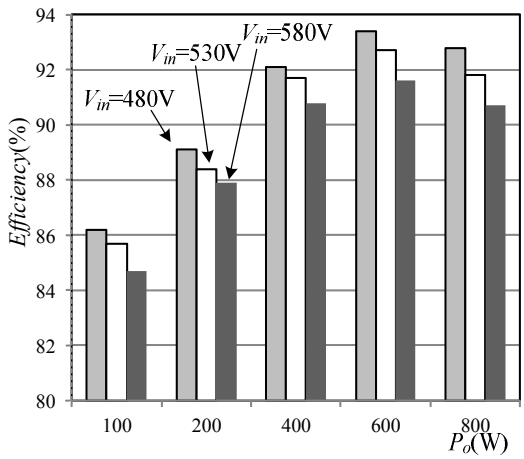


Fig. 10. Measured circuit efficiencies of the proposed converter from 10% load to 100% load at different input voltages.

VI. CONCLUSION

A soft switching DC/DC converter with two three-level PWM circuits with the sane power switches and two series-connected transformers is presented to achieve the

functions of 1) ZVS turn-on for both the leading and lagging switches from 25% to 100% load, 2) low voltage stress of MOSFETs with $v_{stress}=V_{in}/2$ using three-level PWM scheme, 3) no output filter inductors using two series-connected transformers, and 4) low current stress of transformer windings, output inductors and rectifier diodes using two center-tapped circuit topologies. Phase-shift PWM is adopted to generate four PWM signals and to regulate the output voltage. The energy stored in the resonant inductance and magnetizing inductance is used to achieve ZVS turn-on of the leading switches. However, only the energy stored in the resonant inductance is used to achieve ZVS turn-on of the lagging switches. The system analysis, operation mode and design considerations of the proposed converter are discussed in detail. Finally, experiments with 1*k*W prototype are provided to verify the theoretical analysis and demonstrate the effectiveness of the proposed converter.

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