New GGNMOS I/O Cell Array for Improved Electrical Overstress Robustness

Yon-Sup Pang and Youngju Kim

***Abstract*—A 0.18-μm 3.3 V grounded-gate NMOS (GGNMOS) I/O cell array for timing controller (TCON) application is proposed for improving electrical overstress (EOS) robustness. The improved cell array consists of 20 GGNMOS, 4 inserted well taps, 2 end-well taps and shallow trench isolation (STI). Technology computer-aided design (TCAD) simulation results show that the inserted well taps and extended drain contact gate spacing (DCGS) is effective in preventing EOS failure, e.g. local burnout. Thermodynamic models for device simulation enable us to obtain lattice temperature distributions inside the cells. The peak value of the maximum lattice temperature in the improved GGNMOS cell array is lower than that in a conventional GGNMOS cell array. The inserted well taps also improve the uniformity of turn-on of GGNMOS cells. EOS test results show the validity of the simulation results on improvement of EOS robustness of the new GGNMOS I/O cell array.**

***Index Terms*—EOS, GGNMOS, TCAD, simulation, ESD, timing controller**

I. INTRODUCTION

Modern integrated circuits should be designed to be robust to EOS/ electrostatic discharge (ESD) [1-5] for preventing circuit/device failure due to burnout. It has been reported that major failure mechanisms due to EOS/ESD are thermal overload caused by dissipated energy or dielectric breakdown resulting from strong electric field or high voltage stress imposed for a certain amount of time [1]. Fig. 1 shows an SEM picture after EOS test of our conventional 0.18-μm 3.3V GGNMOS cell array fabricated in our company, The GGNMOS cell array is for TCON applications [2]. The burnout area is due to excessive heat generated at the center of the GGNMOS cell array.

TCAD simulation was essentially used for proposing an improved GGNMOS cell array with inserted well taps and extended DCGS, which is robust to the EOS failure. The extended DCGS as well as the inserted well taps are effective in lowering the maximum lattice temperature. The conventional GGNMOS cell array has multiple fingers for reducing the total silicon area, but the GGNMOS cells do not turn on uniformly [3]. TCAD simulation results show that the inserted well tap can improve the uniformity of turn-on of the GGNMOS cells.

Transmission line pulsing (TLP) measurement is used for observing electrical characteristics of semiconductor devices under ESD stress, but long pulse-transmission line pulsing (LP-TLP) measurement needs to be used for

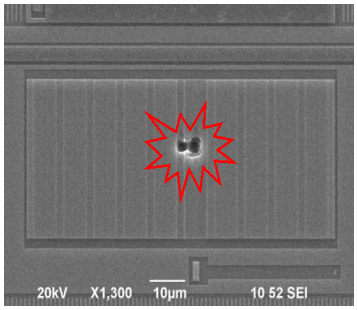

Fig. 1. SEM picture of conventional GGNMOS cells after EOS test.

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MagnaChip Semiconductor, 1 Hyangjeong-dong, Hungduk-gu, Cheongju-si, 361-725, Korea
E-mail : ysbahng@naver.com

characterizing integrated circuits to remove ambiguous I-V characteristics of TLP [1, 4]. LP-TLP was used for obtaining experimental EOS failure test and TCAD simulation results in this paper.

Section II describes cross-sectional view of conventional GGNMOS I/O cell array, and models for process and device simulations. An improved GGNMOS I/O cell array robust to EOS stress is proposed and compared with the conventional one in Section III. Experimental results on the improved GGNMOS cell array are also presented in Section III. Conclusions are drawn in Section IV.

II. Device Structure and TCAD Simulation

1. Cross-sectional View of GGNMOS Cell Array

The cross-sectional view of two adjacent 0.18-μm 3.3-V GGNMOS I/O cells of TCON is shown in Fig. 2.

The space between the drain contact and the gate poly edge is wider than that on the source side. The GGNMOS cell array has finger-type gates to reduce the chip size.

2. TCAD Simulation

Layout-based partition of the 100-μm long 20-GGNMOS cell array, the reflection of single GGNMOS cell and the most accurate process models on point defects, dopant activation and diffusion available for process simulation [6, 7] were used for obtaining doping profiles and device structures as shown in Fig. 3 in a reasonable simulation time. To save process simulation time, the entire layout of the GGNMOS cell array is

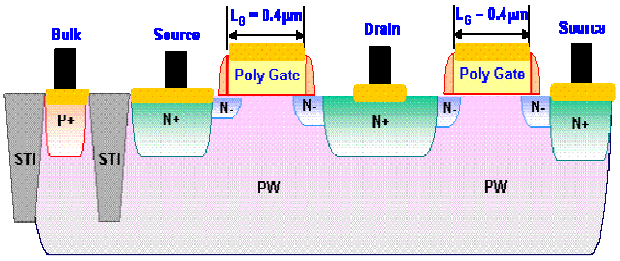


Fig. 2. Cross-sectional view of two adjacent 0.18-μm 3.3 V conventional GGNMOS I/O cells.

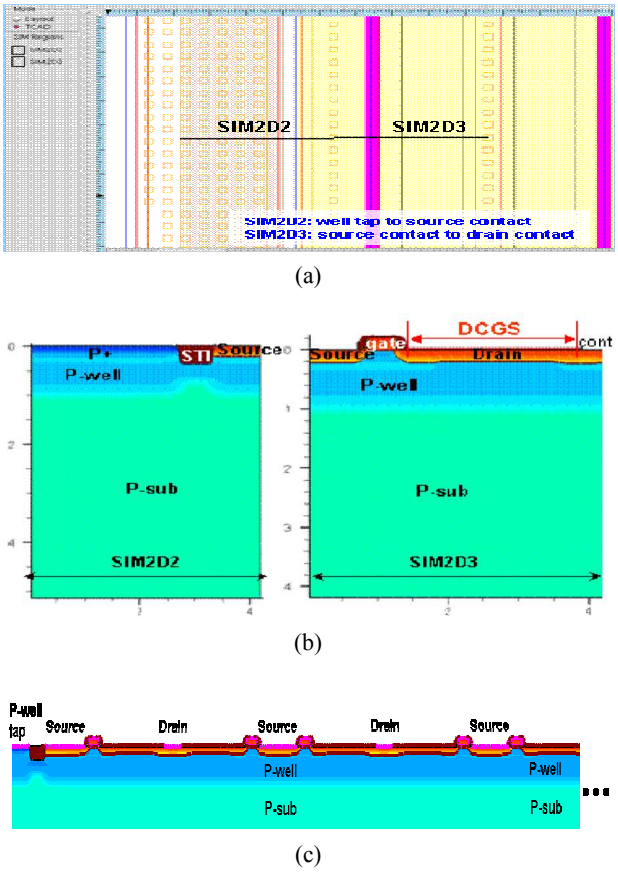


Fig. 3. (a) Layout view of 0.18-μm 3.3 V conventional GGNMOS I/O cells for TCAD simulation, (b) simulated 2D doping profiles of p-well tap region (SIM2D2) and GGNMOS (SIM2D3), (c) simulated conventional GGNMOS cell array with 20 GGNMOS, 2 end-well taps and STI.

partitioned into 2 p-well tap regions and 20 GGNMOS cells. Fig. 3(a) shows a part of the entire layout, which consists of the left-side p-well tap region (SIM2D2), the first GGNMOS cell (SIM2D3) and its adjacent GGNMOS cell. The left side p-well tap region and the first GGNMOS are simulated separately as shown in Fig. 3(b). They along with their identical and reflected ones are put together to form the whole cell array as shown in Fig. 3(c). This partition and unification technique saves process simulation time of the 100-μm or longer cell array. Models on the thermodynamics, the doping-, field- and temperature-dependent mobility, the band gap narrowing, the generation-recombination and the avalanche generation were used for device simulation [8]. The lattice temperature inside the cells can be computed non-uniformly, using the thermodynamic models. The maximum lattice temperature is a parameter used for evaluating EOS robustness of simulated cell arrays.

III. IMPROVED EOS ROBUSTNESS

The long-pulse EOS stress waveform with 50 μsec duration is compared with the short-pulse ESD one with 100 nsec duration in Fig. 4. Traditional TLP using the short-pulse ESD stress waveform is to characterize single devices [1], but LP-TLP using the long-pulse EOS stress waveform is to characterize complex integrated circuits [1, 2, 4]. LP-TLP should be used for removing ambiguous I-V characteristics of integrated circuits in TLP measurement. The EOS input voltage pulse has the maximum voltage, V_{max}, as a parameter and 50 μsec duration at $V_{max}/2$. The single 3.3V GGNMOS of the cell array has been used for ESD protection, and has the DC and TLP I-V characteristics as shown in Figs. 5(a) and (b). The TLP I-V characteristic was obtained after the ESD stress waveform in Fig. 4(b) was applied to the 3.3 V GGNMOS. The peak values of the maximum lattice temperature and the total drain current of the conventional 20 GGNMOS cell array during the EOS stress time are observed at the maximum EOS stress voltage, V_{max}, in the EOS simulation results of Figs. 5(c) and (d). To evaluate the uniformity of turn-on of the

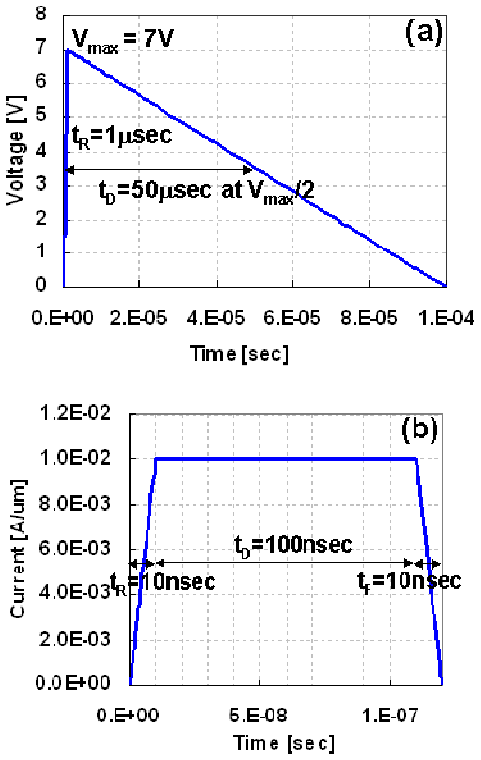


Fig. 4. (a) EOS, (b) ESD stress waveforms where t_R, t_D and t_F are the rise time, duration and fall time, respectively.

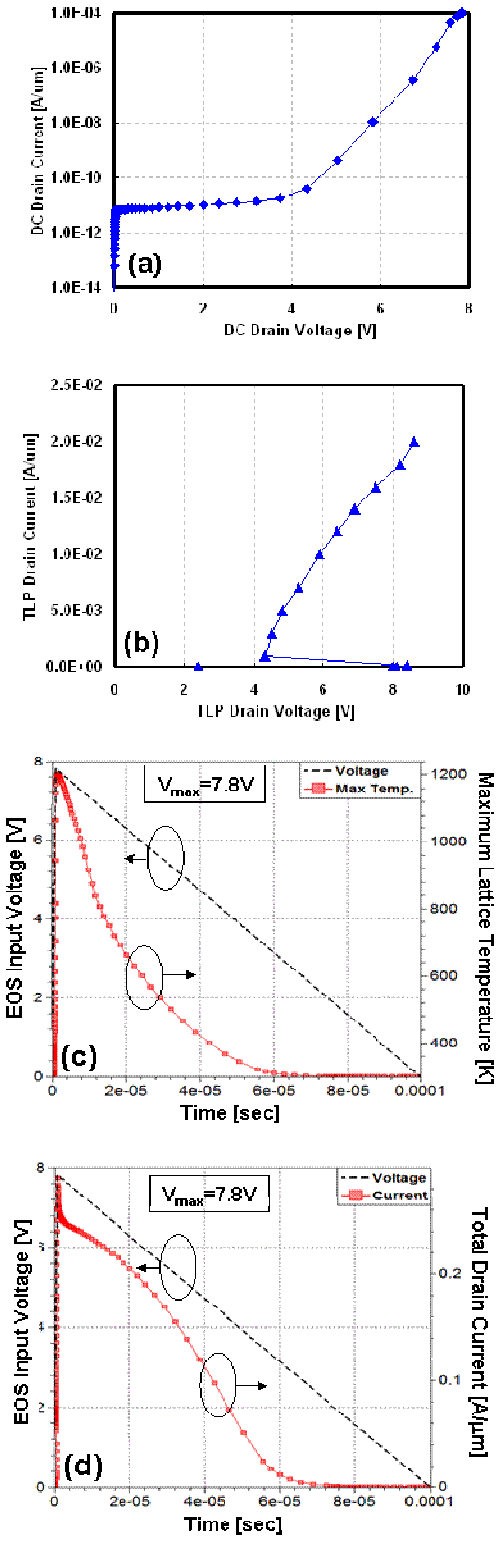
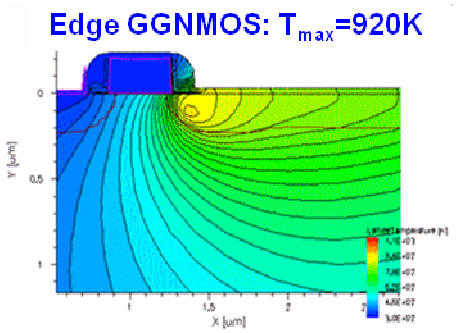


Fig. 5. (a) DC I_D-V_{DS} characteristic at V_{GS}=0 V of the single GGNMOS, (b) TLP I_D-V_{DS} characteristic of the single GGNMOS responding to the ESD input current pulse in Fig. 4 (b), and the variations of (c) the maximum lattice temperature, (d) the total drain current with time of the conventional GGNMOS cell array responding to the EOS input voltage pulse in Fig. 4 (a). V_G=V_S=0 V.

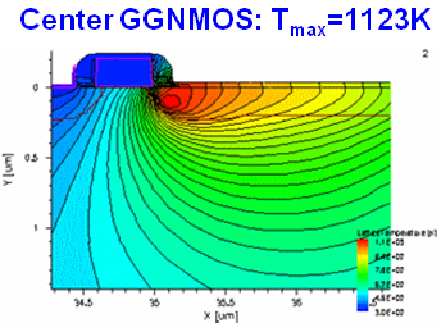
GGNMOS cells, the local maximum lattice temperatures, T_{max}, of the center and the edge GGNMOS were checked. The maximum lattice temperature of the center GGNMOS is 22% higher than that of the edge GGNMOS of the conventional cell array in Fig. 6.

The extended drain contact gate spacing (DCGS) is effective in reducing the maximum lattice temperature of the cell array and the difference between the local maximum lattice temperatures of the GGNMOS cells as shown in Figs. 7 and 8.

As DCGS is increased, the drain resistance increases and in consequence, the drain junction field intensity of the each GGNMOS decreases. Fig. 9(a) shows a simulated structure of the improved new 0.18-μm 3.3V GGNMOS cell array with 20 GGNMOS, 4 inserted well taps, 2 end-well taps and STI. The inserted well taps are also effective in reducing the peak value of the maximum lattice temperature of the cell array as well as the difference between the local maximum lattice temperatures of GGNMOS cells as shown in Fig. 9(b) and (c).

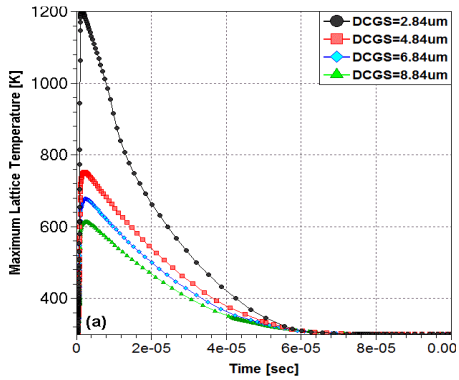


(a)

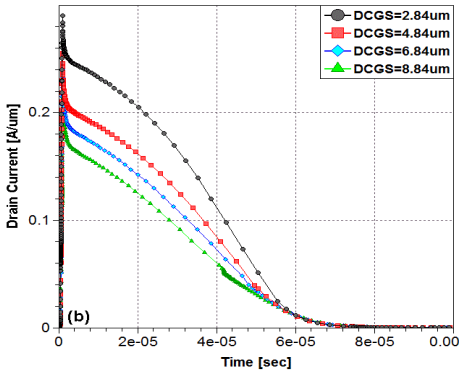


(b)

Fig. 6. Lattice temperature contours in (a) the edge, (b) the center GGNMOS with DCGS=2.84 μm of the conventional cell array at t=1 μsec after the EOS input voltage pulse was applied. T_{max} (Center GGNMOS) > T_{max} (Edge GGNMOS) by 22%.



(a)



(b)

Fig. 7. Simulated dependence of (a) maximum lattice temperature, (b) drain current on DCGS of the GGNMOS cell array responding to the EOS input pulse. V_{max}=7.8 V.

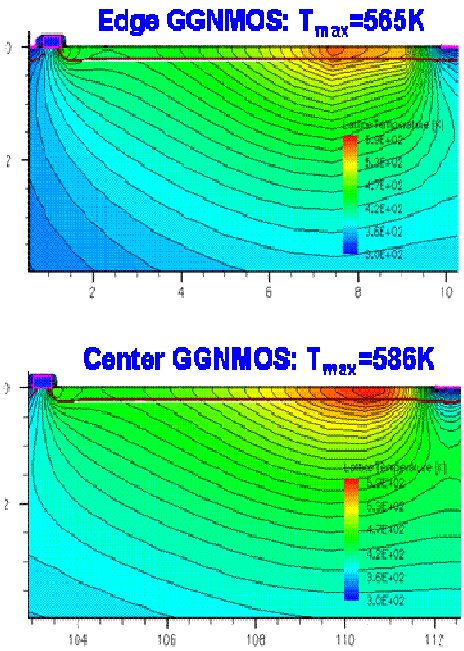


Fig. 8. Lattice temperature contours in (a) the edge, (b) the center GGNMOS with DCGS=8.84 μm at t=1 μsec after the EOS input voltage pulse was applied. T_{max} (Center GGNMOS) > T_{max} (Edge GGNMOS) by 3.72%.

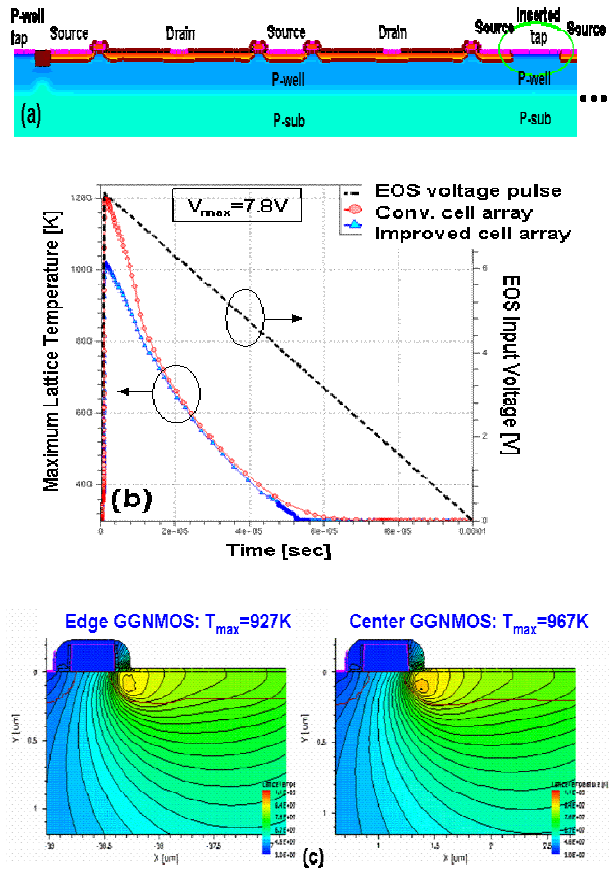


Fig. 9. (a) Improved GGNMOS cell array with inserted taps, (b) the variations of the maximum lattice temperature with time of the conventional and the improved GGNMOS cell arrays with DCGS=2.84 μm responding to the EOS input voltage pulse, (c) lattice temperature contours in the edge and the center GGNMOS at t=1 μsec after the EOS input voltage pulse was applied. T_{max} (Center GGNMOS) > T_{max} (Edge GGNMOS) by 4.31%.

Excessive holes generated by the impact ionization or tunneling can be taken out of the GGNMOS cells efficiently through the inserted taps. Fig. 10 shows that the peak value of the maximum lattice temperature of the improved GGNMOS cell array is lower than that of

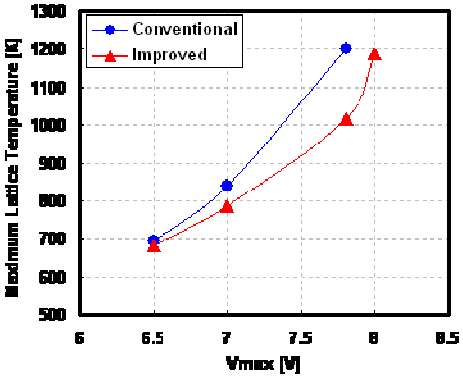


Fig. 10. Dependence of the peak maximum lattice temperature of the conventional and the improved GGNMOS cell arrays on the maximum voltage of the EOS voltage pulse.

conventional GGNMOS cell array for each V_{max} value. The EOS test results on the output voltage to failure in Table 1 show that the improved GGNMOS cell array with the extended DCGS and the inserted well taps is robust to the EOS failure.

IV. CONCLUSIONS

A 0.18-μm 3.3V GGNMOS I/O cell array with the extended DCGS and the inserted well taps for TCON application has been proposed for improving EOS robustness, using TCAD simulation. Thermodynamic models for TCAD simulation were essentially used to compute the lattice temperature non-uniformly inside the GGNMOS cells. The improved GGNMOS cell array has a lower peak value of the maximum lattice temperature and smaller difference between the local maximum lattice temperatures in the GGNMOS cells than those of the conventional GGNMOS cell array. The validity of the simulation results on improvement of EOS robustness of the new GGNMOS cell array was verified with EOS failure test results.

Table 1. Experimental results on the output voltage to failure for four different test modes

Mode	Stress polarity	$V_{OUT(Failure)}$ target	Failure test results ($V_{OUT(Failure)}$)		
			Conventional	Conventional (Increased gate width)	Improved (Added inserted taps, increased DCGS and gate width)
VDD grounded	Positive	≥17 V	13 V	16 V (23%)	26 V (100%)
	Negative	≥17 V	14 V	16 V (14%)	31 V (121%)
VSS grounded	Positive	≥17 V	10 V	10 V (0%)	17 V (70%)
	Negative	≥17 V	11 V	13 V (18%)	32 V (191%)

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Yon-Sup Pang (Bahng) received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, in 1984 and 1986, respectively, the graduate engineer degree in computer engineering from Syracuse University, Syracuse, NY, USA in 1992, and the Ph.D. degree in electrical and computer engineering from the University of Arizona, Tucson, AZ, USA in 2000. From 1994 to 2002, he as a researcher/research associate/research assistant worked on design and modeling of deep-submicrometer and sub-100-nm MOSFETs for low-power and high-performance applications, semiconductor device models for circuit simulation, electronic packaging and computer simulation techniques at the University of Arizona. His research for the graduate computer engineer degree at Syracuse University was about computer-aided logic/physical design and computer hardware. He joined Hynix and MagnaChip Semiconductor in Korea in 2003 and 2004, respectively, where he has been working on various aspects of mixed-signal, nonvolatile memory, high-voltage and power semiconductor devices. He is currently a senior member of technical staff and a leader of the technology computer-aided design group at MagnaChip Semiconductor. From March 2009 to February 2010, he as an adjunct professor/lecturer was with the department of electronic engineering of Pai Chai University in Daejeon, Korea. His current research and development interests include design of mixed-signal, nonvolatile memory, high-voltage and power semiconductor devices, and device, process and reliability simulation techniques and models. Dr. Pang is a member of the IEEE Electron Devices Society and an editing member of Modeling and Simulation Chapter of International Technology Roadmap for Semiconductors, and served as a reviewer of IEEE Transactions on Electron Devices.