PCRAM Flip-Flop Circuits with Sequential Sleep-in Control Scheme and Selective Write Latch

Jun-Myung Choi, Chul-Moon Jung, and Kyeong-Sik Min

Abstract—**In this paper, two new flip-flop circuits with PCRAM latches that are FF-1 and FF-2, respectively, are proposed not to waste leakage during sleep time. Unlike the FF-1 circuit that has a normal PCRAM latch, the FF-2 circuit has a selective write latch that can reduce the switching activity in writing operation to save switching power at sleep-in moment. Moreover, a sequential sleep-in control is proposed to reduce the rush current peak that is observed at the sleep-in moment. From the simulation of storing '000000' to the PCRAM latch, we could verify that the proposed FF-1 and FF-2 consume smaller power than the conventional 45-nm FF if the sleep time is longer than 465 μs and 95 μs, respectively, at 125°C. For the rush current peak, the sequential sleep-in control could reduce the current peak as much as 77%.**

Index Terms—**Phase-change RAMs, flip-flop circuit, nonvolatile retention latch, sequential sleep-in control, selective write latch**

I. INTRODUCTION

Phase-Change RAMs (PCRAM) have been studied for many years due to better scalability than DRAMs and FLASH memories thus they are considered now as strong candidates for future memories [1, 2]. In addition to the traditional applications, PCRAM can be merged with CMOS digital circuits thus it can extend the usefulness beyond the traditional memory applications. For example, the nonvolatile nature of PCRAMs can be exploited by retention latches [3]. Using PCRAM latches, flip-flop's (FFs) data can be stored at the latches during the sleep time. Using the retention latches, the FF can be cut off from power lines during the sleep time thereby they do not waste any leakage power when they are sleep [4].

The memristor retention latch was proposed in [4], but, in this paper, a newly proposed PCRAM flip-flop is different from the memristor FF in two aspects [5]. First, memristor latch is programmed by bipolar voltage pulses. For PCRAM latch, the programming is done by unipolar current pulses for 'SET' and 'RESET' writing. The new FF circuit in this paper is designed and tested to provide the current pulses for PCRAM latch not voltage pulses [5]. Second, a new sequential control for moving the FF's data to PCRAM latches is proposed here [5]. This is very essential to mitigate large rush current that is caused by the PCRAM writing at the sleep-in moment. Because the slow sleep-in does not degrade system performance, we can reduce the rush current peak by increasing the sleep-in time.

II. TWO PCRAM FLIP-FLOP CIRCUITS AND SEQUENTIAL SLEEP-IN CONTROL

In this paper, we propose two PCRAM FF circuits that are FF-1 and FF-2, respectively. The FF-1 is shown in Fig. 1(a). Here the FF-1 circuit is composed of master-slave FF and PCRAM latch that is used to store FF's data during the sleep time. In Fig. 1(a), D_{IN} is input data and CK and CKB are clock signal and its inverted version, respectively. Q and QB are output signal and its

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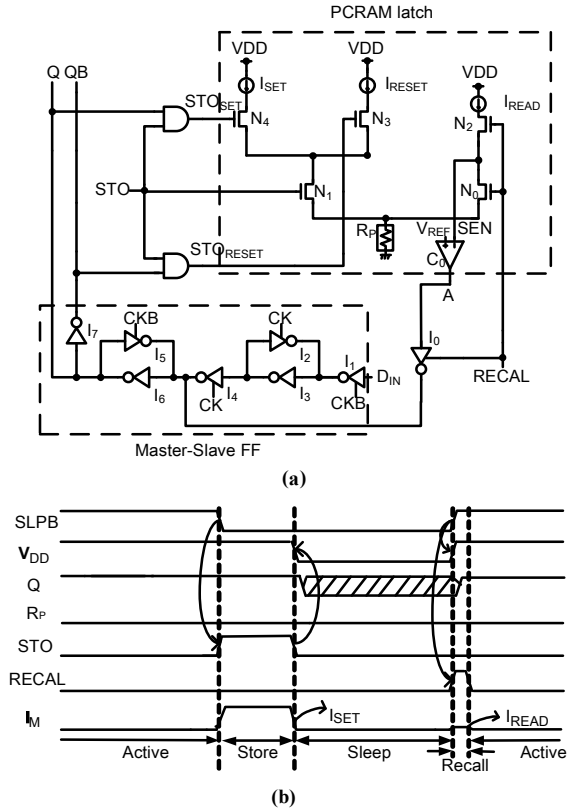

Fig. 1. (a) FF-1 circuit with PCRAM latch, (b) its timing diagram.

complement, respectively. STO becomes high when the FF-1's data is stored at the PCRAM latch in Fig. 1(a). RECAL is enabled to transfer the data from the PCRAM latch to the FF when the active mode begins. I_1, I_2, and I_3 constitute the master latch. Similarly the slave latch is composed of I_4, I_5, and I_6. I_7 is an inverter to drive QB. I_0 is a clocked inverter to drive the slave latch for the recalling operation. N_1 and N_4 are turned on when the FF-1's data is '1' and STO becomes high in order to store FF-1's data at the PCRAM latch. At this time, I_{SET} as large as 600 μA is applied to decrease PCRAM resistance to R_{SET} by the current mirror circuit. Table 1 shows the PCRAM states. For '0', the PCRAM state is 'RESET' and R_{RESET} is 200 kΩ. For '1', the PCRAM state is 'SET' and R_{SET} is 7 kΩ. The 'SET' and 'RESET' current are 600 μA and 1250 μA, respectively. N_1 and N_3 are turned on when the FF-1's data is '0' and STO becomes high in order to store FF-1's data at the PCRAM latch. At this time I_{RESET} as large as 1250 μA is applied to increase PCRAM resistance to R_{RESET}. R_P means PCRAM cell. For the FF-1 to recall the latch's

Table 1. The states of PCRAM data

Data	State of PCRAM	Writing Current
0	R_{RESET} = 200 kΩ	1250 μA
1	R_{SET} = 7 kΩ	600 μA

data, N_0 and N_2 are turned on by RECAL signal. I_{READ} as small as 20 μA is applied to PCRAM. When this small I_{READ} is applied, PCRAM resistance does not change because I_{READ} is too small to change the PCRAM resistance. According to PCRAM resistance, a voltage which is associated with the sensing node 'SEN' can be higher or lower than V_{REF}. The voltage of 'A' node is changed according to PCRAM data and I_0 transfers the data from the PCRAM latch to the FF-1's slave latch. The timing diagram of Fig. 1(a) is shown in Fig. 1(b). SLPB signal is low during the sleep time and becomes high when the active mode starts. When SLPB becomes low, STO pulse signal is applied to the PCRAM latch for storing the FF-1's data at the PCRAM latch. When STO is high, PCRAM resistance is changed according to the FF-1's data. After the sleep-in, the FF-1 circuit can be cut off from external power lines such as V_{DD} thus we can eliminate the energy leak in the FF-1 circuit during the sleep time. At the wake-up moment, the supply voltage of the FF-1 is connected to V_{DD} again and then RECAL pulse is issued. If RECAL signal is high, N_0 and N_2 are turned on and the clocked inverter, I_0 is also turned on for restoring operation, in Fig. 1(b).

Fig. 2(a) shows the PCRAM FF-2 circuit, where the selective write circuit is added to avoid unnecessary switching in the storing operation. The selective write circuit is composed of the XOR gate, I_8, the NAND, I_9, and the NOR, I_{10}. The XOR compares 'Q' and 'A' nodes. If they are the same, I_8 gives '0' to disable INT_STO. If 'Q' and 'A' are different, INT_STO becomes high to be enabled. The enabled INT_STO signal goes into I_{11} and I_{12} to write 'SET' or 'RESET' according to the FF-2's data. If INT_STO is disabled, we can know that both I_{11} and I_{12} are turned off to stop the write operation thereby the unnecessary switching can be avoided. Before applying STO signal to FF-2 circuit, READ signal should be issued first to read the PCRAM latch's data before the write operation. Fig. 2(b) shows the timing diagram of FF-2 circuit when the FF-2's data is the same with the previously stored data at the PCRAM latch. Fig. 2(c) shows the timing diagram of FF-2 circuit when the FF-

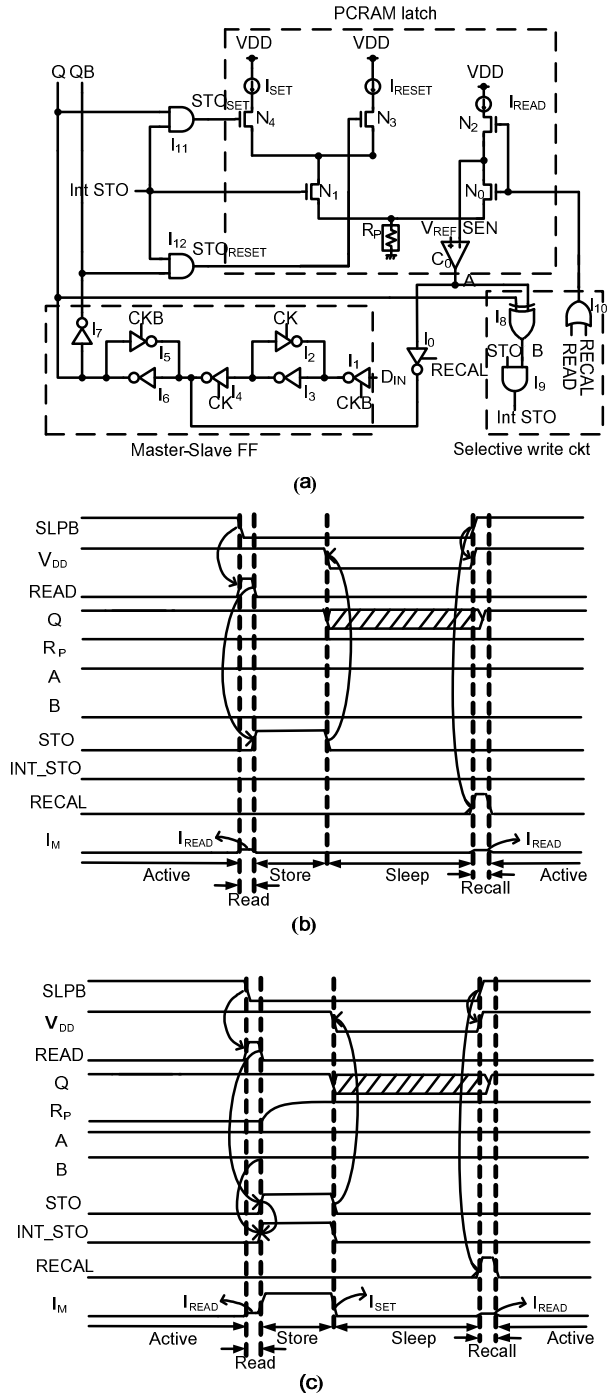

Fig. 2. (a) FF-2 circuit with selective write latch, (b) the timing diagram of FF-2 when the FF-2's data is the same with the stored data at PCRAM latch, (c) the timing diagram of FF-2 when the FF-2's data is different from the stored data at the PCRAM latch.

2's data is different from the PCRAM latch's data.

Fig. 3(a) shows the conventional sleep-in control scheme that programs all the FF circuits at one time. This simultaneous writing to PCRAM latches leads to very

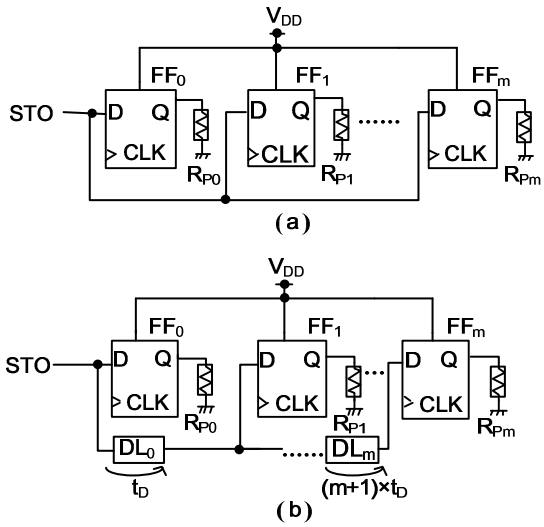

Fig. 3. (a) The conventional sleep-in control scheme, (b) the proposed sequential sleep-in control scheme. DL means the delay line.

large rush current that can destroy the stored data and degrade the reliability such as electromigration. Moreover, power supply noise like IR drop and di/dt noise become more severe by this high rush current peak. Fig. 3(b) shows the proposed sequential sleep-in control, where the PCRAM latches are written one by one not simultaneously to distribute the rush current peak over a certain period of time. The certain time period can be controlled by the delay line, DL in Fig. 3(b). One more thing to note is that the sequential sleep-in control does not degrade the system performance. This is because the storing operation can be done at the sleep time thus it can be hidden from the active-mode operation. Unlike the sleep-in, the wake-up in FF circuit should be completed in a very short time. If the wake-up is slow, it means that the active-mode starting is delayed to slow down system performance.

III. PCRAM MODEL AND SIMULATION

To simulate the PCRAM retention latch, we used a PCRAM model developed previously [6].

$$V_P = \frac{L_n(k_1 R_X I_P + 1)}{k_1} \times \left[w L_n \left(R_{ON} I_P + V_H / \frac{L_n(k_1 R_X I_P + 1)}{k_1} \right) \right]$$

$$\text{where } w = 1 \Big/ \sqrt[n]{\left(\frac{I_P - I_{TH}}{I_X - I_{TH}} \right)^n + 1} \quad (0 \le w \le 1) \qquad (1)$$

Eq. (1) combines the SET-RESET regional equation

and the ON regional equation into one unified equation using an exponential and a logarithmic function as indicated in Eq. (1). Here a transition phenomenon between the SET-RESET and ON region is modeled using a weighting variable that controls a relative portion of each region. Here V_P and I_P are PCRAM voltage and current, respectively. R_X, R_{ON}, and V_H are SET-RESET resistance, ON resistance, and holding voltage, respectively. k_1 is a coefficient of the SET-RESET region and w means a weighting variable which is calculated between 0 and 1. The value of n used in this simulation is 9. As n becomes larger, we can have a sharper transition from the Negative Differential Resistance (NDR) region to the ON region. Fig. 4(a) shows comparison between the measured PCRAM data and the unified PCRAM model [6]. Fig. 4(b) shows PCRAM resistance changes from 'RESET' to 'SET' and vice versa according to the crystal fraction ratio.

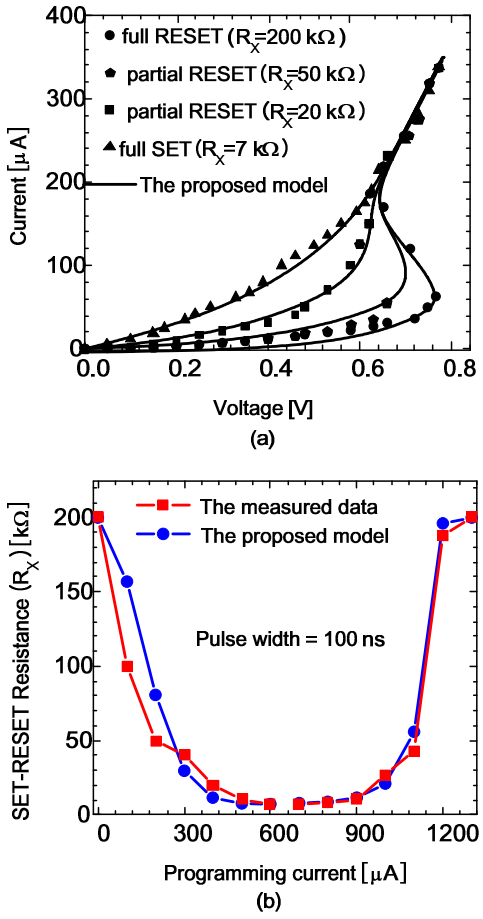

Fig. 4. (a) I-V comparison between the measured data [1] and the proposed unified model [6], (b) Comparison between the measured data [1] and simulated resistance in the full SET, full RESET, partial SET, and partial RESET state [6].

Fig. 5 compares the power consumption between the proposed FF-1 with the normal PCRAM latch and the FF-2 circuit with the selective write latch. As explained in the section II, the FF-2 circuit can save more switching power than FF-1, because the selective write circuit can prevent unnecessary swithcing power from being consumed when the FF's data is the same with the previously stored data at the PCRAM latch. In Fig. 5, we considered various data patterns of '000000', '101010', '111111', and '11001100'. For '101010', the FF's data is always different from the previous latch data. It means that the selective write circuit enables INT_STO always thereby the power saving due to the selective write cannot be expected. For '111111', the FF's data is always the same with the stored data at PCRAM latch. In this case, INT_STO is disabled thereby the uncessary switching can be avoided to save the write switching power. When the data pattern is '000000', the power saving is increased more than '111111'. This is because the RESET current is larger than the SET current. The FF-2 circuit is more power-efficient by 29% than the FF-1 circuit on average.

Fig. 6(a), (b), (c), (d), (e), (f), (g), and (h) compare the current dissipation between the conventional FFs and the proposed FF-1 and FF-2 circuits for T=25 °C and T=125 °C. In Fig. 6, 90-nm FF means the conventional

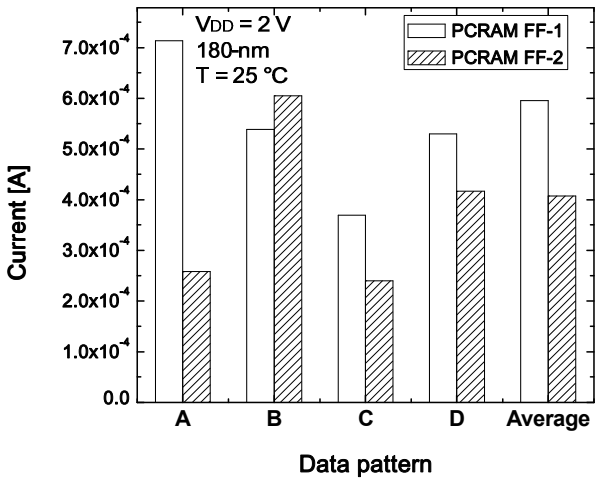

Fig. 5. Current consumption of the FF-1 and FF-2 circuits in the storing operation for various data patterns. The data patterns for A, B, C, and D are '000000', 101010', '111111', and '11001100', respectively. Here I_{SET} and I_{RESET} are 600 μA and 1250 μA, respectively. The cycle time for the STORE and RECALL operation is 370 ns.

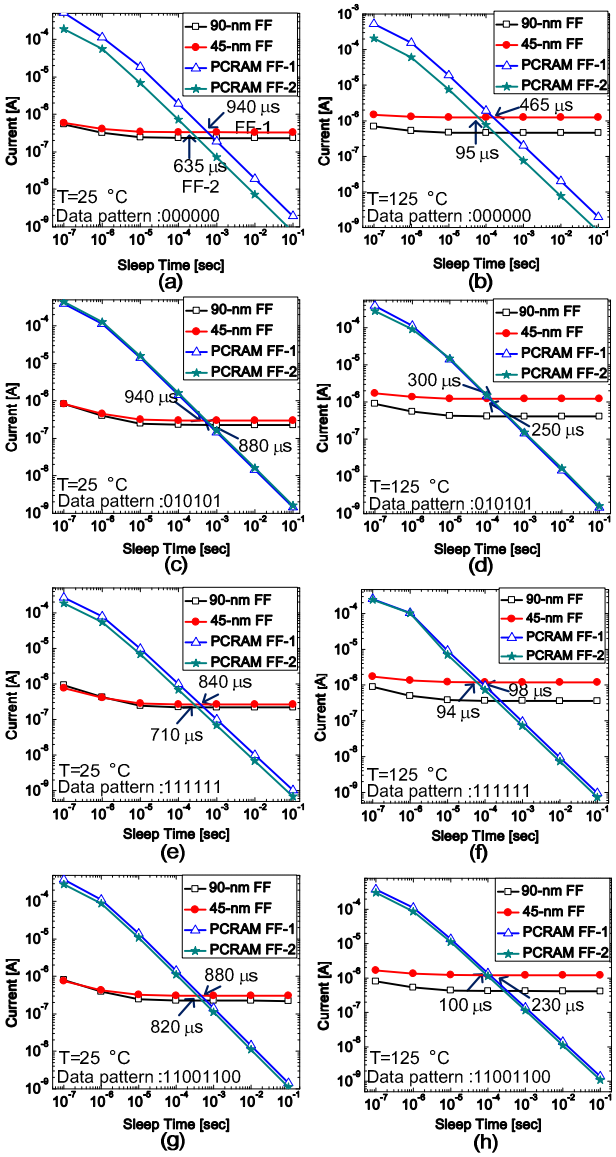

Fig. 6. Comparison of current dissipation between the conventional FFs with 45-nm and 90-nm, the FF-1, and the FF-2. Here the crossover times of FF-1 and FF-2 whose sleep energies are equal to the conventional 45-nm FF are written inside these figures. The crossover times of FF-1 and FF-2 are shown in right and left, respectively (a) Data pattern=000000, T=25 °C, (b) Data pattern=000000, T=125 °C, (c) Data pattern=101010, T=25 °C, (d) Data pattern=101010, T=125 °C, (e) Data pattern=111111, T=25 °C, (f) Data pattern=111111, T=125 °C, (g) Data pattern=11001100, T=25 °C, (h) Data pattern=11001100, T=125 °C.

FF is made of 90-nm devices. Similarly, 45-nm means the FF with 45-nm devices. The proposed FF-1 and FF-2 circuits are made of 180-nm devices with PCRAM latches. In this comparison, we used V_{DD} as low as 1 V and 1.2 V, for 45-nm and 90-nm, respectively. For the SPICE parameters of 45-nm and 90-nm, the Predictive Technology Models (PTMs) were used in this paper [7]. For simulation 180-nm devices, SAMSUNG 0.18-µm model was used. The comparison of current dissipation is done for various data patterns. Fig. 6(a) and (b) are for the data pattern of '000000' and T =25 °C and T= 125 °C, respectively. In Fig. 6(a) and (b), the 90-nm and 45-nm FFs show that the amounts of current dissipation seem saturated as the sleep time becomes longer. This is because the conventional FFs of 90-nm and 45-nm have a large amount of leakage current during the sleep time. Compared with the conventional FFs, the new FF-1 and FF-2 consume much larger power when the sleep time is short. However, as the sleep time increases, the new FF-1 and FF-2 show that the current dissipation continues to be decreased more and more without showing any saturation. The large disipation of the new FF-1 and FF-2 when the sleep time is short is due to the storing and recalling operation. Here we can define a crossover time, when the sleep energy of PCRAM FF circuit becomes equal to the conventional FF. The crossover time means that if the sleep time is longer than the crossover time, the new FF becomes better enenrgy-efficient than the conventional FF. In Fig. 6(a), when the data pattern is '000000', the crossover times of FF-1 and FF-2 for 45-nm FF are 465 µs and 95 µs, respectively, at 125 °C.

Fig. 7(a) shows the comparison of peak current between the conventional sleep-in control scheme and the proposed sequential sleep-in control scheme in Fig. 3. Fig. 7(b) shows the peak current reduction of the proposed scheme. Here we simulated 10 FF circuits with STO pulse width as long as 100 ns. The delay time used in the simulation in Fig. 7(a) and (b) was 20 ns.

The area overhead of the FF-1 circuit in Fig. 1(a) is compared with the conventional FF circuit with high V_{TH} latch. Using DONGBU 0.18-µm CMOS technology, the area overhead is estimated by 45%. One thing to note here is that the current mirrors of I_{SET}, I_{RESET}, and I_{READ} in Fig. 1(a) can be shared with the other FF-1 circuits thus they do not degrade the area overhead. The area overhead as large as 45% is mainly due to the comparator C_0 in Fig. 1(a) that is composed of differential-pair amplifier and output buffers. If we replace the comparator C_0 with the simple inverter-type comparator that is used in ref. [3], the area overhead becomes as small as 12.3%.

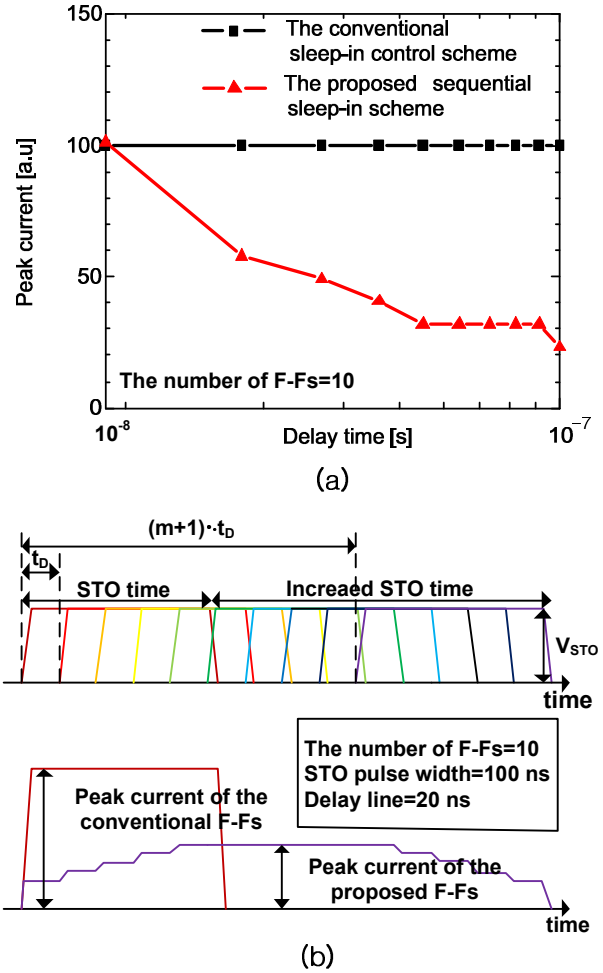

Fig. 7. (a) Comparison of peak current between the conventional sleep-in control scheme and the proposed sequential sleep-in scheme, (b) Peak current reduction of the proposed scheme.

IV. CONCLUSIONS

In this paper, the PCRAM FF-1 and FF-2 circuits were proposed not to waste leakage during the sleep time. And, also, the sequential sleep-in control was proposed to reduce the rush current peak. From the simulation results of the data pattern '000000', the proposed FF-1 wastes smaller power than the 45-nm FF if the sleep time is longer than 465 μs at 125°C. The FF-2 circuit can shorten the crossover time more as short as 95 μs at 125 °C. For the rush current peak, the sequential sleep-in control could reduce the peak as much as 77%.

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