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Analysis of Electromigration in Nanoscale CMOS Circuits†

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Abstract As CMOS technology is scaled down more aggressively, the reliability mechanism (or aging effect) caused by the diffusion of metal atoms along the conductor in the direction of the electron flow, also called electromigration (EM), has become a major reliability concern. With the present of EM, it is difficult to control the current flows of the MOSFET device and interconnect. In addition, nanoscale CMOS circuits suffer from increased gate leakage current and power consumption. In this paper, the EM effects on current of the nanoscale CMOS circuits are analyzed. Finally, this paper introduces an on-chip current measurement method providing lifetime electromigration management which are designed using 45-nm CMOS predictive technology model.

Key Words : Reliability, Aging effect, Electromigration, EM.

1. Introduction

With CMOS technology scaling, reliability issues have become an important concern to VLSI designers, especially in the nanoscale MOSFET technology [1]-[5]. Under normal operation conditions, a transistor device can be changed by various stress sources such as negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), hot carrier injection (HCI), and time-dependent dielectric breakdown (TDDB): The NBTI has become a key reliability issue in nanometer PMOS devices. It describes the parameter degradation under a negative (static) bias stress mode at elevated temperature. A corresponding dual effect, known as PBTI is seen for NMOS devices, when a positive (static) bias stress is applied across the gate oxide of the NMOS device. The HCI causes a degradation of the electrical parameters of a transistor when the transistor is switching. The TDDB causes a conduction path to form through a gate dielectric layer placed under electrical stress, leading to parametric or functional failure. These stress sources (NBTI, PBTI, HCI, and TDDB) change the threshold voltage of the transistor device, which causes temporal degradation in device reliability and even result in failures in the transistor circuits.

In addition, scaled interconnects suffer from electormigration (EM) which is the process of metalion transport due to high current density stress in metal and which can result in changes in the metal wire resistance or even catastrophic disconnections. The EM occurs in the interconnect metallization tracks. This diffusion phenomenon occurs when the current density in the tracks is sufficiently high to cause drift of the metal atoms in the direction of the electron flow. This process culminates in the formation of voids or extrusions that leads to an increase in electrical resistance or

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to a short between adjacent lines [6]-[11].

In this paper, EM impact on current flow on digital circuits is analyzed at a metal 1 layer. Finally, this paper introduces an on-chip current measurement method providing lifetime electromigration management.

2. Electromigration (EM)

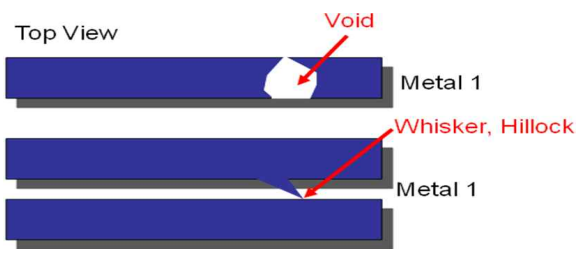
Electromigration is the diffusion of metal atoms along the conductor in the direction of the electron flow. This directional diffusion of metal is caused by the momentum transfer from electrons to atoms. Threfore, the metal atoms move in the direction of electron flow.

This diffusion process fills metal ion vacancies found in the crystal and will leave vacancies in the location from where atoms moved. This mechanism can eventually generate metal build up along the metal line (hillocks), causing shorts or opens to be left behind as shown in Fig. 1.

Electromigration degradation can affect both metal leads and Contacts/Vias. Time to Fail (TTF) of a metal lead or Contact/Via. It can be modeled using Black's equation as follows:

$$TTF = A \times \left(\frac{1}{J}\right)^n \times \left(\frac{E_a}{kT}\right) \quad (1)$$

where n and A are material constants (n=1 in TI's models), J is the current density flowing through the line, k is the Boltzman's constant, T is the Temperature, E_a is the activation energy.



<Figure 1> EM Stress

EM is degraded by the following factors:

- Leads and Vias current density: The higher the current density in the leads, the smaller TTF. For this reason, it is important to size up metal leads and increase number of Vias in interconnect to meet EM performance.
- Temperature: Higher lead temperature decreases TTF. Metal lead temperature is a function of I_{rms} (root mean square current).
- Leads microstructure (grain size/compos- ition): Usually, smaller grain size generates higher failure rate because of more grain boundaries. Also, interfaces between metal films and oxide or barriers can affect EM performance.
- Product Speed. Higher speed translates in more current through metal leads
- Current flow direction: Bipolar pulses in metal leads result in smaller EM damage than unipolar pulses. This is due to the recovery mechanisms when current flow direction is reversed in the metal lead.

3. EM Analysis

The traditional methodology calculates leads average (Iem) and rms current limits (Irms) with several approximations:

- FIT is calculated based on test structures and is not representative of product FIT.
- Current limits are not function of the current waveform. In reality, EM is affected by the duty cycle and polarity of the applied waveform. The longer the duty cycle, the higher is the impact on the EM. The more asymmetric the waveform polarity the higher EM degradation.
- Joule heating in metal wire and Vias is considered negligible as long as Irms doesn''t

exceed the required limits. However, with implementation of low-k dielectric which has about 30-35% the thermal conductivity of silicon dioxide films, Joule heating becomes very important.

- Since EM is strongly activated by temperature, Joule heating in a metal wire could contribute to a strong decrease of wire TTF.

A new methodology that overcomes all of the above assumptions and, more importantly, is based on product level FIT budget, is introduced is called self-consistent electro- migration model and allows to combine thermally dependent phenomena of Joule heating and EM wearout to give self- consistent solutions for I_{emmax} and I_{rmsmax} current limits to be used in the design.

For unipolar pulses as shown in Fig. 2, typical of power grid leads, the effective value of the current density for EM is computed from simulated values of I(t) as the average current density in Eqn. 1. The equation is given by:

$$I_{emeff} = \frac{1}{T}\int_0^T I(t)dt \qquad (2)$$

where T is the period.

For bipolar pulses as shown in Fig. 3, typical of signal leads, the effective value of the current density for EM is computed from simulated values of I(t), using the Average Recovery-Model (ACR) provided by TI that takes into account damage recovery when current flow direction is inverted. The equation is as follows:

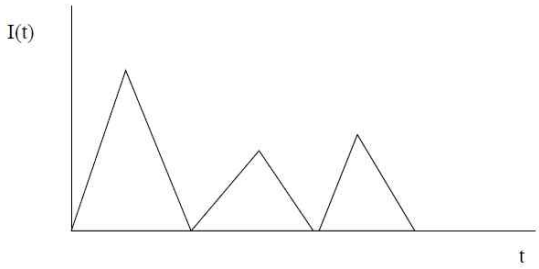
$$J_{emeff} = \frac{1}{T}\left\{\int_0^T I_{pos}dt - r\int_0^T |I_{neg}|dt\right\} \qquad (3)$$

where r is 0.6 (recover factor)

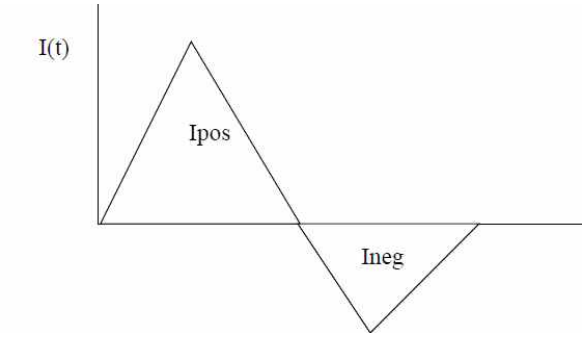
Therefore, the root mean square current is defined by Eqn. 4, and the peak current (Eqn. 5) is the maximum current for the absolute current.

$$I_S = \sqrt{\frac{1}{T}\int_0^T I^2(t)dt} \qquad (4)$$

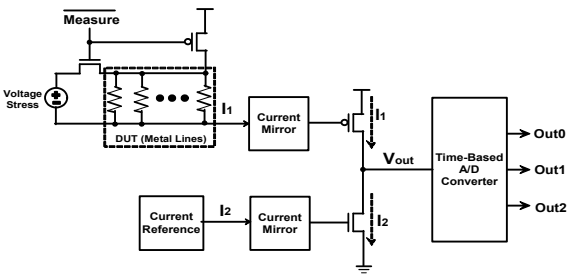
$$I_{peak} = \max(|I(t)|) \qquad (5)$$



<Figure 2> Unipolar current waveform.



<Figure 3> Biipolar current density waveform



<Figure 4> Proposed sensor circuit to predict EM.

4. Proposed EM sensor circuit

In this paper, a new EM sensor circuit is proposed. The sensor circuit uses several metal lines in parallel to predict the impact of EM as shown in Fig. 4 which can be used to estimate the accumulated damage and the remaining lifetime of metal lines. The metal lines in parallel are stressed to predict EM, and the failure of one or more metal lines during the stress condition will increase the current in the remaining lines. The increased (changed) current will be detected by a current comparator.

5. Simulation Results

In order to show the EM effect on real interconnection, a metal line considering the EM model has been implemented and evaluated HSPICE. EM current limits per metal width are provided as an example in Table 1.

<Table 1> Example of self-consistent EM limts-Metal 1 (T=105 C, LR_{crit}=30)

r	I_{emmax} (mA/um)	I_{rmsmax} (mA/um)
r15	0.2300	31.43
0.0010	0.4764	15.06
0.0015	0.5028	13.11
0.0022	0.5244	11.29
0.0032	0.5424	9.637
0.0046	0.5556	8.159
0.0068	0.5664	6.862
0.0100	0.5736	5.741
0.0147	0.5796	4.784
0.0215	0.5832	3.977
0.0316	0.5868	3.298
0.0464	0.5880	2.731
0.1000	0.5904	1.867
0.2154	0.5919	1.2740
0.4642	0.5928	0.8690
1.000	0.5928	0.5930

In order to obtain EM limits, the r factor, also called duty cycle, must be calculated using the following definition:

$$r = \left(\frac{I_{emeff}}{I_{\mathrm{seff}}} \right)^2 \tag{6}$$

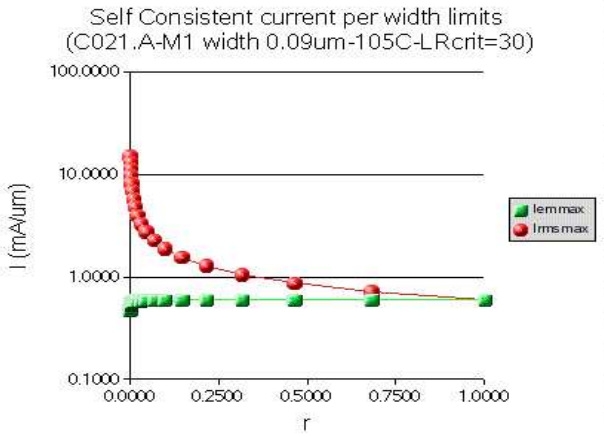
where I_{emeff} and I_{rmseff} are the effective EM current density and RMS current density obtained from simulated time dependence of current density $I(t)$.

The qualitative behavior of the self- consistent solutions as shown in Fig. 5 is as follows:

1) $r=1$ is equivalent to DC condition where there is no Joule heating (Power lines).
2) As r decreases below 1, typical of signal lines, Jem limit will decrease as wire temperature (Joule heating) increases.
3) For upper metal leads, I_{emmax} decreases faster for smaller r than lower metal leads, due to increased distance of wire from substrate and increased Joule heating.
4) Limits are different for different metal widths.
5) Current density limits are set to guarantee that product total EM FIT doesn't exceed 10.

These tables are generated by using thermal simulations of specific structures incorporating dummy metal, nominal metal stack thicknesses and widths and material conductivity. In order to use current density tables, designers must extract I_{emeff} and I_{rmseff} at ffnh corner and calculate duty cycle factor, r, from Eqn. 6.

For a given value of r from simulations, the closest smaller value of r must be used in the table. The metal wire under analysis must not exceed correspondent I_{emmax} and I_{rmsmax} limits. Current limits for $r15$ are used when r is smaller than minimum r value reported in the table. J_{rmsmax} value correspondent to $r15$ is also used as $J_{peakmax}$.



<Figure 5> EM self-consistent solutions.

6. Conclusion

In this paper, the EM effects on current flow of the nanoscale CMOS circuits are analyzed using a metal line. The qualitative behavior of the self-consistent solutions has been presented in the simulation results. Finally, Finally, this paper introduces an on-chip current measurement method providing lifetime electromigration management.

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