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Comparative Analysis of Three-Phase AC-DC Converters Using HIL-Simulation

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Abstract

This paper presents a comparative evaluation of various topologies for three-phase power converters using the hardware-in-the-loop (HIL) simulation technique. Various switch-mode AC-DC power converters are studied, and their performance with respect to total harmonic distortion (THD), efficiency, power factor and losses are analyzed. The HIL-simulation is implemented in an Altera Cyclone II DE2 Field Programmable Gate Array (FPGA) Board and in the Matlab/Simulink environment. A comparison of the simulation and HIL-simulation results is also provided.

Key words: FPGA, Hardware-in-the-loop (HIL), Simulation, Three-phase AC-DC converters

I. INTRODUCTION

The advances in power semiconductor devices have catapulted numerous studies on pulse width modulation (PWM) techniques to improve the quality of sinusoidal input current so that the current adheres to harmonic standards such as IEEE Std. 519, IEC 1000-3-2 and IEC 61000-3-2. As a result, a significant number of PWM switch-mode AC-DC power converters have been proposed to replace conventional diode rectifiers to achieve a pure sinusoidal input current with a low total harmonic distortion (THD) and a unity power factor [1]-[5]. Various topologies such as buck, boost, and buck-boost have been developed so that the output voltage can be controlled to a desired value while reducing harmonic currents.

For low and medium voltage DC loads requirements, buck switch-mode rectifiers have been proposed to step-down the output voltage [3], [6]-[8]. However, these converters are not suitable for step-up voltage conversions. To produce a high DC voltage, boost rectifiers have been proposed in [9]-[11]. Due to inductors placed in series with the inputs, boost converters draw a continuous current flow and contain a low switching frequency content. These features give boost converters an advantage over current-source buck converters, which draw pulse width modulated currents [12]. However, recent technological developments require power supplies with wider conversion rates especially in photovoltaic applications and electric vehicle technologies. Wider conversion ratios can be obtained by adjusting the modulating control signal of the converter. In practice, the attainability of the conversion ratios is limited, especially when the duty ratio is nearing 0 or 1. As a result, major deterioration of the output voltage and inductor current signals occur. Another approach is the use of transformers to step-up/down the DC output. However, limited power capacity, design complexity, poor cross regulation, and high inrush currents are some of the drawbacks of using a transformer [13]. To achieve a wider conversion ratio, cascaded converters have been proposed, where two or more converters are connected together in a multistage operation [13]-[16].

Progress in digital technologies such as field programmable gate arrays (FPGAs) has enabled engineers to develop complex controllers without considerable hardware modifications. The integration of software and a FPGA for real-time simulation has been done in [17]-[19]. Hardware-in-the-loop simulation is a tool for the implementation and verification of a controller's functionality without increasing the risk of damaging the prototype during actual testing. Moreover, conventional simulations do not consider the resolution limit of the processor chip. By implementing a discretized model for simulation accuracy, the controller design can be tested under realistic conditions.

In this paper, a performance study of various AC-DC converters based on HIL-simulations is presented. The simulation model is done in the Matlab/Simulink environment. An Altera DSP Builder, containing high-level algorithm very-high-speed hardware descriptive language (VHDL), is integrated with the Simulink blocks to create a hardware/software co-simulation model. The comparison is done with respect to the converters' efficiencies, the total

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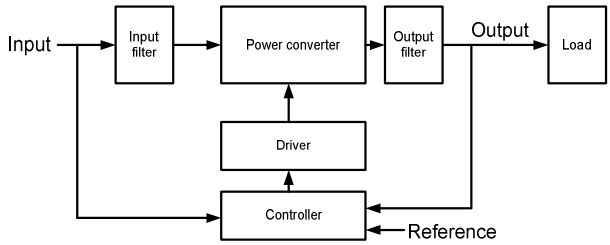


Fig. 1. Three-phase power converter system.

harmonic distortions (THDs), the power factors, and the conversion ratios. The four topologies compared in this paper are: (1) a conventional three-phase buck-boost converter, (2) a three-phase four-switch buck-boost converter, (3) a three-phase buck + boost converter, and (4) a three-phase buck converter with a modified boost output stage.

II. THREE-PHASE AC-DC PWM RECTIFIERS

There are a few papers in the literature concerning three-phase buck-boost converters. Several topologies for AC-DC switch-mode rectifiers, either in single-stage or multi-stage, have been introduced [1, 2, 14, 20-23]. Generally, the power converter system is illustrated in Fig.1.

A. Conventional Three-phase Buck-boost Converter

Fig. 2(a) shows a conventional three-phase buck-boost converter. A diode bridge is connected to an IGBT switch, S_1, and the inductor L_1 receives energy when the switch is conducting and none of the energy goes through the output due to a diode that is reverse biased.

The inductor discharges the energy to the output capacitor and the load when the switch is turned off and the supply is cut off from the output. Thus the inductor current decreases as the DC capacitor is negatively charged during the freewheeling interval. Therefore, the DC output voltage has an inverting polarity from the input as expressed below:

$$V_o = -\sqrt{\frac{3}{2}}\frac{D}{1-D}V_{LL} \tag{1}$$

where where D is the duty cycle ($0 \le D \le 1$), V_{LL} is the line-to-line source voltage, and V_O is the output voltage. From the observations above, the buck-boost topology is the only "pure flyback" topology around, in the sense that all of the energy transferred from the input to the output must have been previously stored in the inductor.

Although the conventional converter design is simple, it produces non-sinusoidal input currents as shown in Fig. 2(b) and the current appears for only 2/3 of the half cycle. Thus the current contains high harmonic components. Some negative consequences of these harmonics are an increase in the power loss, excessive stress on the components, heating of the equipment, voltage sags, power factor reduction, overdimensioning of the conductors, and deterioration of the power quality [24].

B. Three-phase Four-switch Buck-boost Converter

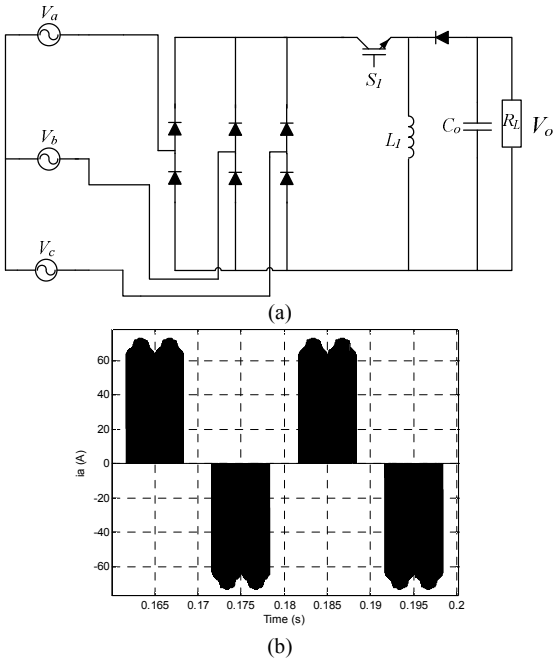


Fig. 2. (a) Conventional three-phase buck-boost converter, (b) Waveform of input current of phase *a*.

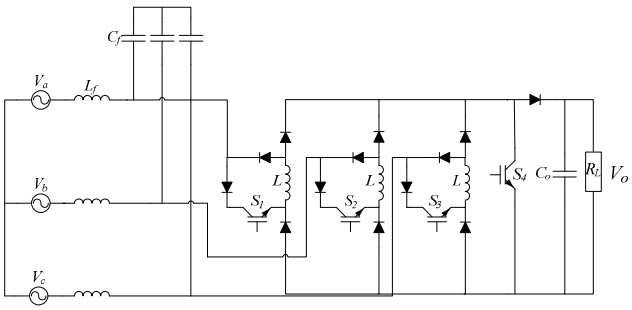


Fig. 3. Three-phase four-switch buck-boost converter.

A three-phase four-switch buck-boost converter has been introduced in [2]. It operates in discontinuous conduction mode (DCM). This converter solves the sixth times line problem that often appears at the ripple of the output voltage.

The circuit configuration is shown in Fig. 3, in which each leg is connected to four diodes, a semiconductor switch and an inductor. The four switches are concurrently controlled by one PWM signal. Thus the charging and discharging of the inductors occur in parallel mode, providing a faster response for the energy transfer to the load. In short, fewer passive components are used during circuit implementation. The voltage conversion ratio is given by:

$$\frac{V_o}{V_{LL}} = \sqrt{\frac{1}{3}}\frac{D}{1-D} \tag{2}$$

C. Three-phase Buck + Boost Converter

A three-phase buck + boost converter has been described in [14] as shown in Fig. 4. The buck rectifier stage is based on [25]. Each phase of the supply is connected to the inductor. The switching is modulated by sinusoidal PWM (SPWM) and

is divided into six equal-time intervals of the 360° mains cycle. There are two modes of operation: (a) only two switches are modulated and the third is in the on state, and (b) only one switch is conducting and the other two are in the off condition, thus providing a freewheeling path for the inductor current when all of the input currents are zero. In other words, one switch remains in the continuous conduction mode for a sextant of the mains cycle. The reference sine wave needs to be phased locked to the supply voltage.

The boost stage is activated only when a higher level of DC output voltage has to be achieved. The switches at the buck-input stage and the boost-output stage use the same switching frequency in this paper for ease of PWM control implementation.

The voltage conversion ratio is given by:

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{3}$$

where V_i is the bridge voltage.

D. Three-phase Buck-boost Converter with a Modified Boost Output Stage

Fig. 5 shows the proposed converter, which utilizes a three-phase buck converter and is cascaded with a modified boost output stage. The circuit is designed to achieve a high DC voltage gain. At the DC bus stage, the cascaded boost converter employs a voltage multiplier cell so that even with a small duty cycle, a wider conversion ratio can be obtained. The converter operates in continuous conduction mode (CCM). For simplicity, only one PWM signal operates switches S_4 and S_5. The expression for the cascaded boost converter is derived by assuming a steady-state condition.

$$V_{Lm} DT_S = V'_{Lm}(1-D)T_S \tag{4}$$

$$V_{L1} DT_S = V'_{L1}(1-D)T_S \tag{5}$$

$$V_{L2} DT_S = V'_{L2}(1-D)T_S \tag{6}$$

The operating principle is described as follows:

Mode I: S_4 and S_5 are turned on. The diodes D_1, D_2, and D_3 are blocked. The equivalent inductor, L_m, is receiving energy from the DC bus. The energy stored in C_1 is discharged. The voltage, V_{C3}–V_{C2}, is applied across the inductor, V_{L2}.

$$V_i = V_{Lm} \tag{7}$$

$$V_{C1} = V_{L1} \tag{8}$$

$$V_{L2} = V_{C3} - V_{C2} \tag{9}$$

Mode II: S_4 and S_5 are turned off. The diodes D_1, D_2 and D_3 start conducting. The energy stored inside L_m is transferred to the capacitor, C_1, and the energy stored in L_2 is transferred to the output through the output diode, D_3.

$$V'_{Lm} = V_{C1} - V_i \tag{10}$$

$$V'_{L1} = V_{C3} - V_{C1} \tag{11}$$

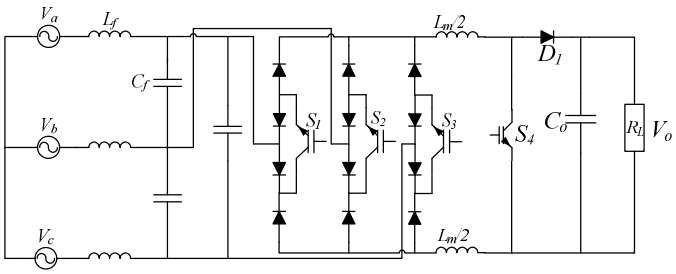


Fig. 4. Three-phase buck + boost rectifier [14].

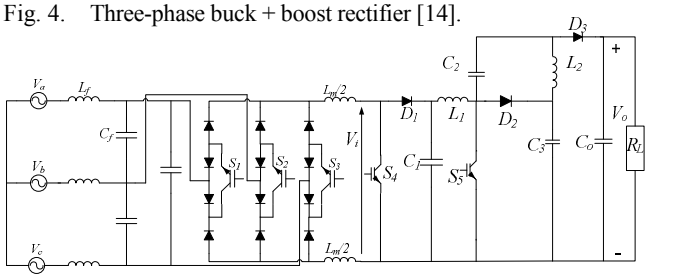


Fig. 5. Proposed three-phase buck-modified boost converter.

$$V'_{L2} = V_{C2} \tag{12}$$

$$V_{C3} + V'_{L2} = V_o \tag{13}$$

Thus the conversion ratio can be expressed as:

$$\frac{V_o}{V_i} = \frac{1+D}{(1-D)^2} \tag{14}$$

The input filter design for the converters discussed in this paper is based on:

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{15}$$

where f_r is the resonant frequency, f_c is the carrier frequency, L_f is the input filter inductor, and C_f is the input filter capacitor. The selection of the capacitor and the inductor must comply with $f_r << f_c$ in order to avoid resonance effects and to ensure carrier attenuation [5].

III. HIL DESIGN DESCRIPTION

The circuit simulation model and the PWM controller are implemented based on the process flow shown in Fig. 6. The power converters are modeled in the Matlab/Simulink environment and the PWM control is developed by using Altera DSP Builder blocks as depicted in Fig. 1. The DSP Builder allows the integration of VHDL codes and the simulation models in the Matlab/Simulink environment.

The signal compiler block generates the HDL code of the PWM controller design. Then Altera Quartus II can analyze, synthesize, and fit the design based on the Altera Cyclone II DE2 FPGA board settings. The signals are converted into a fixed-point system with a single-tasking mode. The three-phase SPWM controller design is shown in Fig. 7, and the SPWM DSP Builder model is shown in Fig. 8 (a), (b) and (c).

The design can be divided into two units: the modulator unit

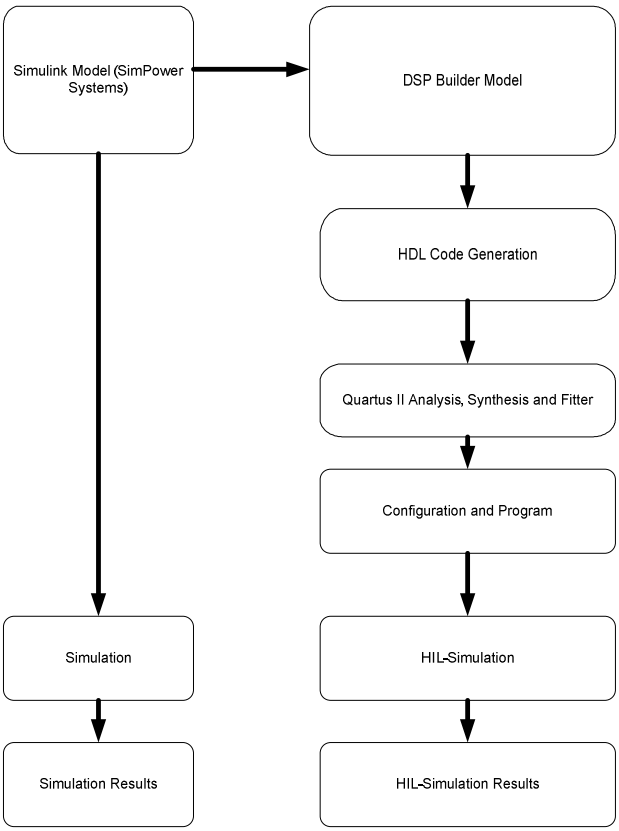


Fig. 6. HIL-Simulation Process Flow.

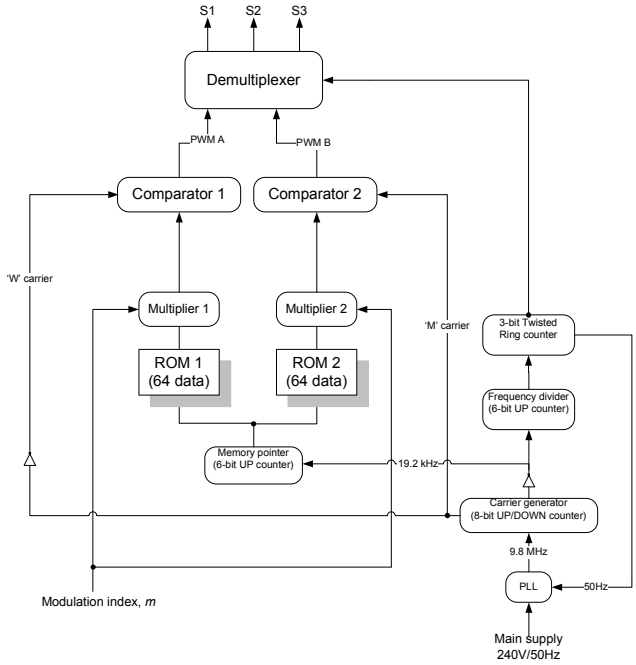


Fig. 7. Block diagram of three-phase PWM generator for three-phase buck rectifier.

and the synchronization unit. The modulator unit, which consists of carrier and sine reference generators, produces PWM gating signals. The carrier signal is generated based on the expression [26]:

$$f_c = \frac{f_{clk}}{(2^n - 1) \cdot 2} \tag{16}$$

where f_c is the carrier frequency, f_{clk} is the main FPGA clock frequency, and n is the number of bits of the UP/DOWN counter. The number of bits determines the resolution of the system. Thus the number of carrier pulses per half-cycle can be determined from the following expression:

$$f_c = \frac{2p}{T_m} \tag{17}$$

where p is the number of carrier pulses per half cycle, and T_m is the period of the modulating signal.

The reference sinusoidal waveform uses two 60-degree-data, (0^o – 60^o) and (120^o – 180^o). The data are stored in sequential addresses in ROM look-up tables. A 6-bit binary counter acts as a memory pointer to address the data in the ROM and the sine wave samples are updated by clocking the counter. The sinusoidal look-up table is generated from the equation below:

$$V_{2k+1} = A \sin(\frac{2\pi f_m (2k+1)}{2 f_c}) \tag{18}$$

where f_c is the carrier frequency, f_m is the modulating frequency (50Hz), A is the sampled magnitude, and k is the pulse position.

A comparison of the reference sine wave with the W-shaped carrier and the M-shaped carrier is explained in [27]. The concept is shown in Fig. 9. V_{ref1}, V_{ref2} and V_{ref3}, which correspond to modulus three-phase waveforms, are compared to high-frequency carrier signals to generate the PWM signals S1, S2 and S3, respectively.

A 3-bit twisted ring counter operates with a clock signal of 300 Hz and generates a 50 Hz signal, which is fed back to the phase-locked loop (PLL) for synchronization. At the same time, the output of the ring counter is also used as a selector for the de-multiplexing operation.

For HIL-simulation, the PLL is modeled in Simulink, as illustrated in Fig. 10. The phase detector compares the signal from the frequency divider in the FPGA and the reference signal, and makes any necessary adjustments based on the difference to ensure that the frequency and the phase are the same for both signals. The output signal with the frequency, f_{out}, is fed into the FPGA as a clock signal. The relationship between the grid frequency, f_{ref}, and output frequency, f_{out}, is given as:

$$f_{out} = N f_{ref} \tag{19}$$

and the PLL transfer function is expressed as:

$$G(s) = \frac{K_p K_F(s) K_V}{s + \frac{K_p K_F(s) K_V}{N}} \tag{20}$$

where K_p is the gain of the phase detector, K_F is the transfer

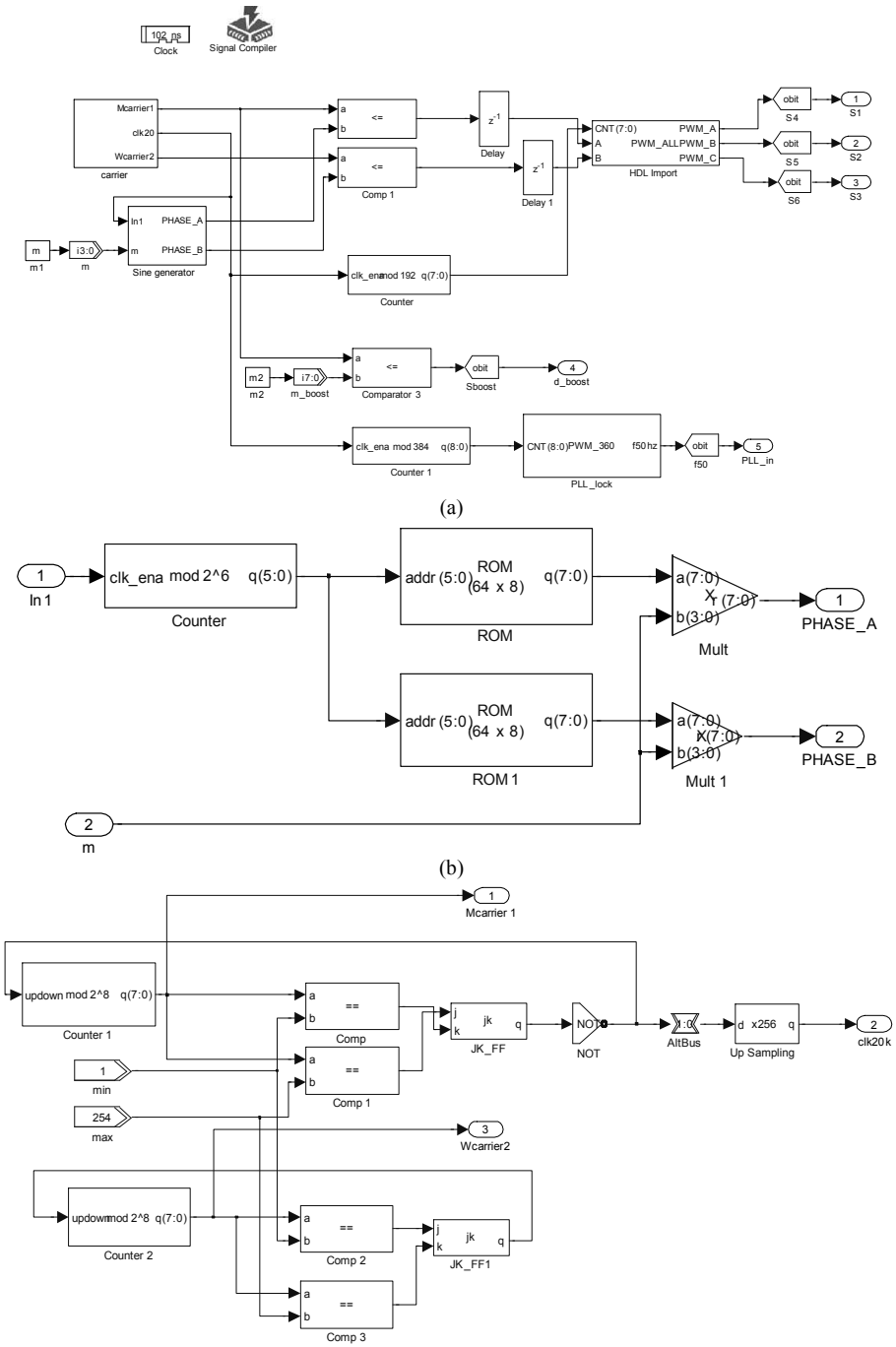


Fig. 8. (a) SPWM control model in DSP Builder, (b) Sine waveform generation from look-up tables, (c) Carrier signal circuit.

function of the low pass filter, K_V is the is the gain of the VCO, and N is the counter value generated from the FPGA.

Fig. 11(a) and (b) show the settings of the HIL block. The block configures the FPGA board and compiles the codes to be programmed into the FPGA for hardware and software co-simulation. When it is implemented into the FPGA, the modified SPWM design uses less than 1% of the total memory and logic elements.

IV. Results and Discussions

To illustrate the performance of the three-phase converters, the parameters in TABLE I are used based on the circuit configurations in Fig. 2 to Fig. 5.

The sampling time for the HIL-simulation is 102ns. A burst mode operation is used to speed-up the process. As a result, a latency of 1024 bits is introduced into the outputs. TABLE II summarizes the comparison, in terms of the displacement factor (DF), the current THD, and the output voltage, V_o, between both of the simulation methods at D=0.5.

The three-phase four-switch buck-boost converter and the conventional converter employ a simple PWM controller when compared to other converters discussed in this paper. It takes

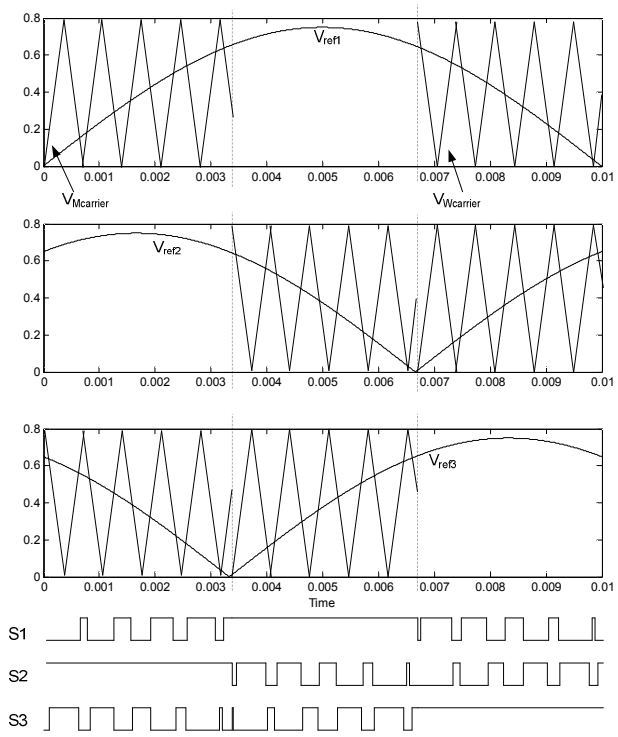


Fig. 9. Comparison of reference signals with carrier signals for PWM generation.

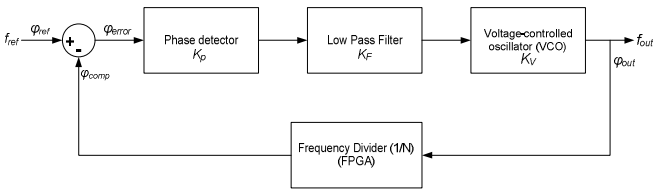
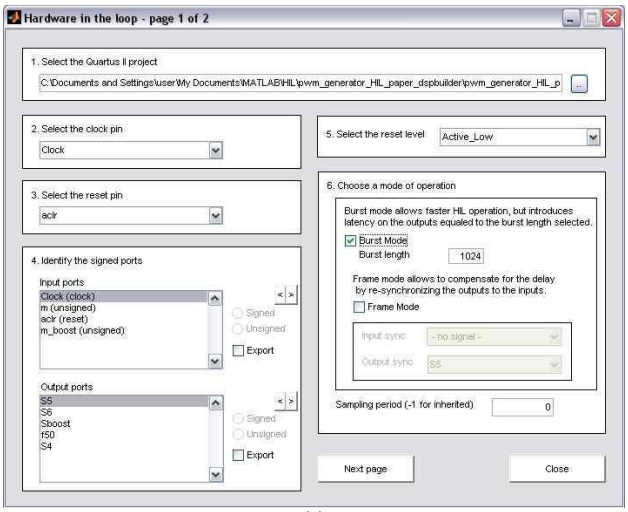


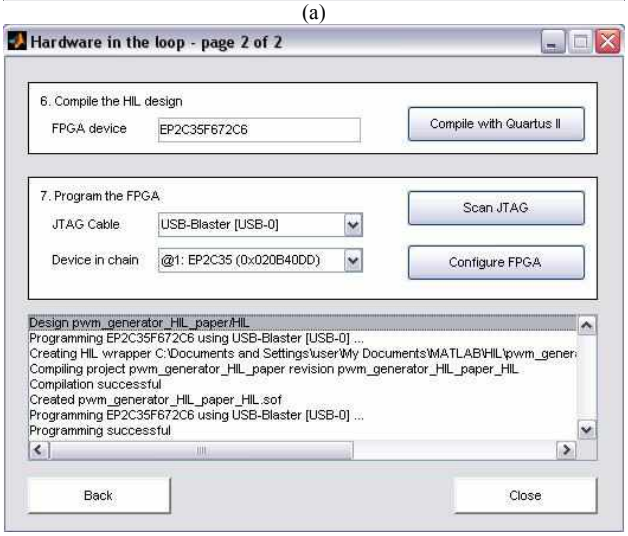
Fig. 10. PLL frequency multiplier block diagram.

less computational time for the FPGA to generate PWM signals. Thus the deviation of the displacement factor between the HIL-simulation and the simulation is almost negligible. However, the three-phase buck+boost and the buck-modified boost rectifiers employ a modified SPWM scheme that takes more calculation time in a FPGA. As a result, the displacement factor between the source voltage and the current is less than unity. To improve the displacement factor, a PLL model is employed in the HIL-simulation method. By referring to TABLE II, it can be seen that the THD and the output voltage have improved when the displacement factor has been optimized.

Fig. 12 (a) and (b) show that the conversion ratios obtained from the two simulation methods are in close agreement. The gain is the ratio of the output voltage, V_O, and the line voltage, V_{in}. The buck-modified boost rectifier illustrates the highest gain among the four converters. The conventional buck-boost and the four-switch buck-boost rectifiers also produce gain that behaves exponentially as the modulation index increases, and the buck+boost converter has a slight reduction of the gain at D=0.9.



(a)



(b)

Fig. 11. (a) Configuration of FPGA board, (b) Compiling and programming the VHDL codes into the FPGA.

Fig. 13 (a), (b), and (c) show the HIL-simulation results of the current THD, the power factor and the efficiency of the various three-phase rectifier configurations. Interestingly, the three-phase buck-modified boost produces a minimum output power that is above 300W. Thus there is no result at 200W for this converter.

The buck+boost converter has a constant THD of about 7% as the output power increases to over 400W, and the conventional buck-boost rectifier shows the highest THDs due to the high level of harmonics in the phase currents. The current THD for the four-switch and the buck-modified boost converters at a 1kW load are 3.3% and 5%, respectively.

The single-stage four-switch buck-boost, buck+boost, and the buck-modified boost converters display a high power factor. However, high RMS harmonic level in the phase currents results in a low power factor for the conventional converter. Thus lower efficiency is produced for the latter.

At a 1kW load, multi-stage converters, i.e. the buck+boost, and the buck-modified boost, generate a lower efficiency when

TABLE I
CONVERTER SPECIFICATIONS AND PARAMETERS

Input phase voltage, V_{in}	120Vrms
Supply frequency, f_m	50Hz
Switching frequency, f_s	19.2kHz
L_f	1mH
C_f	1uF
C_1	1uF
C_2-C_3	680nF
C_o (3-phase buck+boost rectifier)	1000uF
C_o (3-phase 4-switch buck-boost rectifier)	660uF
C_o (Conventional 3-phase buck-boost, and buck- modified boost rectifiers)	470uF
L_1-L_2	1mH
L_m	12mH
L	115uF
IGBT model	IRGP20B120U
Diode model	30CPF10

TABLE II
COMPARISON RESULTS BETWEEN HIL-SIMULATION AND SIMULATION

			3-phase buck +boost	3-phase 4-switch buck-boost	Conventiona l 3-phase buck-boost	3-phase buck-modifi ed boost
Simulation	THD (%)		4.55	5.06	119	3.3
	DF		0.99	0.99	0.99	0.99
	Vo (V)		300	271	-278	600
HIL-Simulation	THD (%)	without PLL	7.15	5.22	120	4.02
	DF	without PLL	0.93	0.99	0.99	0.92
	Vo (V)	without PLL	262	273	-282	511
	THD (%)	with PLL	4.11	N/A	N/A	3.74
	DF	with PLL	0.98	N/A	N/A	0.99
	Vo (V)	with PLL	278	N/A	N/A	550

compared to the single stage four-switch buck-boost rectifier.

The loss analysis consists of conduction and switching losses in the IGBT and diodes. Unfortunately, the analysis does not consider the losses from passive components. The local switching loss, P_{sw}, is calculated from the results obtained from both simulation techniques, by summing the switching occurrences during a pulse period as given below:

$$P_{sw} = f_s \sum_{\substack{switching \\ transitions}} (E_{on} + E_{off} + E_{rr}) \qquad (21)$$

where E_{on} is the turn-on energy loss, E_{off} is the turn-off energy loss, and E_{rr} is the diode reverse recovery energy loss.

The conduction loss, P_{cond}, is calculated during the on-state voltage drop across the semiconductor device and the current

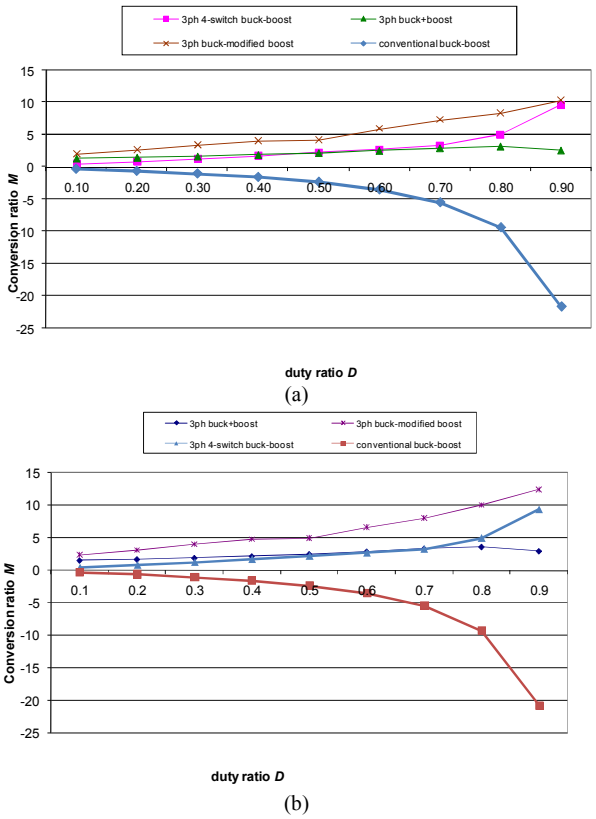


Fig. 12. Comparison of the gain between various converters based on (a) HIL-simulation, (b) simulation.

through it. The resistances of the junction diode, R_F, and the IGBT, R_T, are taken at the highest junction temperature [28]. The conduction loss is derived by averaging the instantaneous power over the line frequency. The calculation of the losses is not accurate since the capacitive parasitic elements and the recovery time are not optimally modeled in Matlab/Simulink. The conduction losses for every switching cycle in the IGBT, P_{cond_s}, and in the diode, P_{cond_D}, are expressed in Eq. (22) and (23) below:

$$P_{cond\_s} = I_T^2 R_T \qquad (22)$$

$$P_{cond\_D} = V_D I_D + I_F^2 R_F \qquad (23)$$

where I_T is the RMS current flowing through the IGBT, V_D is the forward voltage of the diode, I_D is the average current in the diode, R_F is the dynamic resistance of the junction at I_D, and I_F is the RMS current flowing through the diode. The IGBT and diode models used in the calculations are based on the IRGP20B120U and the 30CPF10, respectively, by International Rectifier.

Fig. 14 shows the losses generated by the four converters. As can be seen, the generated losses for each converter are higher when using the HIL-simulation method. The simulation results show that the conventional buck-boost rectifier produces the highest total loss as a result of the large stress imposed on the single IGBT switch. The buck+boost rectifier generates about 93% of the total loss yielded by the conventional converter.

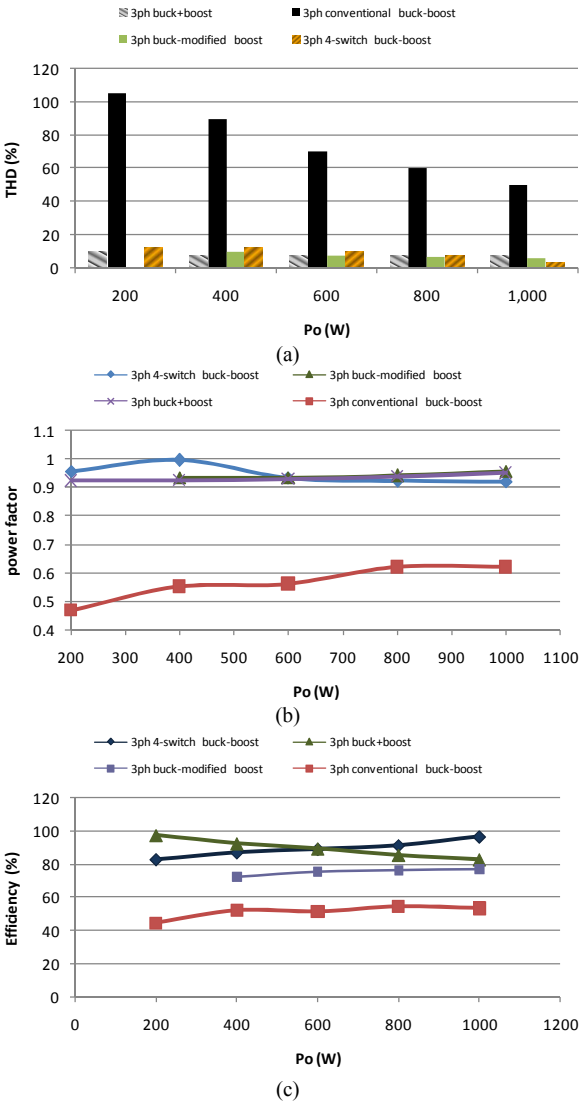


Fig. 13. Comparison of performance between various three-phase rectifier configurations (a) current THD, (b) power factor (c) Efficiency.

The corresponding figures are 67% for the four-switch buck-boost rectifier and 95% for the buck-modified boost converter.

The losses calculated from the HIL-simulation method shows the conventional converter is 1.5% lower than the total losses obtained from the three-phase buck-modified boost rectifier. The buck+boost rectifier generates about 88.4% of the losses generated by the buck-modified boost rectifier, and 58% for the four-switch buck-boost rectifier.

Finally, both simulation methods show that high switching stress is imposed on the single IGBT switch in the conventional circuit when compared with the other circuit configurations.

V. CONCLUSIONS

A comparative study of various three-phase AC-DC rectifier configurations based on a Altera Cyclone II DE2

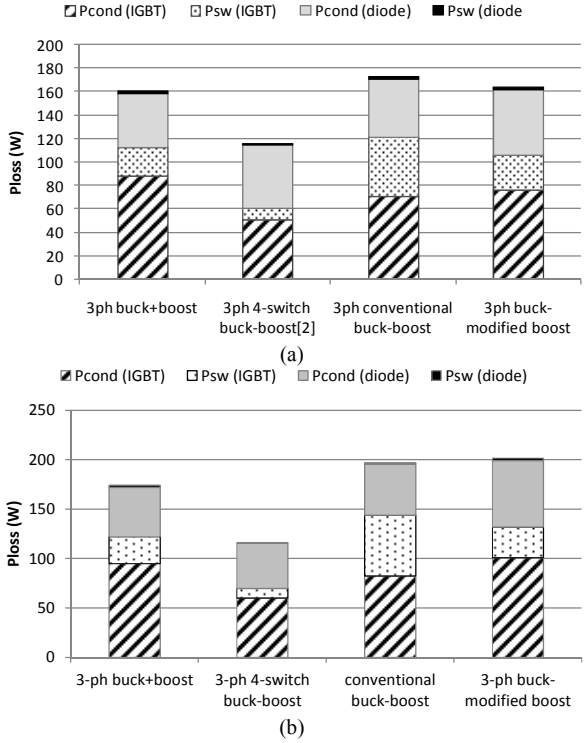


Fig. 14. Loss comparison between various configurations of three-phase buck-boost rectifier at 1kW load by (a) simulation, and (b) HIL-simulation.

Field Programmable Gate Array (FPGA) Board and the Matlab/Simulink environment has been presented. HIL-simulation provides an alternative approach for the implementation and verification of a controller's functionality with a few limitations such as a prolonged simulation time when the time-step is reduced to synchronize with a FPGA clock, and the limited memory allocation of the results. The prolonged calculation time in a FPGA for HIL-simulation affected the displacement factor, which has been optimized by including a PLL circuit in the model. The performance of the converters in terms of THD, power factor and efficiency depends on the switching configurations and the number of semiconductor devices in the circuit. Although the conventional buck-boost rectifier has the lowest number of semiconductor devices, the non-sinusoidal current drawn from the converter contains harmonics, which originate from the circulating RMS current. While some electronic equipment may be able to tolerate the presence of harmonics, vulnerable equipment will suffer from dielectric thermal or voltage stresses that cause premature aging of the electrical insulation. The single-switch conventional rectifier sacrifices harmonic performance and efficiency to achieve a lower production cost. At the same time, utilizing switching devices and complex control systems are necessary to meet lower harmonics and high power factor requirements.

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REFERENCES

[1] A. M. Omar and N. A. Rahim, "FPGA-based ASIC design of the three-phase synchronous PWM flyback converter," in *IEE Proc.-Electr. Power Appl.*, pp. 263-268, 2003.

[2] L.-S. Yang, T.-J. Liang, and J.-F. Chen, , "Analysis and Design of a Novel Three-Phase AC-DC Buck-Boost Converter," *IEEE Trans. Power Electron.,* Vol. 23, No.2, pp. 707-714, Mar. 2008.

[3] A. Stupar, T. Friedli, J. Miniboeck, and J. Kolar, "Towards a 99% Efficient Three-Phase Buck-Type PFC Rectifier for 400 V DCDistribution Systems," *IEEE Trans. Power Electron.,* Vol. PP, No.99, pp. 1-1, Sep. 2011.

[4] Y. Neba, K. Ishizaka, and R. Itoh, "Single-phase two-stage boost rectifiers with sinusoidal input current," *Power Electronics, IET,* Vol. 3, No.2, pp. 176-186, Mar. 2010.

[5] N. A. Rahim, "Closed-loop control of a current-mode ac/dc buck converter in 4 quadrant p-q operation," PhD. Thesis, Heriot-Watt University, Edinburgh, 1995.

[6] T. Nussbaumer, M. Baumann, and J. W. Kolar, "Comprehensive design on a three-phase three-switch buck-type pwm rectifier," *IEEE Trans. Power Electron.,* Vol. 22, pp. 551-562, Mar. 2007.

[7] T. C. Green, M. H. Taha, N. A. Rahim, and B. W. Williams, "Three-phase Step-down reversible ac-dc power converter," *IEEE Trans. Power Electron.,* Vol. 12, No.2, pp. 319-324, Mar. 1997.

[8] D. Z. B. Ye, "A novel modeling and control approach for parallel three-phase buck rectifiers," presented at the Conference Record of the 2001 IEEE Industry Applications Conference, 2001.

[9] P. Barbosa, F. Canales, J. C. Crebier, and F. C. Lee, "Interleaved three-phase boost rectifiers operated in the discontinuous conduction mode: analysis, design considerations and experimentation," *IEEE Trans. Power Electron.,* Vol. 16, No. 5, pp. 724-734, Sep. 2001.

[10] P. J. Grbovic, P. Delarue, and P. Le Moigne, "A novel three-phase diode boost rectifier using hybrid half-dc-bus-voltage rated boost converter," *IEEE Trans. Ind. Electron.,* Vol. 58, No.4, pp. 1316-1329, Apr. 2011.

[11] G. Franceschini, E. Lorenzani, M. Cavatorta, and A. Bellini, "3boost: a high-power three-phase step-up full-bridge converter for automotive applications," *IEEE Trans. Ind. Electron.,* Vol. 55, No. 1, pp. 173-183, Jan. 2008.

[12] T. C. Green, "The impact of EMC regulations on mains-connected power converters," *Power Engineering Journal,* Vol. 8, No. 1, pp. 35-43, Feb. 1994.

[13] M. G. Ortiz-Lopez, J. Leyva-Ramos, E. E. Carbajal-Gutierrez, and J. A. Morales-Saldana, "Modelling and analysis of switch-mode cascade converters with a single active switch," *Power Electronics, IET,* Vol. 1, No. 4, pp. 478-487, Dec. 2008.

[14] M. Baumann and J. W. Kolar, "A novel control concept for reliable operation of a three-phase three-switch buck-type unity-power-factor rectifier with integrated boost output stage under heavily unbalanced mains condition," *IEEE Trans. Ind. Electron.,* Vol. 52, No. 2, pp. 399-409, Apr. 2005.

[15] J. A. Morales-Saldana, E. E. C. Gutierrez, and J. Leyva-Ramos, "Modeling of switch-mode dc-dc cascade converters," *IEEE Trans. Aerosp. Electron. Syst.,* Vol. 38, No. 1, pp. 295-299, Jan. 2002.

[16] H. Matsuo and K. Harada, "The cascade connection of switching regulators," *IEEE Trans. Ind. Appl.,* Vol. IA-12, No. 2, pp. 192-198, Mar. 1976.

[17] O. Jingzhao and V. K. Prasanna, "Matlab/simulink based hardware/software co-simulation for designing using fpga configured soft processors," in *Parallel and Distributed Processing Symposium, 2005. Proceedings. 19th IEEE International*, pp. 148b-148b, 2005.

[18] D. Mic, S. Oniga, E. Micu, and C. Lung, "Complete hardware / software solution for implementing the control of the electrical machines with programmable logic circuits," in *Optimization of Electrical and Electronic Equipment, 2008. OPTIM 2008. 11th International Conference on*, pp. 107-114, 2008.

[19] H. Sunan and T. Kok Kiong, "Hardware-in-the-Loop Simulation for the Development of an Experimental Linear Drive," *IEEE Trans. Ind. Electron.,* Vol. 57, No. 4, pp. 1167-1174, Apr. 2010.

[20] P. F. de Melo, R. Gules, E. F. R. Romaneli, and R. C. Annunziato, "A modified sepic converter for high-power-factor rectifier and universal input voltage applications," *IEEE Trans. Power Electron.,* Vol. 25, No. 2, pp. 310-321, Feb. 2010.

[21] C. T. Pan and T. C. Chen, "Step-up/down three-phase AC to DC convertor with sinusoidal input current and unity power factor," *Electric Power Applications, IEE Proceedings -,* Vol. 141, pp. 77-84, 1994.

[22] U. Kamnarn and V. Chunkag, "Analysis and design of a modular three-phase ac-to-dc converter using cuk rectifier module with nearly unity power factor and fast dynamic response," *IEEE Trans. Power Electron.,* Vol. 24, No. 8, pp. 2000-2012, Aug. 2009.

[23] R. Itoh and K. Ishizaka, "Three-phase flyback AC-DC converter with sinusoidal supply currents," in *IEE Proceedings-B*, pp. 143-151, 1991.

[24] K. N. Sakthivel, S. K. Das, and K. R. Kini, "Importance of quality AC power distribution and understanding of EMC standards IEC 61000-3-2, IEC 61000-3-3 and IEC 61000-3-11," in *Electromagnetic Interference and Compatibility, 2003. INCEMIC 2003. 8th International Conference on*, pp. 423-430, 2003.

[25] L. Malesani and P. Tenti, "Three-Phase AC/DC PWM Converter with Sinusoidal AC Currents and Minimum Filter Requirements," *IEEE Trans. Ind. Appl.,* Vol. IA-23, No. 1, pp. 71-77, Jan. 1987.

[26] N. A. Rahim, T. C. Green, and B. W. Williams, "PWM ASIC design for the three-phase bi-directional buck converter," *International Journal of Electronics,* Vol. 81, No. 5, pp. 603-615, Nov. 1996.

[27] S. R. S. Raihan and N. A. Rahim, "FPGA-based PWM for three-phase SEPIC rectifier," *IEICE Electronics Express,* Vol. 7, No. 18, pp. 1335-1341, 2010.

[28] C. P. Basso, *Switch-mode power supplies: SPICE simulations and practical designs*: McGraw-Hill, Chap.6, 2008.

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