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Novel Zero-Voltage-Switching Bridgeless PFC Converter

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Abstract

In this paper, a new zero-voltage-switching, high power-factor, bridgeless rectifier is introduced. In this topology, an auxiliary circuit provides soft switching for all of the power semiconductor devices. Thus the switching losses are reduced and the highest efficiency can be achieved. The proposed converter has been analyzed and a design procedure has been introduced. The control circuit for the converter has also been developed. Based on the given approach, a 250 W, 400 Vdc prototype converters has been designed at 100 kHz for universal input voltage (90-264 Vrms) applications. A maximum efficiency of 94.6% and a power factor correction over 0.99 has been achieved. The simulation and experimental results confirm the design procedure and highlight the advantages of the proposed topology.

Key words: Bridgeless PFC, Power-factor-correction (PFC), Soft switching; Zero-voltage-switching (ZVS)

NOMENCLATURE

$V_{C_r}(t)$	: Voltage across C_r.
$M_{C_r}(t)$	: Normalized voltage across capacitor C_r.
$I_{Lr}(t)$	: Current of L_r.
$J_{L_r}(t)$	: Normalized current of L_r.
J_{in}	: Normalized input current.
T_s	: Switching period.
f_S	: Switching frequency.
T_f	: Fall time.
I_{s_peak}	: Main switches peak current.
V_o	: Output Voltage.
V_{in}	: Input voltage.
C_r	: Represent 'C_{r1}' or 'C_{r2}'
L_r	: Represent 'L_{r1}' or 'L_{r2}'
K_r	: Normalized L current ripple d ($\Delta i_l / I_l$)
t_{rr}	: Rated reverse recovery time for Diodes

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I. INTRODUCTION

To overcome the challenges of the ever-increasing power densities of today's ac/dc power supplies, designers are continuously looking for opportunities to maximize efficiency, minimize the components count, and reduce the size of components. Conventional rectifiers encounter excessive peak input current and total harmonic distortion (THD) which reduce the power factor (PF) to about 0.5–0.7 [1]. Power factor correction (PFC) converters are employed to decrease these harmonics. A conventional type of PFC converter, which is usually controlled by the average current pulse width modulation (PWM) method, is a full-bridge rectifier followed by a boost converter, as shown in Fig. 1(a) [2]–[4]. However, it suffers from low efficiency and high stress on the main switch. Increasing the switching frequency reduces the volume and weight of the converter but, leads to higher switching losses. Therefore, using the soft-switching techniques is unavoidable for high switching frequency applications. Zero voltage switching (ZVS) and zero-current switching (ZCS) are soft-switching techniques which provide soft switching while retaining the desirable features of conventional PWM converters. ZVS techniques eliminate the turn-on capacitive losses. Thus MOSFETs are preferred for ZVS techniques [2]. The turn-off switching losses caused by tail currents, are a major part of the total switching losses in IGBTs. Therefore, in these converters, using ZCS techniques is more efficient than

ZVS techniques. In some PFC rectifiers, due to high input voltage variations (0 to peak value of the input ac voltage), ZVS may be realized in a restricted area in a utility line cycle. This limits the input ac voltage. Moreover, in conventional boost based PFC converters, conduction losses are higher when compared to diode rectifiers [7], [8]. To reduce conduction losses, the rectifier circuit and the PFC have been combined to introduce a bridgeless PFC converter, as shown in Fig. 1(b) [1], [6]. This combination decreases the conduction losses by reducing the number of semiconductor components in the line current path [9]-[13]. In bridgeless PFC, the body diode of S_2 conducts in the entire positive half line cycle and the body diode of S_1 conducts in the entire negative half line cycle. Using the ZVS technique for this converter can lead to even higher efficiencies. In this paper, a new ZVS PFC converter is proposed. The proposed converter consists of an auxiliary circuit which can provide the ZVS condition for the main switches if it is controlled properly. Conventional ZVS topologies reduce the turn-on switching losses, but the proposed topology reduces the overlap between the voltage and the current on the power switches both during switch turn-off and turn-on (section IV). Therefore, bridgeless PFC and the ZVS technique reduce conduction losses and switching losses, respectively. This maximizes the efficiency and consequently the limitation on switching frequency can be eliminated.

The converter operation and design procedure based on the steady-state are analyzed in the next section. The elimination of the turn-off switching losses is explained in Section IV. In section V the current control strategy is introduced. The design procedure is discussed in Section VI. The simulation and experimental results from a 250 W, 400 Vdc prototype converter at 100 kHz for universal input voltage (90-264 Vrms) applications are given in Section VII and VIII, respectively. These results verify the feasibility of the design process and the advantages of the proposed topology. The proposed converter is suitable for single-phase, power factor correction and universal input voltage applications where high efficiency and low EMI (Electro Magnetic Interference) are important.

II. The Novel Topology and Its Operation

Fig. 2 shows the proposed single-phase bridgeless ZVS-PFC converter. The denoted circuit in the dotted box is the proposed auxiliary circuit which provides soft switching for the main switches. C_{s1} and C_{s2} shown across S_1 and S_2 are the parasitic capacitance of the switches.

L_{r1} and L_{r2} provide soft switching for the main diodes (D_1, D_2) and reduce di/dt at turn-off times. To provide soft switching for the main power switches at turn-on, the auxiliary switch is turned on for a fixed period of time. This provides the soft switching condition for the main switches and reduces the overlap between the current and the voltage at switching times.

The bridgeless PFC operation is symmetrical in the two

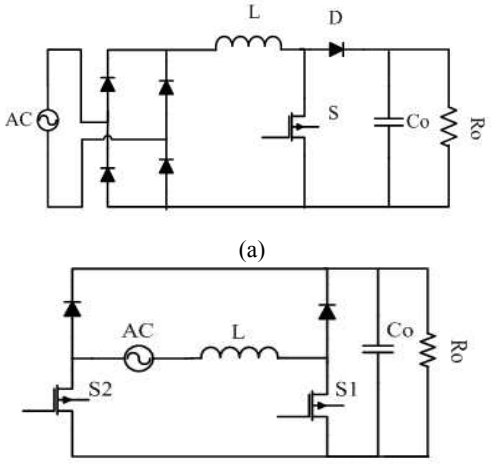


Fig. 1. (a) Conventional boost PFC converter. (b) Conventional bridgeless PFC converter.

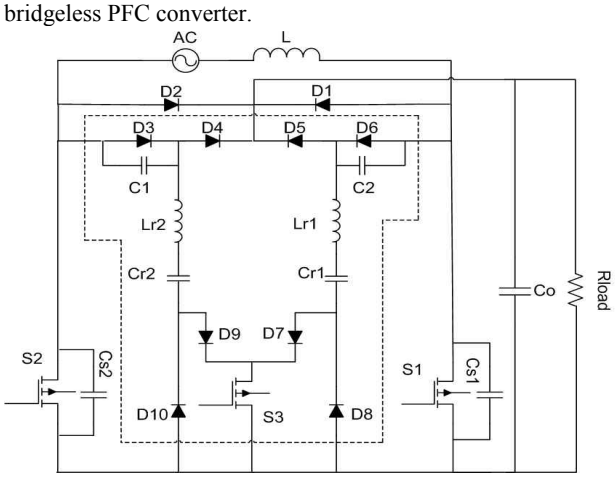


Fig. 2. Proposed ZVS bridgeless PFC converter topology

input line half-cycles. Therefore, one half-cycle of the converter operation is explained here. The auxiliary circuit is divided into two symmetric sections too. Due to the input line half-cycles, one section is inactive. Thus another section of the proposed auxiliary circuit provides the soft switching condition for the main switches. Thus both sections have no effect on the converter efficiency when they are in the inactive mode.

During the subinterval where the converter behaves like a PWM boost converter in the charging and transferring modes, all of the auxiliary components are inactive. Therefore, there is no additional loss in these states.

In order to explain the operation of the converter and to quantify its behavior, the following conditions are assumed:
All components are ideal; the converter operates in the steady state at a fixed switching frequency (f_s). The input voltage (V_{in}) is a sine wave that is assumed to be constant (V_g) in a switching cycle. The output voltage (V_o) is also constant, and the switching frequency is much higher than the ac line frequency. In addition, the input inductor (L) is large enough to be replaced by a current source (I_{in}) during the converter switching period (T_s).

The operation of the converter in a half cycle of the utility line voltage can be divided in 8 subintervals. The equivalent circuits at each subinterval and the theoretical waveforms have been illustrated in Fig. 3 and 4, respectively.

A. Subinterval 1 [t0-t1] [Fig. 3(a)]

This subinterval is considered just to show the initial condition of the switching operation. During this subinterval, D_2 (the boost diode) and the body diode of S_1 are conducting. The load current and the converter are behaving as a simple

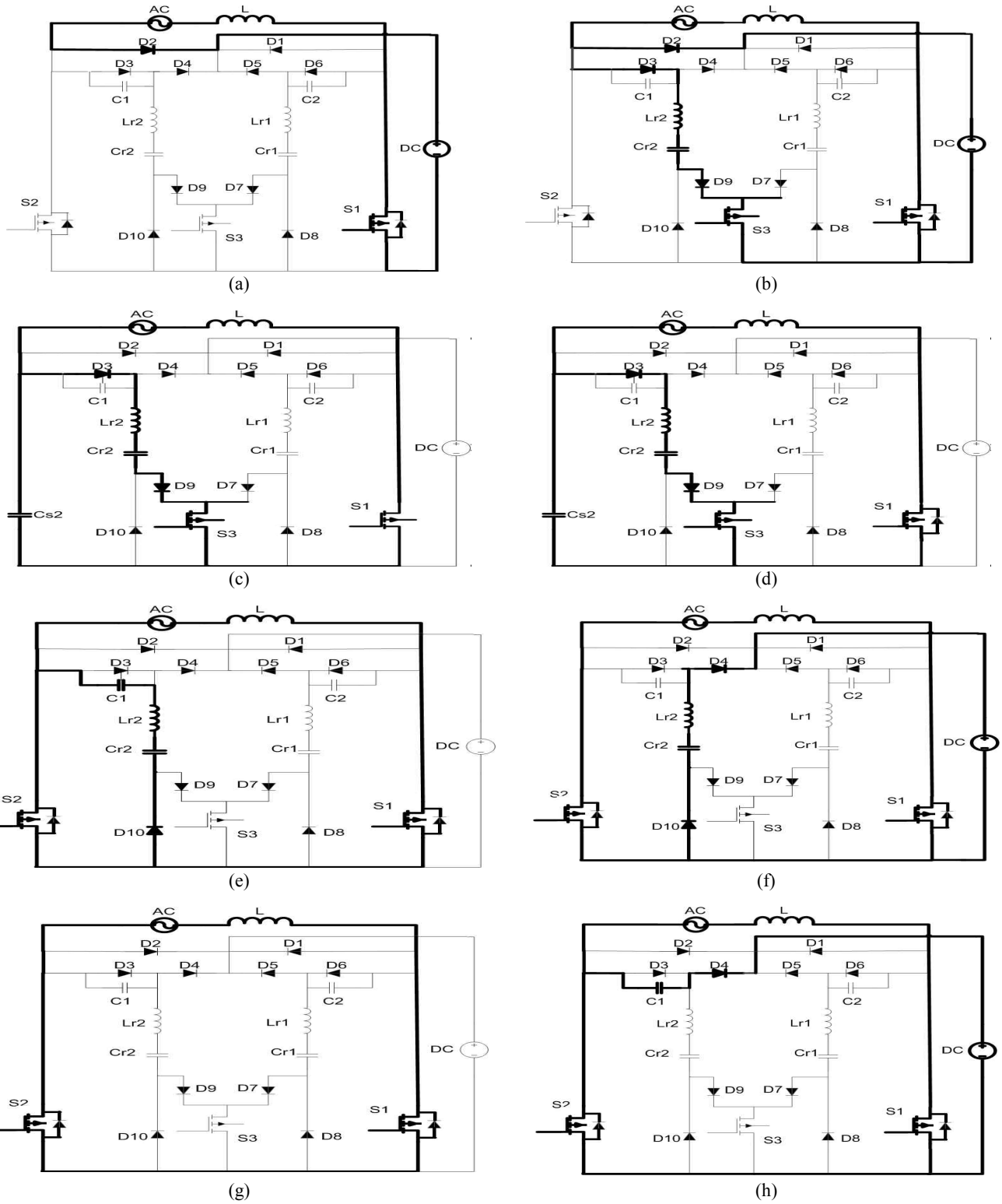


Fig. 3. The main current flow paths in the converter during a switching period (a) Subinterval 1. (b) Subinterval 2. (c) Subinterval 3. (d) Subinterval 4. (e) Subinterval 5. (f) Subinterval 6. (g) Subinterval 7. (h) Subinterval 8.

PWM boost converter where its switch is off and the diode is on. This subinterval is finished when the PFC controller turns on S_3 to start the resonance in the auxiliary circuit before turning the main switch (S_2) on.

B. Subinterval 2 [t_1-t_2] [Fig.3(b)]

This subinterval begins by turning S_3 on and ends when the current of D_2 reaches zero. Due to L_{r2} , this switch turns on with the zero current (ZC) condition. L_{r2} also slows down the turn-off di/dt through the boost diode D_2. The current slowly starts diverting from D_2 to the auxiliary resonant circuit (consisting of L_{r2} and C_{r2}). Therefore, D_2 is turned-off at the zero current at instant t_2. Consider the converter equivalent circuit, as shown in Fig.3 (b). The state plane trajectory is given in Fig. 5. Solving the state plane geometry, the following is obtained:

$$\alpha = \cos^{-1}\left(M - M_{Cr2}(t_2)/M - M_{Cr2}(t_1)\right) \quad (1)$$

where:

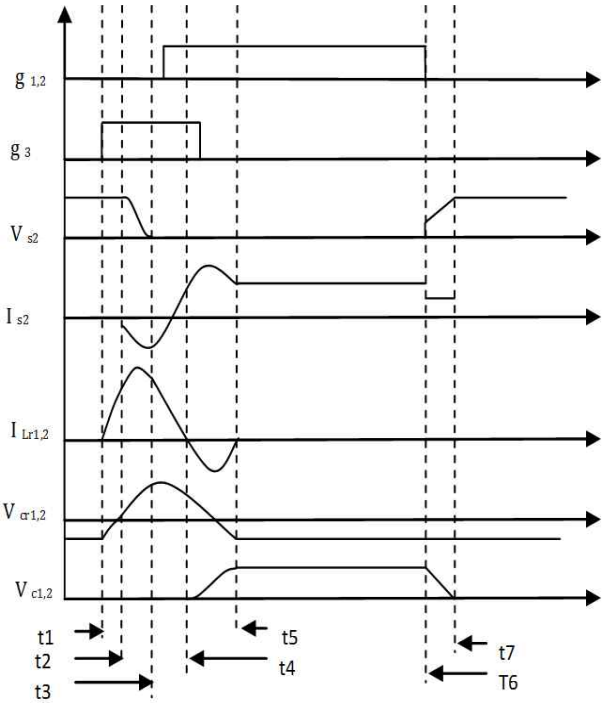


Fig. 4. Theoretical auxiliary circuit's waveforms during a switching period.

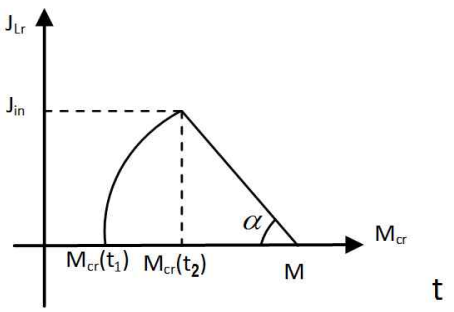


Fig. 5. State plane trajectory of subinterval 2.

$I_{Lr2}(t_1) = 0$, $M_{Cr2}(t_2) = M - J_{in}\cot g(\alpha)$, $t_2 = \alpha/\omega_2$, $V_{base} = V_g$, $R_2 = R_{base} = \sqrt{L_{r2}/C_{r2}}$, $\omega_2 = 1/\sqrt{L_{r2}C_{r2}}$

C. Subinterval 3 [t2-t3] [Fig. 3(c)]

This subinterval begins when the current through D_2 reaches zero and the current is passed through C_{s2}. In this subinterval S_3, D_3 and D_9 are conducting. The equivalent circuit is a third order, as shown in Fig.3(c). The converter equivalent circuit's response can be considered as a resonant response (ringing, illustrated in Fig.6(a)) and as a non-resonant response (integrating ramp, illustrated in Fig.6(b)). Some of the parameters used in Fig.6, are calculated as follows:

$$\Re = C_{s2}/C_{r2}\ , C_t = \left(C_{s2}C_{r2}\right)/\left(C_{s2}+C_{r2}\right) \quad (2)$$

$$I_t = I_{in}/(1+\Re)$$

$$V_{tot} = V_{Cr2} - V_{Cs2} \quad (3)$$

$$V_\Delta = V_{Cr2} + \Re \times V_{Cs2} \quad (4)$$

Where:

$$V_{Cs2} = -V_{tot}/(1+\Re) + V/(1+\Re)$$

$$V_{Cr2} = \left(\Re/(1+\Re)\right)\times V_{tot} + V_\Delta/(1+\Re)$$

$$R_3 = R_{base} = \sqrt{L_{r2}(C_{s2}+C_{r2})/C_{r2}C_{s2}}$$

$$\omega_3 = 1/\sqrt{L_{r2}.(C_{s2}C_{r2}/C_{s2}+C_{r2})}$$

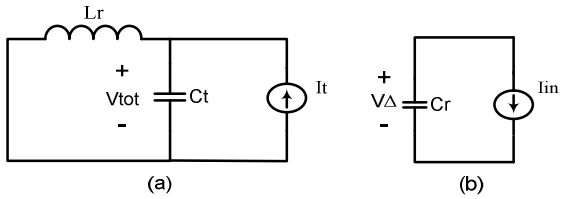
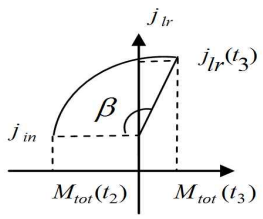
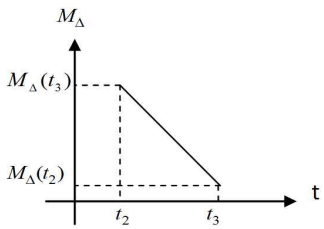


Fig. 6. Converter's simplified equivalent circuit in the 3rd Subinterval.(a) resonant part.(b) non-resonant part.



(a)



(b)

Fig 7. Converter's simplified equivalent circuit in the 3rd subinterval.(a) resonant part.(b) non-resonant part.

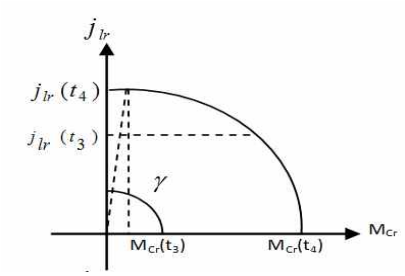


Fig. 8. State plane trajectory of Subinterval 4.

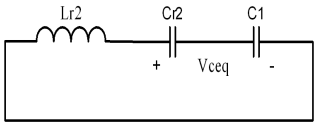


Fig. 9. Converter's equivalent circuit during Subinterval 5.

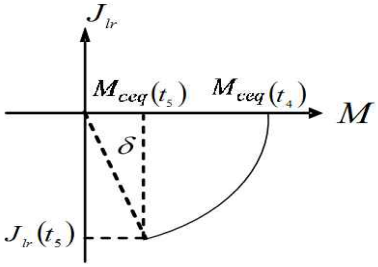


Fig. 10. State plane trajectory of Subinterval 5.

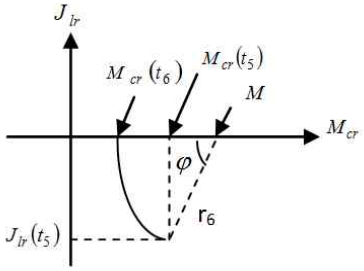


Fig. 11. State plane trajectory of Subinterval 6.

Subinterval 3 is finished when the C_{s2} voltage reaches zero, and the S_3 current is reversed.

The resonant part state plane trajectory and the non-resonant state plane trajectory are shown in Fig. 7(a) and 7(b), respectively.

Considering the equivalent circuits, shown in Fig.3(c), Fig. 6 and Fig. 7 the following can be written:

$$J_{Lr2}(t_3) = M_{tot}(t_2) \times \sin(\pi - \beta) + J_{in} \tag{5}$$

$\beta = \omega_3 t_3$

$$M_{Cs2}(t_3) = -(1/1+\Re) \times (M_{tot}(t_2) \times \cos(\pi - \beta)) + (1/1+\Re) \times (M_{\Delta}(t_2) - J_{in} \times \beta) = 0 \tag{6}$$

$$M_{Cr2}(t_3) = (\Re/1+\Re) \times (M_{tot}(t_2) \times \cos(\pi - \beta)) + (1/1+\Re) \times (M_{\Delta}(t_2) - J_{in} \times \beta \tag{7}$$

At the end of this subinterval the current through the resonant inductor L_{r2} is 0, and voltage across the resonant capacitor C_{r2} is Vc_{r2} (t_3). Based on the aforementioned equation, soft switching can be achieved when the following inequality is satisfied:

$$J_{lr2}(t_3) > J_{in} \tag{8}$$

D. Subinterval 4 [t3-t4] [Fig.3(d)]

During this subinterval, S_3, D_3, D_9 and the body diode of S_2 are conducting. The current of L_{r2} decreases linearly until it reaches I_{in} and the main switch S_2 is just about to start conduction. This is the ZVS subinterval where S_2 must be turned on. The current in the auxiliary circuit decreases below the input current through L and the difference between the two currents starts flowing through switch S_2. This subinterval lasts till t_4 at which time the auxiliary circuit current becomes zero. The state plane trajectory is given in Fig.8.

From Fig.3(d) and Fig.8 the following expressions are derived:

$$M_{Cr2}(t_4) = J_{Lr2}(t_3)/\sin\gamma \tag{9}$$

where:

$\tan\gamma = J_{Lr2}(t_2)/M_{Cr2}(t_2)$, $\omega_4 = 1/\sqrt{L_{r2}C_{r2}}$

$\gamma = \omega_4 t_4$, $R_4 = R_{base} = \sqrt{L_{r2}/C_{r2}}$

E. Subinterval 5 [t4-t5] [Fig.3(e)]

During this subinterval, S_2 and D_{10} are on and the auxiliary circuit current reverses. Diode D_9 prevents this current from flowing through S_3 and so the current is passed through D_{10}. This provides a ZVS turn-off condition for S_3. The auxiliary switch S_3 should be turned-off during this subinterval. At the same time, diode D_3 diverts this current through capacitor C_1 and charges it. Depending upon the amount of resonant current, this capacitor is charged to a voltage level equal to or lower than the output voltage. The equivalent circuit is shown in Fig.9. The state plane trajectory is given in Fig.10, where:

$$V_{ceq} = V_{c_{r2}} + V_{C1} \tag{10}$$

From Figs.9 and 10 the following can be written:

$$J_{Lr2}(t_5) = M_{ceq}(t_4)\sin\delta \tag{11}$$

$$M_{Ceq}(t_5) = M_{C1}(t_4)\cos\delta \tag{12}$$

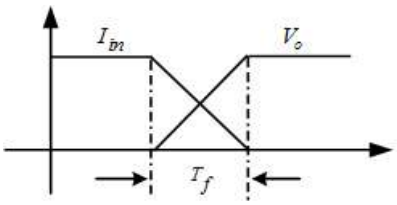
$$M_{c1}(t_5) = M_{Ceq}(t_5) - M_{Cr2}(t_4) \tag{13}$$

$\delta = \omega_5 t_5$, $\omega_5 = \sqrt{1/L_r C_{eq}}$, $C_{eq} = (C_1 C_{r2}/C_1 + C_{r2})$

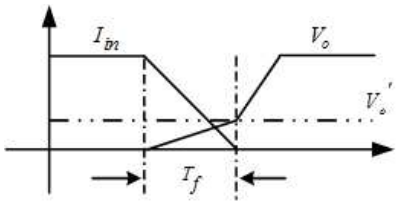
F. Subinterval 6[t5-t6] [Fig.3(f)]

During this subinterval D4, D10 and S2 are conducting. This subinterval ends at t_6 when the auxiliary circuit current reduces to zero. D4 and D10 are turned off at the ZC condition. The state plane trajectory is given in Fig.11. By solving the state plane geometry, the following is obtained:

$$(r_6)^2 = (J_{Lr2}(t_5))^2 + (M - M_{Cr2}(t_5))^2 \tag{14}$$



(a)



(b)

Fig. 12. Power MOSFET's current and voltage waveforms during the turned-off time (a) conventional converter, (b) proposed converter.

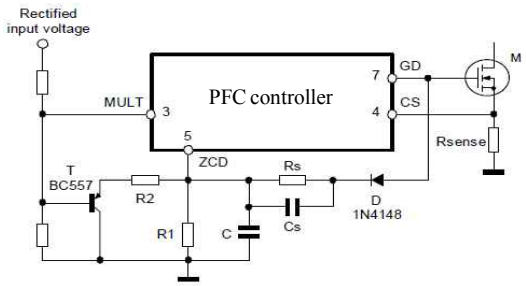


Fig. 13. Schematic of the employed Line-modulated Fixed-Off-Time PFC converter controller [17].

$J_{Lr2}(t_5) = r_6 \times \sin\varphi$, $M - r_6 = M_{Cr2}(t_6)$, $\varphi = \omega_6 t_6$, $\omega_6 = \sqrt{1/L_{r2}C_{r2}}$

If C_1 is charged to a value that is less than the output voltage, then D3 will not conduct. Later on, it will be clear that in such a case a reduced voltage will appear across S2 at the turn-off time instead of a zero voltage. D3 turns on if the following equation is satisfied:

$$M_{C1}(t_6) = M \tag{15}$$

G. Subinterval 7[t6-t7] [Fig.3(g)]

In this subinterval S_2 is conducting. The converter behaves like a PWM boost converter in the charging state and the auxiliary circuit is inactive. This subinterval ends when the main switch is turned-off.

H. Subinterval 8[t7-t8] [Fig.3(h)]

In this subinterval switch S_2 is turned off at the ZVS conditions, and capacitor C_{s2} is charged until the voltage across it is equal to the output voltage. The capacitor C_1 causes the voltage across S_2 to rise slowly because the net voltage appearing across S_2 is the difference between the output voltage V_O and the voltage across C_1. After t_8, the converter is in the same condition as in subinterval 1, and another switching cycle will be started.

III. Reducing the Turn-Off Off Switching Losses

As mentioned before, the ZVS techniques eliminates the turn-on switching losses. Fig.12(a) shows the current and voltage waveforms of a MOSFET during its turn–off time. Its turn-off switching losses can be estimated from Fig.12 (a) as follows:

$$p_{loss} = \frac{1}{2}.V_o.I_{S_1-peak}.F_{sw}.(T_f) \tag{16}$$

During subinterval 8, when MOSFET S_2 is turned off, its drain-source voltage increases very slowly until the stored energy in capacitor C_1 is totally transferred to the output load. Therefore, when the current of the switch decreases to zero the drain-source voltage is much less than V_O. This can significantly reduce the turn-off switching losses. The current and the voltage of S2 in the proposed converter have been shown in Fig.12 (b).

In order to obtain good performance, the value of the capacitor C_1 must satisfy (14).

In the proposed converter, the turn-on switching losses are approximately zero and the turn-off switching losses are reduced significantly. Although the proposed converter has 15 extra components, it reduces both the turn-off and the turn-on losses. Because of all of the auxiliary components operate for a tiny amount of time relative to the switching period time, they are low cost components. Moreover, bridgeless PFC is used which reduces the conduction losses and highest efficiency can be achieved.

IV. Current Control Strategy

Nowadays, the line-modulated Fixed-Off-Time approach is widely used as a current control method in PFC converters. A simplified scheme of the employed PFC controller is shown in Fig. 13 [17]. This circuit makes T_{OFF} as a function of the instantaneous input line ac voltage [16]-[18]. As mentioned before, the proposed converter utilizes two signals to drive the main switches. Therefore, from the main switch gate signal and some logic IC (Monostable and an AND gate) the auxiliary circuit switch gate signal is generated. Any kind of conventional PFC controller can be used with the proposed converter. The simplified extra circuit and the control process are shown in Fig.14.

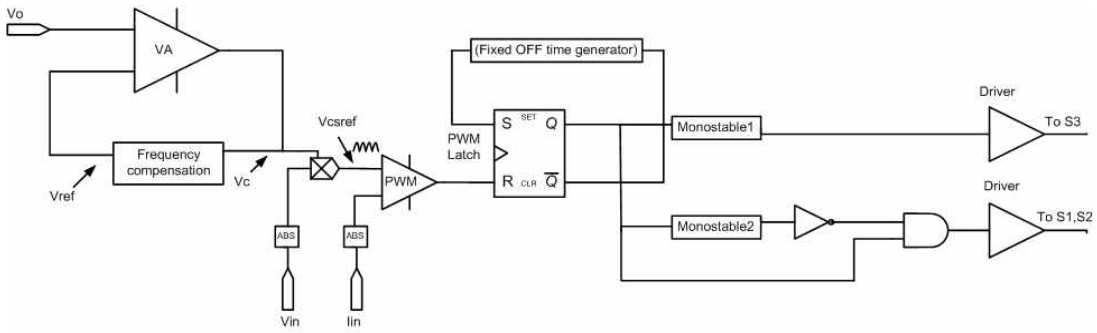
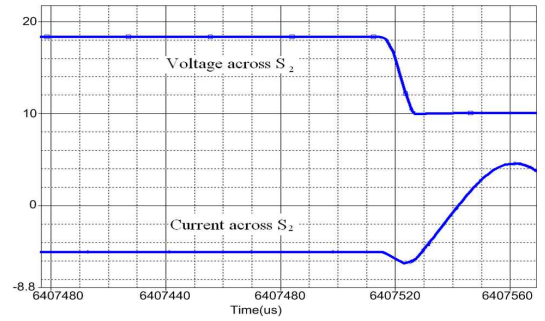
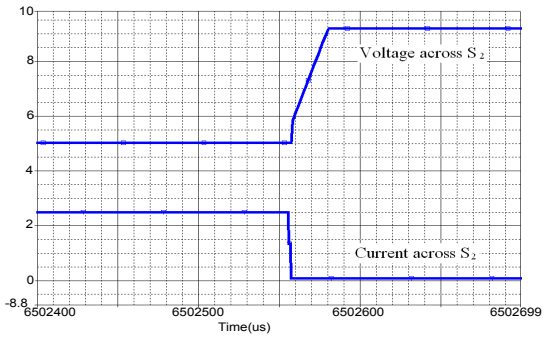


Fig. 14. Auxiliary control circuits block diagram and controller.



(a)



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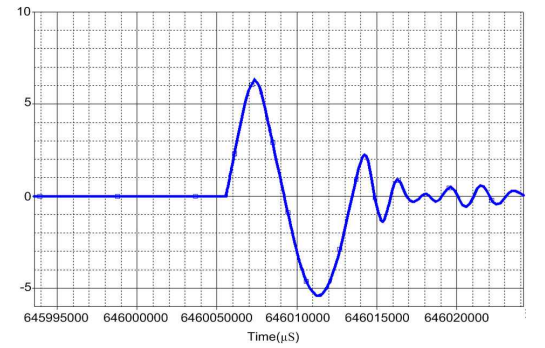


(c)

Fig. 15. Simulation results. a) Voltage and current across main switches S2 (S1 in active mode is short circuit) at turn-on time. b) Voltage and current across main switches S1, S2 at turn-off time. c) Current through Lr.(V: 100 V/div, I: 1 A/div, and Time: 5 ms/div).

V. DESIGN PROCEDURE AND EXAMPLE

The design procedure and an example of the proposed ZVS-PWM bridgeless PFC are described as follows. The specifications of the prototype converter have been tabulated in Table I. The design procedure to obtain the optimum value for L in Fig.2 is expressed as follows:

The K range can be obtained from:

$$K_{\min} = \sqrt{2} \times \left(\frac{V_{in(RMS)\min}}{V_{OUT}} \right) = 95\sqrt{2} / 400 = 0.335 \tag{17}$$

$$K_{\max} = \sqrt{2} \times \left(\frac{V_{in(RMS)\min}}{V_{OUT}} \right) = 265\sqrt{2} / 400 = 0.937 \tag{18}$$

The maximum L current and L can be estimated from:

$$T_{OFF} = \frac{K_{\min}}{f_{sw\max}} = 3.35\mu s \tag{19}$$

$$\Gamma = \frac{P_{in0}}{K_{\min} V_{out}} \frac{4\pi K_r}{2\pi - K_r(4 + \pi K_{\min})} = 1.54 \tag{20}$$

$$L = \frac{V_{OUT}}{\Gamma} T_{OFF} = \frac{400}{1.54} * 3.35 * 10^{-6} = 870\mu H \tag{21}$$

$$I_{Lpk\max} = \frac{P_{in0}}{K_{\min} V_{out}} \frac{4\pi(1 - K_r K_{\min})}{2\pi - K_r(4 + \pi K_{\min})} = \Gamma \frac{1 - K_r K_{\min}}{K_r} = 4 \frac{1 - 0.2 * 0.335}{0.2} = 2.86A \tag{22}$$

A. Calculation of the Resonant Inductor L_t:

The resonant inductor L_r has to be large enough to limit the boost rectifier's di/dt value, during the turn-off time, so that it is less than 100 A/s and not too large. Because, the resonant period T_r will also be too large, this leads to larger conduction losses in the auxiliary circuit. Therefore, L_r must be chosen such that the boost diode D_1 turns-off when it is at least three times its rated reverse recovery time, as mentioned in [1].

Assuming the rated reverse recovery time of the selected boost diode is equal to 30ns, the value of Lr is obtained as follows:

TABLE I
SPECIFICATIONS OF THE PROTOTYPE DESIGNED PFC CONVERTER

Output power	250 W
Output voltage V_o	400 Vdc
Input voltage V_{in}	90-265 Vac
Switching frequency	100 kHz

TABLE II
PART LIST OF THE IMPLEMENTED PROTOTYPE POWER CIRCUIT

Part	Type
S_1,S_2,S_3	IRF840
D_1 , D_2	HFA08TB60
D_3 , D_4 , D_5 , D_6 , D_7 , D_8	MUR1540

TABLE III
COMPARISON OF LOSSES IN HARD SWITCHESD BOOST TOPOLOGY AND PROPOSED TOPOLOGY

Type of losses	Hard switched	Proposed topology
Main switchs	12.32 W	5 W
auxiliary switch	-	1.1 W
All diodes	3.63 W	1.9 W
Lboost	5.5w	5.5W
Resonant Inductor Lt	-	0.9 W
Efficiency	92%	94.6%

$$L_r = \left(3.t_{rr}.V_{pk}/I_{C1}\right) = 3.30ns \times 280/3.93 = 6.4\mu H \quad (23)$$

where V_{pk} is the peak voltage across L_r, according to:

$$V_{pk} = V_o - V_{C1(\min)} \quad (24)$$

B. Calculation of the Resonant Capacitors Cr and C1,2:

It can be concluded that $C_r/C_{1,2}$ should be chosen to be greater than 1 to reduce both the peak voltage stress across S_1 and the auxiliary circuit rms current. Although this gives a smaller value for the ZVS turn-on subinterval, an adequate subinterval may still be obtained by choosing $C_r/C_{1,2}$=3. Soft switching can be achieved when the following equations are satisfied:

$$R_r = 0.21*\left(V_o/I_{in}\right) = 0.21*\left(400/3.722\right) = 22.57 \quad (25)$$

$$I_{in} = I_{in\_pk} - I_{rpp}/2 = 3.72 \quad (26)$$

$$C_r = L_r/(R_r)^2 = 6\mu H/509.33 = 12nF \quad (27)$$

$$C_r/C_{1,2} = 3 \Rightarrow C_1 = 4nF \quad (28)$$

VI. SIMULATION RESULTS

To verify the feasibility of the proposed topology, a prototype converter at 100 kHz, has been designed and simulated by PSPICE. The employed components have been tabulated in Table II. The voltage across S_2 and current through it at the turn-on and turn-off times are shown in Fig. 15. The

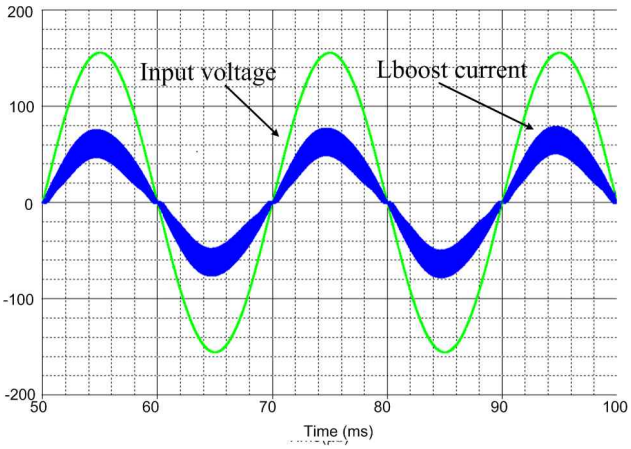


Fig. 16. Converter's input voltage (Vin) and input current (Iin) waveforms.

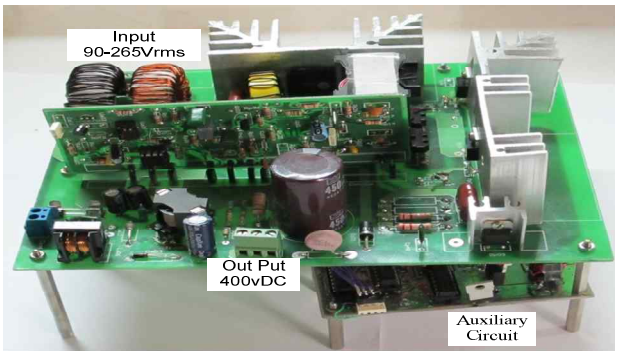


Fig. 17. Prototype of the designed PFC Converter.

waveforms of the input voltage and current of the ZVS-PWM bridgeless rectifier at the rated 250 W are shown in Fig. 16. It can be seen that the main switches (S_1, S_2) turn on with ZVS and turn off at a reduced voltage. Table III gives a comparison of the losses in the conventional hard-switching PWM boost rectifiers and in the proposed ZVS-Bridgeless boost converter. Both converters operate at nominal input voltage (110 Vac) and nominal output power. For the conventional PWM boost rectifier, it can be concluded that the major power dissipations are due to the switching losses.

VII. EXPERIMENTAL RESULTS

A prototype of the designed and simulated converter in the previous section has been implemented to verify the simulation results and the theoretical analysis. Fig. 17 shows a photograph of the new single-phase ZVS-PWM bridgeless PFC converter. To compare the efficiency, a conventional boost PFC converter with hard switching, a ZVS boost converters using the same auxiliary circuit, a hard switching bridgeless converter and finally the proposed circuit were studies using simple modifications in the same circuit (Fig.18).

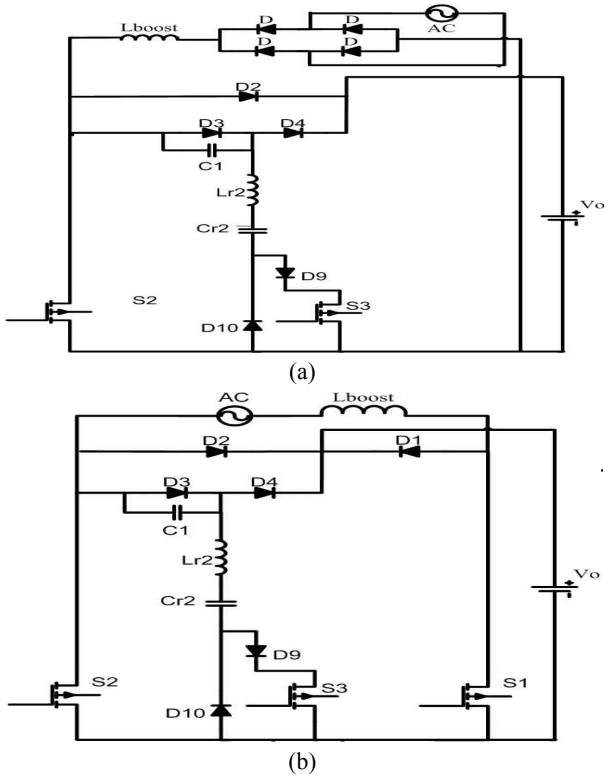


Fig. 18 . (a) Conventional boost PFC with ZVS in main switch (b) Proposed ZVS bridgeless PFC circuit with one switch in ZVS.

To clear the effect of the auxiliary circuit on the main switches, at first, it has been implemented for one switch, as shown in Fig. 18(b). Fig. 19 shows the waveforms of the voltage across the main switch S2 and the current through it at the turn-on and turn-off times. It is important to adjust the gate drive signals of the main and auxiliary switches exactly. Fig.19(c) shows the gate drive signal of the main and auxiliary switches. The waveforms of the input voltage and current and the input line current harmonics of the ZVS-PWM bridgeless rectifier at the rated 250 W are shown in Fig. 20.

Based on these waveforms, the current is practically sinusoidal with a low total harmonic distortion (THD) and a high power factor. It can be seen that the experimental results, shown in Fig. 20, are in good agreement with the theoretical analysis and the simulated results which have been illustrated in Fig. 15. Fig. 21 shows the measured efficiencies of the different converters such as the proposed ZVS bridgeless PFC circuit (Fig.2), the ZVS bridgeless PFC circuit with one switch in ZVS (Fig.18 (b)), the conventional boost ZVS converter (Fig.18 (a)), and the hard-switching conventional boost converter.

Depending on the operating conditions, using the proposed converter can improve the efficiency in the range of 3% to 4.7%.

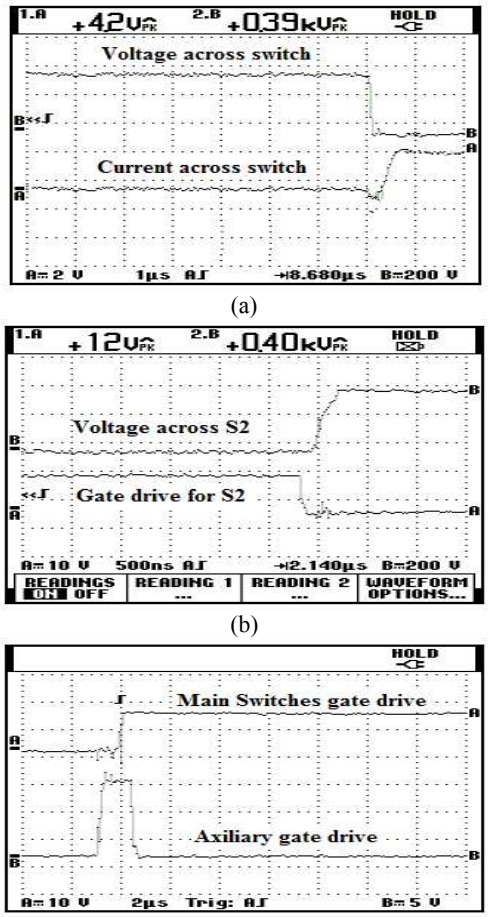
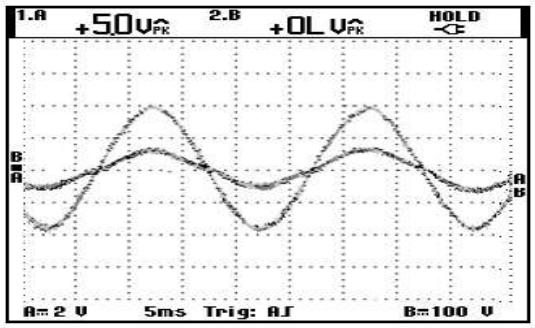


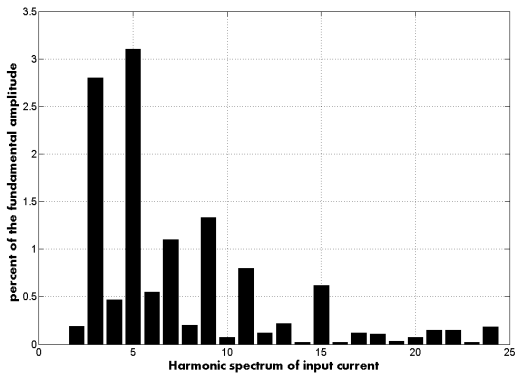
Fig. 19. Experimental results at V = 400 V, P = 250 W: (a) main switch S2 at turn-on, (V: 200 V/div, I: 3 A/div, and Time: 1us/div) (b) main switch S_2 at turn-off. (V: 200 V/div, and Time: 500 ns/div), (c) main and auxiliary gate drive signal.

VIII. CONCLUSIONS

In this paper, a new ZVS-PWM boost rectifier is presented and realized. Realizing soft switching for all of the stresses is the main advantage of the introduced topology. This converter has a higher efficiency when compared to its conventional PWM hard-switching counterpart, due to the soft switching and the lower conduction losses in the power flow path during rectification. This converter realizes soft switching for both the turn-off and turn on times. The overlap between current and voltage reduces through the main switches during the fall time. Based on the converter analysis, characteristic curves have been obtained and a step-by-step design procedure for the converter has been introduced. Experimental results with a 250 W prototype at 100 kHz, verify the feasibility and advantages of the introduced topology. Based on the given approach, the converter prototype has been designed, and simulation and experimental results have been presented. An efficiency of 94.7% is achieved which improves the efficiency more than 4.7%, when compared to the hard-switching converter.



(a)



(b)

Fig. 20. (a) Converter's input line voltage and current waveforms (V: 100 V/div, I: 6 A/div, and Time: 5 ms/div). (b) Input current harmonics.

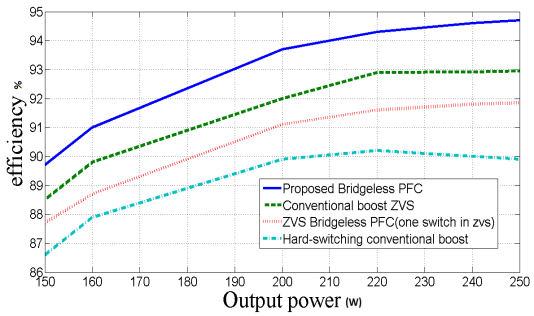


Fig. 21. Experimental efficiencies of the proposed ZVS-PWM Bridgeless PFC and the conventional boost rectifier in 95Vac input voltage.

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