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Embedded Switched-Inductor Z-Source Inverters

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Abstract

In this paper, a ripple input current embedded switched-inductor Z-source inverter (rESL-ZSI) and a continuous input current embedded switched-inductor Z-source inverter (cESL-ZSI) are proposed by inserting two dc sources into the switched-inductor cells. The proposed inverters provide a high boost voltage inversion ability, a lower voltage stress across the active switching devices, a continuous input current and a reduced voltage stress on the capacitors. In addition, they can suppress the startup inrush current, which otherwise might destroy the devices. This paper presents the operating principles, analysis, and simulation results, and compares them to the conventional switched-inductor Z-source inverter. In order to verify the performance of the proposed converters, a laboratory prototype was constructed with 60 V_{dc} input to test both configurations.

Key words: Z-source inverter, embedded Z-source inverter, switched-inductor, boost inversion ability, continuous current

I. INTRODUCTION

High-performance voltage-source inverters [1] are widely used in various applications such as uninterruptible power supplies, distributed power systems, ac motor drives, and hybrid electric vehicles. However, the traditional voltage-source inverter has a couple of major problems: 1) it cannot have an ac output voltage higher than the dc source voltage and can only provide buck dc-ac power conversion; 2) shoot through, generated by both power switches in a leg, is forbidden. For applications where a low input voltage is inverted to a high ac output voltage, an additional dc-dc boost converter is needed to obtain a desired ac output. The additional power converter performs two-stage power conversion with high cost and low efficiency. Unlike traditional voltage-source inverters [1], Z-source inverters were proposed in [2] in order to accomplish single-stage power conversion with buck-boost abilities. In the Z-source inverter, both of the power switches in a leg can be turned on at the same time and thereby eliminate the dead time. This significantly improves the reliability and reduces the output waveform distortion. Various Z-source inverter topologies have been reported in many different studies. Work on Z-source inverters has focused on pulse-width modulation (PWM) strategies [3], [4], applications [5], [6], modeling and control [7], [8], direct ac-ac converters [9], [10], and other Z-network topologies [11]-[13]. A class of quasi-Z-source inverters was proposed in [11], [12] that were designed to overcome the shortcomings of the classic Z-source inverter. Quasi-Z-source inverters have some advantages, such as a reduction in the passive component ratings and an improvement in the input profiles.

Some papers have recently focused on improving the boost factor of the Z-source inverter by using a very high modulation index in order to achieve an improvement in the output waveform [14]-[17]. For instance, studies in [14]-[16] add inductors, capacitors, and diodes to the Z-impendence network in order to produce a high dc link voltage for the main power circuit from a very low input dc voltage. In [17], two inductors in the impedance Z-network are replaced by a transformer with a turn ratio of 2:1 in order to obtain a high voltage gain. These topologies suit solar cell and fuel cell applications, since they require a high voltage gain in order to match the source voltage to the line voltage. Applying switched-capacitor, switched-inductor, hybrid switched-capacitor/switched-inductor structures, voltage-lift techniques, and voltage multiplier cells [18] to the dc-dc

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conversion process provides a high boost in cascade and transformerless structures with a high efficiency and high power density. A successful combination of the Z-source inverter and switched-inductor structure, called the switched-inductor Z-source inverter (SL-ZSI) [14], provides a strong step-up inversion that overcomes the boost limitations of the classic Z-source inverter (ZSI) [2].

The embedded Z-source inverter developed in [19] is built by inserting dc sources into the X-shaped impedance network. Because the dc sources connect directly to the impedance network inductors, the dc input current in the embedded Z-source inverter flows smoothly, compared to that found in a traditional Z-source inverter [2]. The embedded Z-source inverter assumes two sources can produce the same voltage gain as found in a traditional Z-source inverter. The embedded Z-source inverter provides a continuous input current without adding an input passive filter and also a lower voltage on the capacitors.

This paper applies the switched-inductor structure to the embedded-Z-source topology in order to create two new types of inverters, a ripple input current embedded switched-inductor Z-source inverter (rESL-ZSI) and a continuous input current embedded switched-inductor Z-source inverter (cESL-ZSI). The proposed inverters have a high boost voltage inversion ability and a continuous input current. Compared to the SL-ZSI, the proposed rESL-ZSI and cESL-ZSI reduce the voltage stress on the capacitors and improve the reliability. In addition, the proposed inverters avoid the startup inrush current that could destroy the devices. The operating principles, analysis, and simulation results are compared to the switched-inductor Z-source inverter. A laboratory prototype based on a TMS320F2812 digital signal processor (DSP) verifies both of the converter configurations. We also performed a participative simulation integral manufacturing (PSIM) simulation.

II. TRADITIONAL Z-SOURCE INVERTER TOPOLOGIES

Fig. 1(a) shows the original ZSI topology [2] in which the two-port impedance network couples the main inverter circuit to the dc voltage source. It consists of two inductors (L_1 and L_2) and two capacitors (C_1 and C_2) connected in an X configuration. An additional shoot-through zero state is added to the switching states in order to boost the voltage. When the input voltage is large enough to produce the desired ac voltage, the shoot-through zero state is not used and the Z-source inverter operates as a buck inverter—just like a conventional voltage-source inverter. In the original ZSI, the current drawn from the source is discontinuous. This is a limitation in some applications, and a decoupling capacitor bank at the front end is sometimes used to avoid the current discontinuity and protect the energy source.

The embedded Z-source inverter developed in [19] is

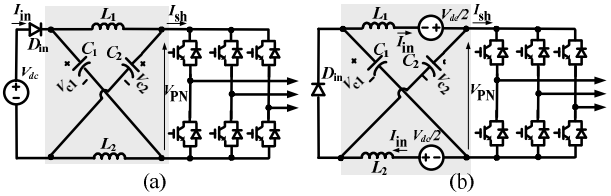


Fig. 1. (a) Original Z-source inverter and (b) embedded Z-source inverter with a continuous input current.

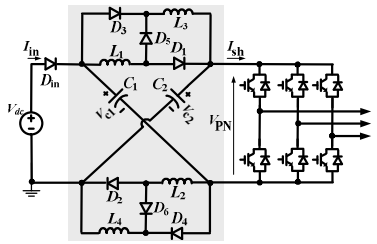


Fig. 2. Switched-inductor Z-source inverter (SL-ZSI) with a discontinuous input current.

designed to insert dc sources into the X-shaped impedance network. Fig. 1(b) shows a continuous input current embedded Z-source inverter with two isolated dc sources. Because the dc sources are directly connected to the impedance network inductors, the dc input current in the embedded Z-source inverter flows smoothly compared to the classic Z-source inverter [2]. The embedded Z-source inverter assumes that the two sources can produce the same voltage gain as the traditional Z-source inverter. The ratio between the dc-link voltage across the inverter bridge V_{PN} and the input dc voltage V_{dc}, called the boost factor in the classical ZSI and embedded ZSI, is expressed by:

$$B_z = \frac{V_{PN}}{V_{dc}} = \frac{1}{1-2T_0/T} = \frac{1}{1-2D}. \quad (1)$$

where T_0 is the interval of the shoot-through state during switching period T and $D = T_0/T$ is the duty cycle of each cycle.

In order to improve the main circuit output power quality, the switched-inductor Z-source inverter (SL-ZSI) [14] possesses high voltage-conversion ratios with a very short shoot-through state. Fig. 2 shows the SL-ZSI topology. It consists of four inductors (L_1, L_2, L_3 and L_4), two capacitors (C_1 and C_2), and seven diodes (D_{in}, D_1, D_2, D_3, D_4, D_5 and D_6). The combinations of L_1-L_3-D_1-D_3-D_5 and L_2-L_4-D_2-D_4-D_6 act as the switched-inductor cells. The boost factor of this inverter [14] is increased to:

$$B_s = \frac{1+T_0/T}{1-3T_0/T} = \frac{1+D}{1-3D}. \quad (2)$$

Despite this increase in boost inversion, the SL-ZSI has a significant drawback in that the current drawn from the source is discontinuous. This is a limitation in some applications, and a decoupling capacitor bank at the front end is sometimes used to avoid the current discontinuity and protect the energy source. In addition, the SL-ZSI cannot suppress the startup inrush current; the resulting voltage and

current spike can destroy the device.

III. EMBEDDED SWITCHED-INDUCTOR Z-SOURCE INVERTERS

Fig. 3 shows the two proposed embedded switched-inductor Z-source inverters, each having two isolated dc sources in which the components used are the same as those shown in Fig.2. The difference between the proposed topologies and the SL-ZSI topology is in the positions of the dc sources. In Fig. 3(a), each isolated dc source is directly connected to the switched-inductor cell (L_1-L_3-D_1-D_3-D_5 or L_2-L_4-D_2-D_4-D_6). Therefore, a ripple appears on the input current of this topology, denoted as a ripple input current embedded switched-inductor Z-source inverter (rESL-ZSI). Conversely, the dc sources in Fig. 3(b) are placed in series with inductors (L_2 and L_3) which results in a continuous input current. The topology shown in Fig. 3(b) is called a continuous input current embedded switched-inductor Z-source inverter (cESL-ZSI). Because the sources in the ESL-ZSI are connected to either an inductor or a switched-inductor cell, the proposed inverters have a flatter input current in comparison to the classic SL-ZSI [14]. The advantages of the proposed inverters are described as follows: 1) the input current is continuous; 2) it provides inrush current suppression at startup, unlike the traditional SL-ZSI in Fig. 2, because no current flows to the main circuit at startup; 3) the capacitor stress voltage is reduced; 4) high boost factor can be obtained by using a small shoot-through duty cycle; and 5) two separate dc sources can be applied.

Like the original Z-source inverter, the proposed inverters have extra shoot-through zero states in addition to the traditional six active and two zero states. Therefore, the operating principles of the proposed inverters are similar to those of the original Z-source inverters and the switched-inductor Z-source inverter. For the purpose of analysis, the operating states are simplified into shoot-through and non-shoot-through states. Figs. 4 and 5 show the rESL-ZSI and the cESL-ZSI equivalent circuits, respectively. In the non-shoot-through states, as shown in Figs. 4(a) and 5(a), the proposed inverter has six active states and two zero states in the inverter main circuit. During the non-shoot-through state, D_{in}, D_5 and D_6 are on, whereas D_1, D_2, D_3 and D_4 are off. L_1 and L_3 are connected in series; L_2 and L_4 are connected in series. Capacitors C_1 and C_2 are charged, whereas the inductors L_1, L_2, L_3, and L_4 transfer energy from the dc voltage sources to the main circuit. The corresponding voltages across L_1, L_2, L_3 and L_4 in this state are V_{L1_non}, V_{L2_non}, V_{L3_non} and V_{L4_non}, respectively.

In the shoot-through states, as shown in Figs. 4(b) and 5(b), the inverter side is shorted by both the upper and lower switching devices in the phase legs. During the shoot-through state, D_{in}, D_5 and D_6 are off, whereas D_1, D_2, D_3 and D_4 are on. L_1 and L_3 are connected in parallel; L_2 and L_4 are connected in parallel. Capacitors C_1 and C_2 are discharged, whereas inductors L_1, L_2, L_3 and L_4 store energy.

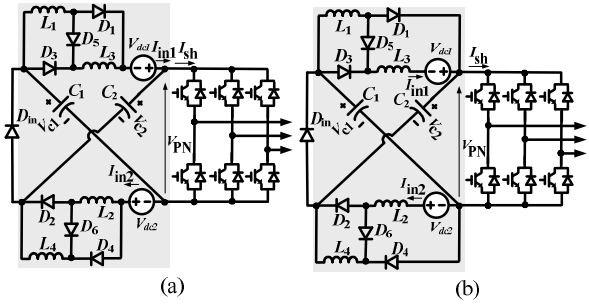


Fig. 3. Embedded switched-inductor Z-source inverters: (a) ripple input current topology (rESL-ZSI) and (b) continuous input current (cESL-ZSI) topology.

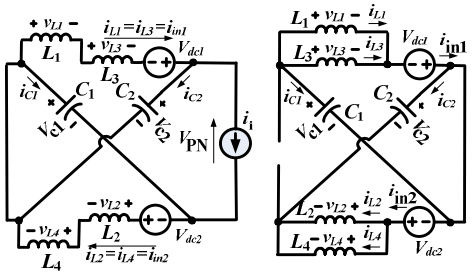


Fig. 4. Operating states of the rESL-ZSI: (a) non-shoot-through and (b) shoot-through.

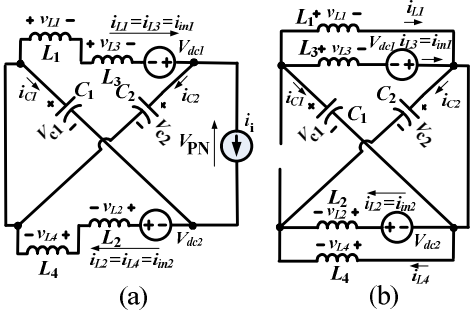


Fig. 5. Operating states of the cESL-ZSI: (a) non-shoot-through and (b) shoot-through.

A. rESL-ZSI Circuit Analysis

In the non-shoot-through state, as shown in Fig. 4(a), we get:

$$v_{L1} + v_{L3} = V_{dc1} - V_{C2} \quad (3)$$

$$v_{L2} + v_{L4} = V_{dc2} - V_{C1} \quad (4)$$

$$V_{PN} = V_{C1} + V_{C2} \quad (5)$$

$$i_{C1} = I_{L2} - i_i \quad i_{C2} = I_{L1} - i_i \quad i_{in1} = I_{L1} \quad i_{in2} = I_{L2}. \quad (6)$$

In the shoot-through state, as shown in Fig. 4(b), we obtain:

$$v_{L1} = v_{L3} = V_{C1} + V_{dc1} \quad (7)$$

$$v_{L2} = v_{L4} = V_{C2} + V_{dc2} \quad (8)$$

$$i_{C1} = -2I_{L1} \quad i_{C2} = -2I_{L2} \quad i_{in1} = 2I_{L1} \quad i_{in2} = 2I_{L1}. \quad (9)$$

Applying the volt-second balance principle to the inductors and capacitors, from (6)-(9) we obtain:

$$\begin{cases} V_{L1\_non} = V_{L3\_non} = \dfrac{-D}{1-D}(V_{dc1} + V_{C1}) \\ V_{L2\_non} = V_{L4\_non} = \dfrac{-D}{1-D}(V_{dc2} + V_{C2}) \\ I_L = I_{L1} = I_{L2} = I_{L3} = I_{L4} = \dfrac{1-D}{1-3D} i_i \\ I_{in} = I_{in1} = I_{in2} = (1+D) I_L. \end{cases} \quad (10)$$

Substituting (10) to (3) and (4), we get:

$$\begin{cases} (1+D)V_{dc1} + 2DV_{C1} - (1-D)V_{C2} = 0 \\ (1+D)V_{dc2} - (1-D)V_{C1} + 2DV_{C2} = 0. \end{cases} \quad (11)$$

Solving (11), we obtain:

$$\begin{cases} V_{C1} = \dfrac{2DV_{dc1} + (1-D)V_{dc2}}{1-3D} \\ V_{C2} = \dfrac{(1-D)V_{dc1} + 2DV_{dc2}}{1-3D}. \end{cases} \quad (12)$$

The peak dc-link voltage across the inverter main circuit is expressed in (5) and can be rewritten as:

$$V_{PN} = V_{C1} + V_{C2} = \frac{1+D}{1-3D}(V_{dc1} + V_{dc2}) = B_r V_{dc}, \quad (13)$$

where $V_{dc} = V_{dc1} + V_{dc2}$ is the total input voltage. The boost factor of the proposed rESL-ZSI, B_r, is defined by:

$$B_r = \frac{1+D}{1-3D}. \quad (14)$$

Comparing (14) to (2), the boost factor of the proposed rESL-ZSI is the same as that found in the SL-ZSI [14].

B. cESL-ZSI Circuit Analysis

In the non-shoot-through state, as shown in Fig. 5(a), the obtained equations are similar to (3)-(6). In the shoot-through state, as shown in Fig. 5(b), we obtain:

$$v_{L1} = V_{C1} \qquad v_{L4} = V_{C2} \quad (15)$$

$$v_{L2} = V_{C2} + V_{dc2} \qquad v_{L3} = V_{C1} + V_{dc1} \quad (16)$$

$$i_{C1} = -2I_{L3} \quad i_{C2} = -2I_{L2} \qquad i_{in1} = I_{L3} \quad i_{in2} = I_{L2}. \quad (17)$$

Applying the volt-second balance principle to inductors and capacitors, from (3), (4), (6), and (15)-(17), obtains:

$$\begin{cases} V_{C1} = \dfrac{2DV_{dc1} + (1-D)V_{dc2}}{(1+D)(1-3D)} \\ V_{C2} = \dfrac{(1-D)V_{dc1} + 2DV_{dc2}}{(1+D)(1-3D)} \\ I_L = I_{L1} = I_{L2} = I_{L3} = I_{L4} = \dfrac{1-D}{1-3D} i_i \\ I_{in} = I_{in1} = I_{in2} = I_L. \end{cases} \quad (18)$$

The peak dc-link voltage cross the inverter main circuit is expressed in (5) and can be rewritten as:

$$V_{PN} = V_{C1} + V_{C2} = \frac{1}{1-3D}(V_{dc1} + V_{dc2}) = B_c V_{dc}. \quad (19)$$

The boost factor of the proposed cESL-ZSI, B_c, is defined by:

$$B_c = \frac{1}{1-3D}. \quad (20)$$

Comparing (20) to (2), the boost factor of the proposed cESL-ZSI is lower than that found in the SL-ZSI [14].

Fig. 6 shows the boost factor versus the duty cycle for the different topologies; curves 1, 2, and 3 are derived from (1), (20), and (14), respectively. The boost ability of the proposed embedded switched-inductor Z-source inverters is higher than that of the classic Z-source inverter [2]. From (12), (13), (18) and (19), we can observe that the proposed inverter topologies are symmetrical when $V_{dc1} = V_{dc2} = V_{dc}/2$. In case two split dc voltage sources $V_{dc}/2$ are not identical, there is no problem at the operation of proposed topologies. In this case, the proposed inverter topologies are asymmetrical and, thereby, $V_{c1} \neq V_{c2}$ as shown in (12) and (18).

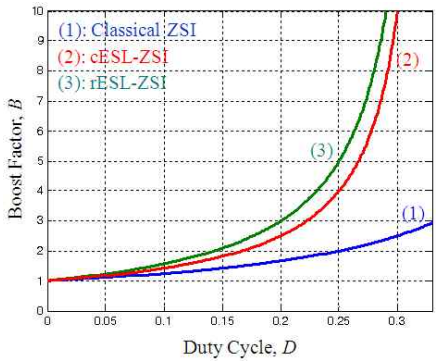


Fig. 6. Comparison of the boost ability of proposed topologies to classic topology: (1) classic Z-source inverter, ZSI, (2) proposed continuous input current embedded switched-inductor Z-source inverter, cESL-ZSI, and (3) proposed ripple input current embedded switched-inductor Z-source inverter, rESL-ZSI.

C. PWM Control for the Proposed Embedded Switched-Inductor Z-Source Inverters

Three basic PWM control methods, simple, maximum [3], and constant boost control [4], work with the proposed ESL-ZSIs. These methods are presented in details in [3] and [4]. The simple boost control method was used for the analysis, simulation, and experiment in this paper. The simple boost control method uses a straight line, whose amplitude is equal to or greater than the peak value of the three-phase references, in order to generate the shoot-through states. The duty cycle of the shoot-through state, D can be adjusted as a constant value. The maximum duty cycle of the shoot-through state is:

$$D = (1 - M) \quad (21)$$

where M is the modulation index.

Substituting (21) into (14) and (20), we get the equivalent boost factor for the rESL-ZSI and cESL-ZSI:

$$\begin{cases} B_r = \dfrac{2-M}{3M-2} \\ B_c = \dfrac{1}{3M-2}. \end{cases} \quad (22)$$

The peak value of the phase voltage from the inverter output is expressed by:

$$\hat{v}_{ph} = M \cdot V_{PN}/2 = M \cdot B \cdot V_{dc}/2, \quad (23)$$

where B is B_r or B_c.

The voltage gains (MB) of the rESL-ZSI and cESL-ZSI are defined by:

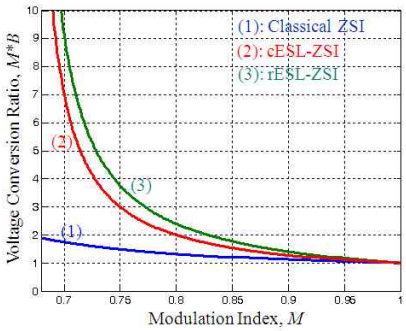


Fig. 7. Voltage conversion ratios versus modulation index for different topologies using simple boost control method.

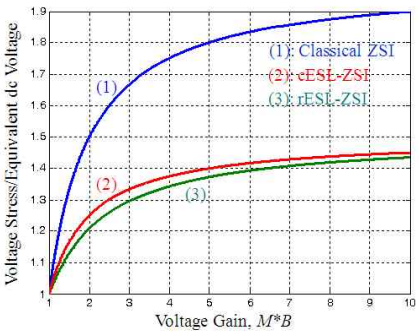


Fig. 8. Voltage stress comparison of the proposed embedded switched-inductor Z-source inverters to the classic ZSI.

$$\begin{cases} G_r = \dfrac{\hat{v}_{ph}}{V_{dc}/2} = M \cdot B_r = \dfrac{2M - M^2}{3M - 2} \\ G_c = M \cdot B_c = \dfrac{M}{3M - 2}. \end{cases} \tag{24}$$

Fig. 7 shows the voltage conversion ratios versus the modulation indices of the different topologies under simple boost control. Compared with the classic Z-source inverter [2] and using the same modulation index, the proposed inverters provide a higher voltage boost inversion. Therefore, for the same voltage conversion ratio, the proposed inverters use a higher modulation index in order to improve the inverter output quality.

The voltage stress V_s across the switching devices can be defined by the ratio of its peak dc link voltage to the minimum dc voltage (GV_{dc}) needed for the traditional ZSI to generate the same ac output voltage at M = 1 [4]. This ratio relates to the extra cost for the inverters to obtain the voltage boost and to the higher voltage stress. The respective ratios of the voltage stress to the equivalent dc voltage for the rESL-ZSI and cESL-ZSI can be expressed as:

$$\begin{cases} \dfrac{V_S}{G_r V_{dc}} = \dfrac{B_r V_{dc}}{G_r V_{dc}} = \dfrac{2 + 3G - \sqrt{9G^2 - 4G + 4}}{2G - 9G^2 + 3G\sqrt{9G^2 - 4G + 4}} \\ \dfrac{V_S}{G_c V_{dc}} = \dfrac{B_c V_{dc}}{G_c V_{dc}} = \dfrac{3}{2} - \dfrac{1}{2G}. \end{cases} \tag{25}$$

Fig. 8 shows the active switch voltage stress comparison of the proposed embedded switched-inductor Z-source inverters to the classic ZSI. As shown in Fig. 8, for the same dc-ac output voltage gain the proposed inverters have a lower voltage stress across the active switching devices. Therefore, the proposed inverters have many benefits in high voltage gain applications.

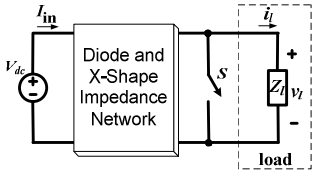


Fig. 9. Unified and simplified equivalent circuit of impedance-type power inverters, i.e., proposed inverters, switched-inductor ZSI, embedded ZSI, and classic ZSI.

D. Input Current Ripple and Stress Comparisons to the Other Topologies

Differing control conditions cause varied input current ripples in power inverters. For comparison, we assume that the inductor current ripple for all of the inverters is small and ignorable. The simple boost control was used to analyze the characteristics of the input current ripple for the proposed rESL-ZSI, the proposed cESL-ZSI, the SL-ZSI [14], the embedded ZSI [19], and the classic ZSI [2]. This simplifies them, as shown in Fig. 9. The ac side circuit is represented by its simplified equivalent dc load [7]. An inductive load impedance ($Z_l = R_l + sL_l$) directly connects in parallel with the active switch S in Fig. 9, where i_l and v_l are the instantaneous load current and voltage, respectively. I_l and V_l are the average current and voltage during a switching cycle in the steady state.

Using the steady-state analysis method found in [7] for Fig. 9, we obtained the voltage and current stresses on the main components, such as the power switch, D_{in}, L, C, and the dc link. For the switched-inductor Z-source inverter, the input current is expressed as:

$$I_{in} = 2I_L - I_l. \tag{26}$$

In the shoot-through state, I_{in} = 0, and in the traditional zero-state, I_l = 0; therefore, $I_{in} = 2I_L$. In the active states, $I_{in} = 2I_L - I_l$. In the steady state, the inductor current of the switched-inductor Z-source inverter as shown in Fig. 2 is expressed by:

$$I_L = \frac{1 - D}{1 - 3D} I_l \bigg|_{D=1-M} = \frac{M}{3M - 2} I_l. \tag{27}$$

Substituting (27) into (26), the average input current of the switched-inductor Z-source inverter [14] is:

$$\overline{I_{in}} = (1 - D)(2I_L - I_l)|_{D=1-M} = (2 - M)I_L. \tag{28}$$

Fig. 10 shows the detailed input current for the SL-ZSI topology. The deviation of the input current and its average value is expressed by:

$$\Delta I_{in} = |I_{in} - (2-M)I_L| = |2I_L - I_l - (2-M)I_L| = |M \cdot I_L - I_l|. \tag{29}$$

For the rESL-ZSI shown in Fig. 3(a), the input current in the non-shoot-through state is I_L; the input current in shoot-through state is $2I_L$. The average input current of the rESL-ZSI, as expressed in (10), is:

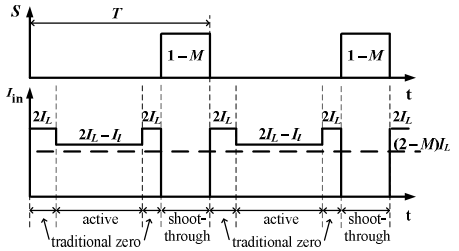


Fig. 10. SL-ZSI input current ripple.

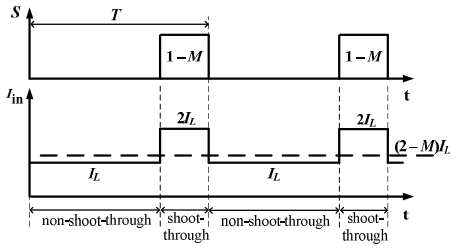


Fig. 11. rESL-ZSI input current ripple.

$$\overline{I_{in}} = (1 + D)I_L|_{D=1-M} = (2 - M)I_L. \quad (30)$$

The detailed input current for the proposed rESL-ZSI topology is shown in Fig. 11. The deviation of the input current and its average value is expressed by:

$$\Delta I_{in} = |I_{in}-(2- M)I_L| = |I_L - (2 - M)I_L| = |(1 - M)I_L|. \quad (31)$$

For the cESL-ZSI shown in Fig. 3(b), the input current is I_L. Therefore, the input current ripple in the cESL-ZSI is negligible and equal to zero. Table I compares the input current ripple equations for the proposed inverters to the other topologies for the same M and V_{dc}. In Table I, the peak value of the phase voltage $\hat{v}_{ph}$ from the inverter output is obtained using the simple boost control method [3]. Table I shows that the voltage and current stresses of the proposed cESL-ZSI are lower than those of the rESL-ZSI and of the SL-ZSI for the same M and V_{dc}.

When the cESL-ZSI or the rESL-ZSI replaces a SL-ZSI [14] in a particular case, V_{dc} and $\hat{v}_{ph}$ are usually fixed. If we guarantee that the modulation index in the SL-ZSI [14] and the rESL-ZSI is s, the corresponding modulation index in the cESL-ZSI will be $\frac{2s^2 - 4s}{3s^2 - 3s - 2}$ in order to produce the same $\hat{v}_{ph}$ from the same V_{dc}, when using the simple boost control. Table II gives the resulting voltage and current stresses of the proposed rESL-ZSI, the proposed cESL-ZSI and the SL-ZSI. The proposed inverters incur lower voltage stress on the capacitors, and a lower input current ripple in comparison with the SL-ZSI [14] for the same V_{dc}, $\hat{v}_{ph}$ and R_l. The current stresses and voltage stress on the switches and diodes of the proposed rESL-ZSI are the same as those of the SL-ZSI, whereas the current stresses and voltage stress on the switches and diodes of the proposed cESL-ZSI are higher than those of the SL-ZSI for the same V_{dc}, $\hat{v}_{ph}$, R_l and passive components.

TABLE I

GOVERNING CURRENT AND VOLTAGE EQUATIONS FOR THE SAME M AND V_{DC}

	rESL-ZSI	cESL-ZSI	SL-ZSI	Embedded ZSI	Classical ZSI
$\hat{v}_{ph}$	$\frac{2M - M^2}{3M - 2}\frac{V_{dc}}{2}$	$\frac{M}{3M - 2}\frac{V_{dc}}{2}$	$\frac{2M - M^2}{3M - 2}\frac{V_{dc}}{2}$	$\frac{M}{2M - 1}\frac{V_{dc}}{2}$	$\frac{M}{2M - 1}\frac{V_{dc}}{2}$
V_C	$\frac{1}{M}\hat{v}_{ph}$	$\frac{1}{M}\hat{v}_{ph}$	$\frac{2}{2 - M}\hat{v}_{ph}$	$\frac{1}{M}\hat{v}_{ph}$	$2\hat{v}_{ph}$
V_{PN} V_{Din}	$\frac{2}{M}\hat{v}_{ph}$	$\frac{2}{M}\hat{v}_{ph}$	$\frac{2}{M}\hat{v}_{ph}$	$\frac{2}{M}\hat{v}_{ph}$	$\frac{2}{M}\hat{v}_{ph}$
I_L	$\frac{M^2}{3M - 2}\frac{V_{PN}}{R_l}$	$\frac{M^2}{3M - 2}\frac{V_{PN}}{R_l}$	$\frac{M^2}{3M - 2}\frac{V_{PN}}{R_l}$	$\frac{M^2}{2M - 1}\frac{V_{PN}}{R_l}$	$\frac{M^2}{2M - 1}\frac{V_{PN}}{R_l}$
I_{Din}	$2I_L - I_l$	$2I_L - I_l$	$2I_L - I_l$	$2I_L - I_l$	$2I_L - I_l$
I_{sh}	$4I_L$	$4I_L$	$4I_L$	$2I_L$	$2I_L$
I_l	MV_{PN} / R_l	MV_{PN} / R_l	MV_{PN} / R_l	MV_{PN} / R_l	MV_{PN} / R_l
i_{in}	I_L; $2I_L$	I_L	0; $2I_L - I_l$; $2I_L$	I_L	0; $2I_L - I_l$; $2I_L$
$\overline{I_{in}}$	$(2 - M)I_L$	I_L	$(2 - M)I_L$	I_L	I_L
ΔI_{in}	$\|(1-M)I_L\|$	0	$\|M \cdot I_L - I_l\|$	0	$\|I_L - I_l\|$

where I_{Din}, I_{sh}, I_l, i_{in} and R_l are the peak current across the diode D_{in}, the peak shoot-through current across the main power circuit during the shoot-through state, the average load current, the instantaneous input current, and the equivalent load register, respectively.

TABLE II

GOVERNING CURRENT AND VOLTAGE EQUATIONS FOR THE SAME V_{DC}, $\hat{v}_{ph}$ AND R_L

	SL-ZSI	rESL-ZSI	cESL-ZSI
$\hat{v}_{ph}$	$\frac{2s - s^2}{3s - 2}\frac{V_{dc}}{2}$		
V_C	$V_{Cs} = \frac{s}{3s - 2}V_{dc}$	$\frac{-s + 2}{2s}V_{Cs} < V_{Cs}$	$\frac{-3s^2 + 3s + 2}{4s}V_{Cs} < V_{Cs}$
V_{PN} V_{Din}	$V_{PNs} = \frac{2 - s}{s}V_{Cs}$		$\frac{-3s^2 + 3s + 2}{-2s + 4}V_{PNs} > V_{PNs}$
I_L	$I_{Ls} = \frac{s^2}{3s - 2}\frac{V_{PNs}}{R_l}$		$(2 - s)I_{Ls} \geq I_{Ls}$
I_{Din}	$I_{Dins} = \frac{2 - s}{s}I_{Ls}$		$\frac{2s^2 - s - 2}{s - 2}I_{Dins} > I_{Dins}$
I_{sh}	$I_{shs} = 4I_{Ls}$		$(2 - s)I_{shs} \geq I_{shs}$
I_l	sV_{PNs} / R_l		
i_{in}	0; $2I_{Ls} - I_l$; $2I_{Ls}$	I_{Ls}; $2I_{Ls}$	$(2 - s)I_{Ls}$
$\overline{I_{in}}$	$(2 - s)I_{Ls}$		
ΔI_{in}	$\Delta I_{ins} = \frac{s^2 - 3s + 2}{s}I_{Ls}$	$\frac{s}{2 - s}\Delta I_{ins} \leq \Delta I_{ins}$	0

IV. SIMULATION RESULTS

PSIM simulations were used to verify the features of the proposed inverters as shown in Fig. 3. The simulation parameters were $L_1 = L_2 = L_3 = L_4 = 1$ mH, $C_1 = C_2 = 1000$ μF, and $V_{dc} = 60$ V. The switching frequency was 10 kHz; the three-phase balanced load was $R = 50$ Ω/phase and $L_l = 4.5$ mH/phase. The simple boost control method was used. In the

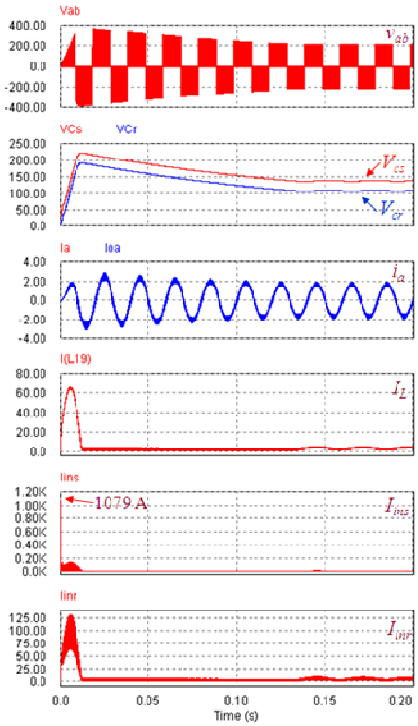


Fig. 12. Simulation results using simple boost control for rESL-ZSI and SL-ZSI with M = 0.78 and T_0/T = 0.22. From top to bottom: output line-to-line voltage v_{ab}, SL-ZSI capacitor voltage V_{Cs}, rESL-ZSI capacitor voltage V_{Cr}, output current i_a, inductor current I_L, SL-ZSI input current I_{ins}, and rESL-ZSI input current I_{inr}.

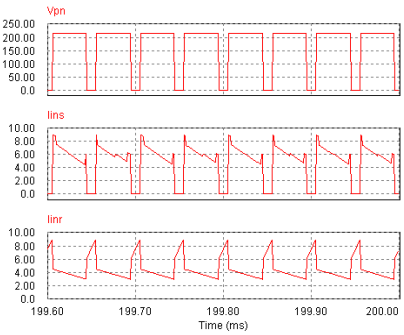


Fig. 13. Simulation results for enlarged steady state waveforms for rESL-ZSI and SL-ZSI with M = 0.78 and T_0/T = 0.22. Top: dc-link voltage, center: SL-ZSI input current, bottom: proposed rESL-ZSI input current.

simulation, all of the components were ideal; the initial state of the capacitors was set to 0 V. For the proposed rESL-ZSI and the SL-ZSI, we set M = 0.78. To produce the same output voltage as the proposed rESL-ZSI from the same input voltage, the modulation index for the proposed cESL-ZSI needed to be 0.757.

Figs. 12 and 13 show the simulation results for the proposed rESL-ZSI and the SL-ZSI when V_{dc1} = V_{dc2} = 30 V, M = 0.78 and T_0/T = 0.22. From Figs. 12 and 13, we can see that both the SL-ZSI and the rESL-ZSI produce the same 215

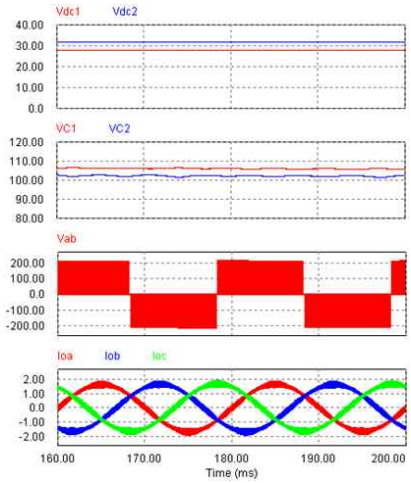


Fig. 14. Simulation results of the proposed rESL-ZSI when V_{dc1} = 28 V, V_{dc2} = 32 V, M = 0.78 and T_0/T = 0.22. From top to bottom: input voltages, capacitor voltages, line-to-line voltage and output phase currents.

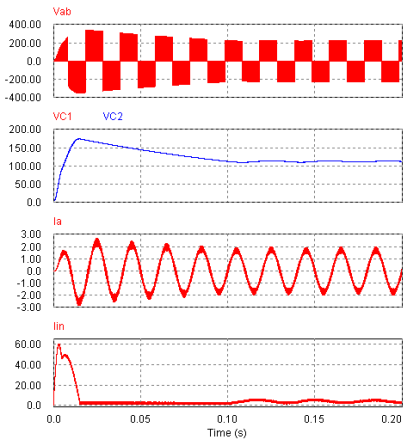


Fig. 15. Simulation results using simple boost control for cESL-ZSI with M = 0.757 and T_0/T = 0.243. From top to bottom: output *line*-to-line voltage, capacitor voltage, output current, and input current I_{in}.

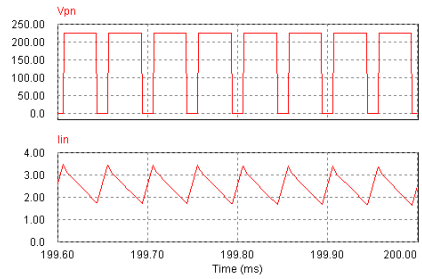


Fig. 16. Simulation results for enlarged cESL-ZSI waveforms in steady state with M = 0.757 and T_0/T = 0.243. Top: dc-link voltage, bottom: input current.

V peak dc-link voltage, V_{PN} and the same 1.16 A_{rms} phase current, i_a; the capacitor voltage for the SL-ZSI was boosted to 136 V whereas the capacitor voltage for the rESL-ZSI was 106 V in the steady state. The input current of the rESL-ZSI had a lower ripple than that found for the SL-ZSI. A huge

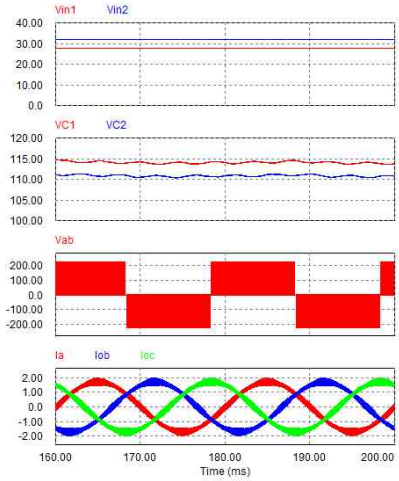


Fig. 17. Simulation results of the proposed cESL-ZSI when V_{dc1} = 28 V, V_{dc2} = 32 V, M = 0.757 and T_0/T = 0.243. From top to bottom: input voltages, capacitor voltages, line-to-line voltage and output phase currents.

inrush current that could destroy the devices occurred at the SL-ZSI startup.

In order to verify that there is no problem at the operation in case two split DC voltage sources $V_{dc}/2$ are not identical, Fig. 14 shows the simulation results of the proposed rESL-ZSI when V_{dc1} = 28 V, V_{dc2} = 32 V, M = 0.78 and T_0/T = 0.22. The voltages of the capacitors (C_1 and C_2) are respectively boosted to 109 V and 105 V from the total input voltage of 60 V; the voltage gain is the same as in case V_{dc1} = V_{dc2} = 30 V.

Figs. 15 and 16 show the simulation results for the proposed cESL-ZSI when V_{dc1} = V_{dc2} = 30 V, M = 0.757 and T_0/T = 0.243. The peak dc-link voltage of the cESL-ZSI was boosted to 220 V. The output phase current was also 1.16 Arms, and the capacitor voltage of the cESL-ZSI was boosted to 110 V in the steady state. The input current of the cESL-ZSI was flat and the same went for the inductor current. Fig. 17 shows the simulation results of the proposed rESL-ZSI when V_{dc1} = 28 V, V_{dc2} = 32 V, M = 0.757 and T_0/T = 0.243. The capacitor C_1 and C_2 voltages are respectively boosted to 112 V and 109 V from the total input voltage of 60 V; the voltage gain is the same that in case V_{dc1} = V_{dc2} = 30 V.

As shown in Figs. 12 to 17, producing the same 1.16 A_{rms} output phase current from the 60 V input dc voltage creates a lower capacitor voltage stress, a lower input current ripple, and a smaller startup inrush current occurred in the proposed inverters, compared to the SL-ZSI. As shown in Fig. 12, the V_{cs} of the capacitors in the SL-ZSI was initially at 30 V, but had no initial value in the proposed rESL-ZSI and cESL-ZSI, as the initial voltage across the Z-source capacitors is zero and the huge inrush current flows through diode D_{in}, C_1, C_2 and charges the capacitors immediately to V_c = $V_{dc}/2$ = 30 V, as shown in Fig. 2 in the switched inductor Z-source inverter.

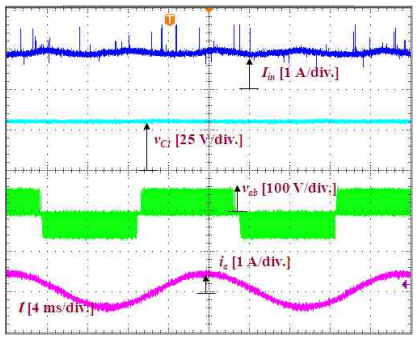


Fig. 18. Experiment waveforms of proposed rESL-ZSI when M = 0.78 and T_0/T = 0.0. From top to bottom: input current, capacitor C_1 voltage, output line-to-line voltage, and output phase current at 4 ms/div.

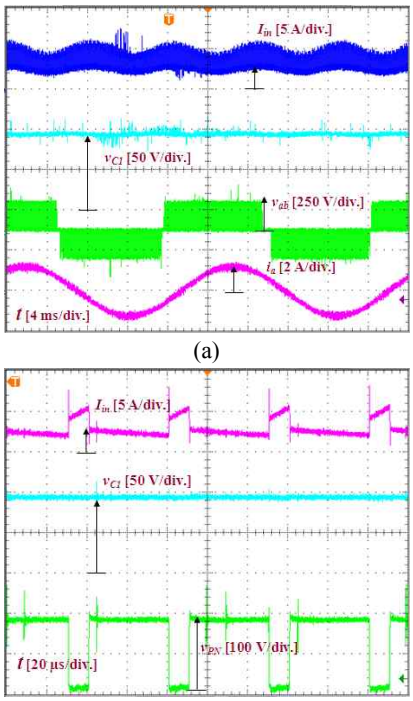


Fig. 19. Experiment results of proposed rESL-ZSI when M = 0.78 and T_0/T = 0.22. (a) From top to bottom: input current, capacitor C_1 voltage, output line-to-line voltage, and output phase current at 4 ms/div. (b) Top: input current, center: capacitor C_1 voltage, bottom: dc-link voltage at 20 µs/div.

The capacitors in the proposed rESL-ZSI and cESL-ZSI have no initial value because no current flows to the main circuit at startup. In case two split DC voltage sources $V_{dc}/2$ are not identical, Figs. 14 and 17 show that there is no problem at the operation of proposed topologies. In this case, the proposed inverter topologies are asymmetrical and thereby $V_{c1} \neq V_{c2}$.

V. Experimental Verifications

We constructed a laboratory prototype based on a TMS320F2812 DSP in order to verify the properties of the proposed rESL-ZSI and cESL-ZSI. The prototype used the same parameters as used in the simulation. Fig. 18 shows the

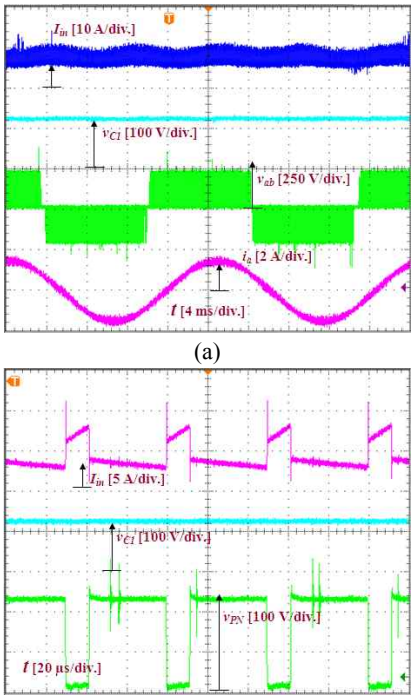


Fig. 20. Experiment results of proposed rESL-ZSI when M = 0.76 and T_0/T = 0.24. (a) From top to bottom: input current, capacitor C_1 voltage, output line-to-line voltage, and output phase current at 4 ms/div. (b) Top: input current, center: capacitor C_1 voltage, bottom: dc-link voltage at 20 µs/div.

experimental results for the proposed rESL-ZSI without a shoot-through state when M = 0.78 and T_0/T = 0.0. In Fig. 18, the waveforms from top to bottom are the input current, capacitor C_1 voltage, output line-to-line voltage, and the output phase current. The peak line-to-line voltage pulse is equal to the 60 V of the dc input voltage. This matches the theoretical analysis for the non-shoot-through state case. Next, we tested the high boost ability of the proposed rESL-ZSI by keeping M = 0.78 and increasing the shoot-through duration to T_0/T = 0.22. Fig. 19 shows the experiment waveforms for the proposed rESL-ZSI when M = 0.78 and T_0/T = 0.22. The dc-link voltage was boosted from 60 V to 182 V, the rms value of the phase current was 1 A_{rms}, and the instantaneous input current was I_L and $2I_L$, sequentially.

In order to verify more clearly the performance of proposed rESL-ZSI, Fig. 20 shows the experimental results when M = 0.76 and T_0/T = 0.24. The dc-link voltage was boosted from 60 V to 220 V, and the rms value of the phase current was 1.18 A.

Next, the system was reconfigured to reflect the proposed cESL-ZSI topology. Fig. 21 shows the experimental results for the no shoot-through state when M = 0.757 and T_0/T = 0.0. The peak line-to-line voltage pulse was equal to the dc input voltage of 60 V. We then set T_0/T = 0.243 and kept M = 0.757. Fig. 22 shows the experiment waveforms for the proposed rESL-ZSI when M = 0.757 and T_0/T = 0.243. The dc-link

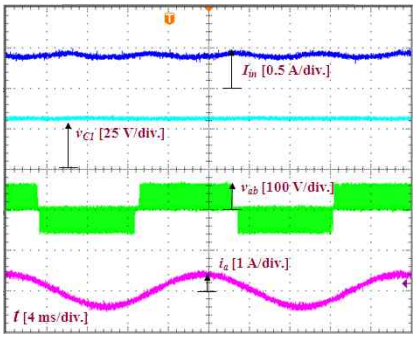


Fig. 21. Experiment waveforms of proposed cESL-ZSI when M = 0.757 and T_0/T = 0.0. From top to bottom: input current, capacitor C_1 voltage, output line-to-line voltage, and output phase current at 4 ms/div.

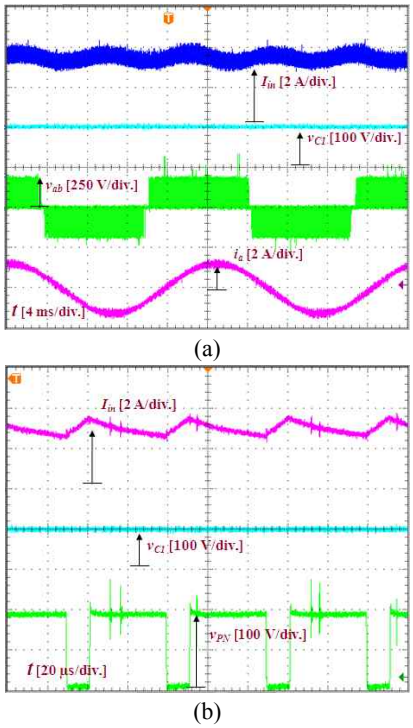
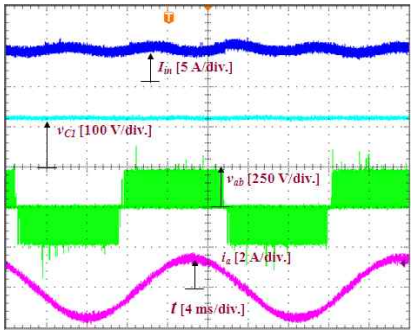


Fig. 22. Experiment results for proposed cESL-ZSI when M = 0.757 and T_0/T = 0.243. (a) From top to bottom: input current, capacitor C_1 voltage, output line-to-line voltage, and output phase current at 4 ms/div. (b) Top: input current, center: capacitor C_1 voltage, bottom: dc-link voltage at 20 µs/div.

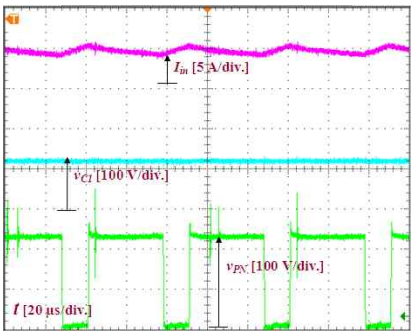
voltage was boosted from 60 V to 187 V, the rms value of the phase current was 1 A_{rms}, and the input current was continuous.

For a higher voltage of the proposed cESL-ZSI, Fig. 23 shows the experimental results when M = 0.74 and T_0/T = 0.26. The dc-link voltage was boosted from 60 V to 225 V, the rms value of the phase current was 1.18 A_{rms}, and the input current was flatter than that shown in Figs. 19 and 20 of the rESL-ZSI.

From Figs. 19 and 22, we observe that the voltage gain in experiment results is lower than that in simulation results. This is due to the system parasites appeared in the



(a)



(b)

Fig. 23. Experiment results of proposed cESL-ZSI when M = 0.74 and T_0/T = 0.26. (a) From top to bottom: input current, capacitor C_1 voltage, output line-to-line voltage, and output phase current at 4 ms/div. (b) Top: input current, center: capacitor C_1 voltage, bottom: dc-link voltage at 20 µs/div.

experimental setup. The measured efficiency of the proposed rESL-ZSI and cESL-ZSI at 1 A_{rms} output current approximates and only reaches 84.75%. This may be because the circuit parameters have not been selected optimally. The semiconductors such as power switches and diodes are the main contributors to the total loss of the proposed inverters. The simulation and experimental results show that the proposed rESL-ZSI and cESL-ZSI achieve a high boost inversion compared to the classic ZSI. When compared to the SL-ZSI [14], the proposed rESL-ZSI and cESL-ZSI have a lower voltage stress on the capacitors and a lower input current ripple for the same input and output voltages. In addition, the proposed inverters eliminate the startup inrush current.

VI. Conclusions

This paper proposed two types of embedded switched-inductor Z-source inverters, possessing either a ripple or continuous input current with the following main characteristics: a high boost voltage inversion ability and a continuous input current. Compared to the SL-ZSI, for the same input and output voltage, the proposed rESL-ZSI and cESL-ZSI offer reduced voltage stress on the capacitors, and can suppress the startup inrush current, which otherwise may destroy the devices. In addition, the dc input current in the proposed rESL-ZSI and cESL-ZSI flows smoothly without the need to add external second-order filters. Although the proposed rESL-ZSI can produce a higher output voltage gain in the case of the same modulation index and the same input voltage, its dc input current contains more ripple than that found in the proposed cESL-ZSI.

The experiment results for the 60 V_{dc} input verified the high step-up inversion ability; the simulation and experimental results show that the proposed inverters have a high boost inversion ability. Compared with a traditional combination of dc-dc converter and inverter, the advantages of the proposed inverters are described as follows: 1) the upper and lower devices of the same phase leg in the proposed inverters can be gated on simultaneously and thereby eliminate the dead time, which significantly improves the reliability and reduces the output waveform distortion; 2) they offer a simplified single stage power conversion topology with one active switch less. The proposed rESL-ZSI and cESL-ZSI are applicable for fuel cells or photovoltaic applications where a low input voltage is inverted to a high ac output voltage.

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