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Method of SSO Noise Reduction on FPGA of Digital Optical Units in Optical Communication

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Abstract

There is a growing need for optical communication systems that convert large volumes of data to optical signals and that accommodate and transmit the signals across long distances. Digital optical communication consists of a master unit (MU) and a slave unit (SU). The MU transmits data to SU using digital optical signals. However, digital optical units that are commercially available or are under development transmit data using two's complement representation. At low input levels, a large number of SSOs (simultaneous switching outputs) are required because of the high rate of bit switching in two's complement, which thereby increases the power noise. This problem reduces the overall system capability because a DSP (digital signal processor) chip (FPGA, CPLD, etc.) cannot be used efficiently and power noise increases. This paper proposes a change from two's complement to a more efficient method that produces less SSO noise and can be applied to existing digital optical units.

Keywords : Low Power Noise, Field Programmable Gate Array, Digital Optical Unit, Noise Figure, Simultaneous Switching Outputs

Ⅰ. INTRODUCTION

As an engineering technology to solve the problem of blind spots and to enhance network coverage, repeaters play an important role in present CDMA, W-CDMA, WiBro, GSM, and LTE mobile communication business networks[1~3]. Fig. 1 shows such a repeater in a network application.

The main components of a repeater are uplink and downlink transceivers, a DSP module, an optical module, a management module, and a power supply module. For different applications, there are different types of repeaters such as RF wideband repeaters, fiber optic repeaters, digital optical repeaters, and band selective repeaters. Among these repeaters, the digital optical repeater gives the highest performance for its price and is currently the most popular. The main specifications to note when evaluating a repeater are its intelligence (i.e., the local and remote monitors), the ACPR (adjacent channel power ratio), the noise figure, and reliability.

However, problems occur when repeaters are used for transmission optimization[4]. Power noise can add unwanted noise to the system, thereby adversely affecting the system's noise floor.

The SNR (signal-to-noise ratio) of a receiver is dominant in the Noise Figure. Hence, in order to compensate for the high SNR, we place an LNA (low noise amplifier) at the receiver's front end to improve

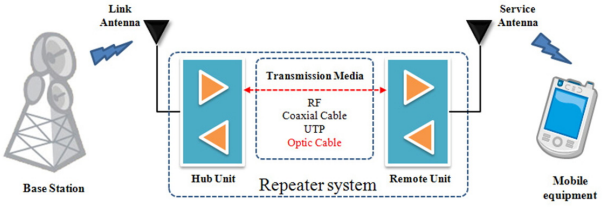

Fig. 1. Scheme of repeater in network application.

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the overall noise figure[5]. Despite the presence of the LNA, as the digital unit's noise figure in the middle of the system becomes higher, the noise figure of all systems proportionally becomes depleted.

Ⅱ. Related Works

Fig. 2 shows that the MU converts analog signals to digital signals with a 14-bit parallel data bus using an ADC (analog to digital converter) by digital sampling. Most current digital optical units use two's complement representation, since this method makes it easy to process digital signals and to understand the data. However, problems occur when transmitting data.

First, this study focuses on the power noise status of the optical module when transmitting data using two's complement and the relationship to the number of SSOs when using an FPGA chip in the DSP. As shown in Fig. 2, data conversion for each sampling mainly occurs when the ADC's input level is low. Data error is found because sample data is two's complement and there exists quantization noise. Table I lists the actual values of the sample data.

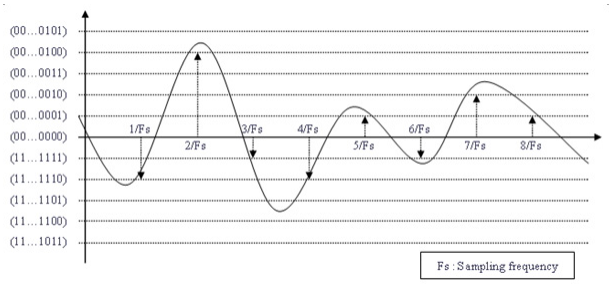

Fig. 2. Sampling on low-level input signal.

Table 1. Sampling Data.

Sampling frequency	Sampling data
1/Fs	**11 … 1110**
2/Fs	00 … 0100
3/Fs	11 … 1111
4/Fs	11 … 1110
5/Fs	00 … 0001
6/Fs	11 … 1111
7/Fs	00 … 0010
8/Fs	00 … 0001

As shown Table I, two's complement causes many changes in data when sampling low-level input signals. Excessive changes in data mean a large number of SSOs in the DSP chip.

If a DSP and an FPGA are used together, the SSO must be considered. If the number of SSOs becomes excessive, there is high possibility for transmission data to be lost because it reduces reliability and causes power noise. Moreover, it not only reduces the efficiency of the chip, but it can also cause the chip to malfunction. however, if the skew rate, meaning the fast drive strength, is 12 mA, around eight SSOs per bank are recommended. However, since FPGAs are relatively inexpensive, the number of recommended SSOs decreases. Currently, an increasing number of applications require large volumes of data transmission and wide broadb and range. Thus, FPGAs are more in demand. Since the number of SSOs must be limited, it is important to use them efficiently.

As shown in Table I, 12 SSOs are obtained for 14 bits when converting from 1/Fs to 2/Fs.

In Fig. 3, there is extensive switching data to paralleled data, and the serial data is transmitted in a data burst. The transceiver in the optical module consumes a large amount of current if the bit is "1" at serial transmission, while consuming lower current at bit "0" in consecutive sections. If this occurs repeatedly, power fluctuates which is the immediate cause of power noise. Fig. 4 indicates the power noise that results from the transmission of two's complement, as measured by an oscilloscope.

The test conditions are shown in Fig. 5: FS, 100

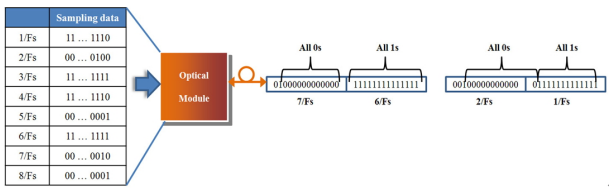

Fig. 3. Transmission of the parallel data.

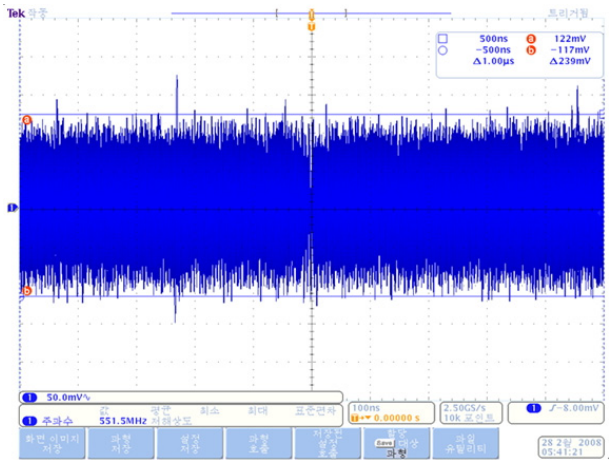

Fig. 4. Power noise of the two's complement type.

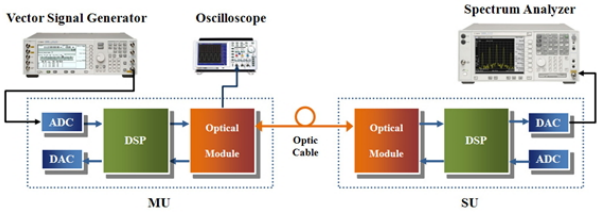

Fig. 5. Test environment.

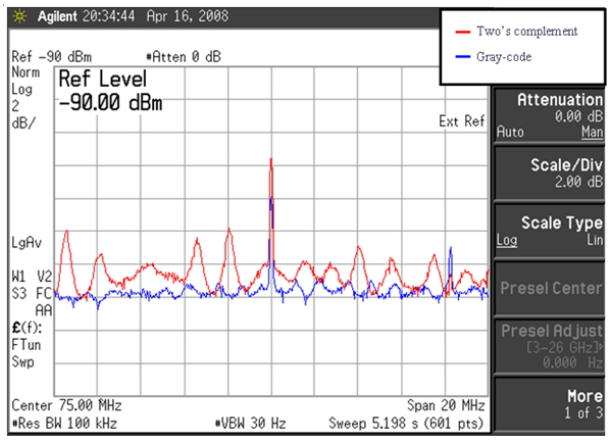

Fig. 6. Comparison of two's complement type and Gray-code type.

Table 2. Setting parameters of spectrum analyzer.

Parameter	Value
Center Frequency	**75 MHz**
Span	20 MHz
Ref level	-90 dBm
Sale/DIV	2 dB/DIV
Attenuator	0 dB
RBW	100 kHz
VBW	30 Hz

MSPS; digital optical module, 2.5 Gbps; single tone, -85 dBm made by a signal generator into the MU's ADC. The MU power is measured by an oscilloscope: oscilloscope input coupling, AC; impedance, 1 MΩ; vertical level, 50 mV/DIV. As shown in Fig. 6, the measured value is max 239 mV.

Under this condition, the DAC (digital-to-analog converter) of the SU is measured using a spectrum analyzer. The red line in Fig. 6 shows the pattern of the spectrum as measured by the spectrum analyzer. The settings of the spectrum analyzer are listed in Table 2.

As shown in Fig. 6, the red spectrum indicates that a low-level input signal comes into the ADC and is transmitted in two's complement. In this case, power noise increases, and spurious occurs within in-band of the spectrum. This impairs the noise figure.

Ⅲ. Data scrambling Scheme

As mentioned previously, two's complement presents many problems during the transmission of data. Data should be scrambled before it is transmitted in order to solve these problems. Various data scrambling methods exist: binary offset, Gray code, etc. Here, we will investigate the spectrum and power noise characteristics when scrambling data using Gray code. If two's complement is replaced by Gray code in Table 1, the obtained result is as shown in Table 3. Data conversion is processed by

Table 3. Gray Code Data.

Sampling frequency	Sampling data
1/Fs	**11 ··· 1110**
2/Fs	00 ··· 0100
3/Fs	11 ··· 1111
4/Fs	11 ··· 1110
5/Fs	00 ··· 0001
6/Fs	11 ··· 1111
7/Fs	00 ··· 0010
8/Fs	00 ··· 0001

the DSP.

Table 3 indicates that Gray code data conversion results in fewer data bursts than two's complement. Fewer data bursts indicate that the number of SSOs as well as power noise can be decreased.

Ⅳ. Analysis and Experiment Results

As shown in Fig. 5, the test environment is established for an actual test of the applied compression algorithm.

As shown in Fig. 7, the measurement value is 148 mV which shows an improvement of 91 mV over two's complement. Moreover, as shown in Fig. 6, spurious within in-band shows an improvement of 3 - 4 dB over two's complement.

If the input signal level to the ADC is high, improvement is seen in the power noise but not so much in SSO. As the signal level of the input data increases, the amount of data change decreases when compared to lower signal levels.

Considerations for data scrambling are as follows: to process data scrambling, a coding/encoding module must be added to the digital signal processing. The Gray code conversion mentioned previously should use the Gray code conversion part from two's complement data. Moreover, general sum or multiplication may not be possible for scrambled data.

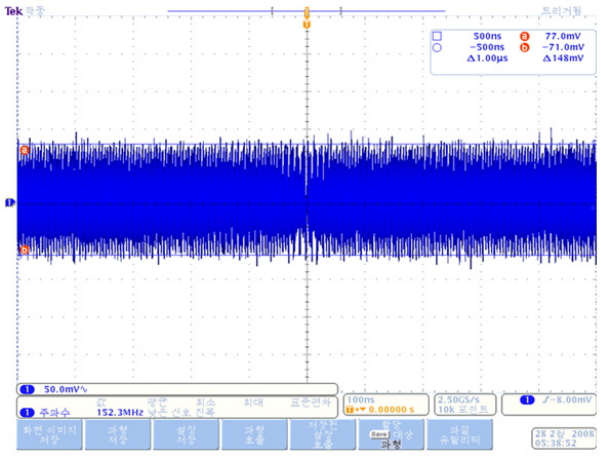

Fig. 7. Power noise of Gray code type.

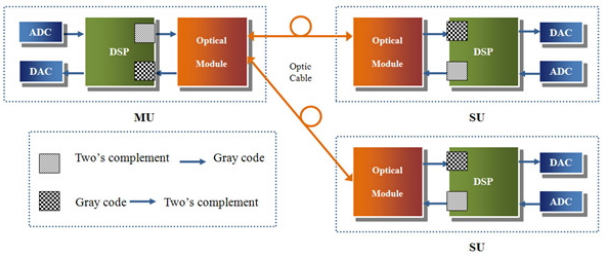

Fig. 8. Two's complement and the Gray code in digital optical unit.

Thus, the coding/encoding process must be required if there is a DSP in the middle of the transmission path. Fig. 8 indicates the location of the coding/encoding section, where data is converted from two's complement to Gray code. When the data is converted back from Gray code to two's complement in the DSP of the SU, transmission is complete.

If the coding/encoding module requires extensive resources or delay, the unit cost may increase owing to the change in the target device of the DSP. Moreover, since delay is a very important specification in mobile communication, it is necessary to select a scrambling method with less delay. Because coding/encoding is a very simple DSP process in Gray code, it presents no resource or delay problems Therefore, Gray code conversion is one of the best data scrambling methods available for digital optical communication, a finding which was also confirmed through tests.

Ⅴ. Conclusion

Data scrambling is one of the best methods for reducing power noise and increasing the efficiency of the FPGA's SSO resources. Previously installed digital optical transmission devices can also use data scrambling since it does not require any hardware modifications, but only DSP firmware updates. The device transmits low-level signals to the fixed device to minimize loss of power. The lower the power noise when low-level signals come into the device,

the more favorable is the service quality. This means that the lesser spurious, the better noise figure the system has. Eventually, this can lead to overall improvement in service quality.

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