

Performance inspection of smart superconducting fault current controller in radial distribution substation through PSCAD/EMTDC simulation

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Abstract

In power grid, in order to level out the generation with demand, up-gradation of the system is occasionally required. This will lead to more fault current levels. However, upgrading all the protection instruments of the system is both costly and extravagant. This issue could be dominated by using Smart Fault Current Controller (SFCC). While the impact of Fault current Limiters (FCL) in various locations has been studied in different situations for years, the performance of SFCC has not been investigated extensively. In this research, SFCC which has adopted the characteristics of a full bridge thyristor rectifier with a superconducting coil is applied to three main locations such as load feeder, Bus-tie position and main feeder location and its behavior is investigated through simulation in presence and absence of small Distributed Generation unit (DG). The results show a huge difference in limiting the fault current when using SFCC.

Keywords : SFCC, Full bridge thyristor rectifier, Distributed Generations, Bus-tie location

1. INTRODUCTION

Today, due to the inevitable load elevation, the power grid is more dynamically encountering changes than ever before, especially at distribution level where Distributed Generation Resources (DGR) have been installed; such as those resources are small wind power systems, photovoltaic systems, fuel cells, etc. One of the most conspicuous concerns which involve the whole protection system in this case, is the amount of fault current which will rush through the system. In radial distribution systems where the generation unit is located at one side and the loads are at the opposite side, the proper location for fault current controllers is the branches connected to the generation bus. However, this concept is not true in presence of DG units. When Distributed Generations are installed there will be two major challenges in consequence; (1) the output power may be dynamically changing, e.g. alterations in mechanical power of the wind generator and (2) some of the DGs are combined with loads so the power flow is not necessarily in one way from generation to the load and the DG unit can act as either load or generator [1]. In this paper, authors demonstrated the high fault current caused by DG unit and the effectiveness of the Smart Fault Current Controller (SFCC) on mitigating this faulty situation. For achieving this objective, there are different kinds of Fault Current Limiters. One of the most flexible ways to maintain and control the fault current to the desired level is by using full bridge thyristor rectifiers. The superconducting coil is considered for the fault current controller in this study to

mitigate the first half cycle peak of fault current.

By using other Fault Current Limiters, such as resistive or inductive types, current modification is done to a specific pre-considered amount and is not adjustable enough. Using power electronic devices in the structure of the fault limiter in addition to a smart control center in SFCC gives the ability to maintain and control the fault current to a desired level continuously.

SFCC adopts a full bridge thyristor rectifier using a superconducting coil, a thyristor control circuit which produces the pulse signals for the gate when a fault occurs. In normal operation the related angle for thyristors is zero, and coil current is rectified through thyristors and, a large inductor constructed by a superconducting coil [1]. The structure of SFCC is displayed in [1], [4]. The schematic view of the model which is used in this study is delineated in [2].

This paper tends to investigate the operation of SFCC in a typical Bus-tie location in absence and presence of DGs via PSCAD/EMTDC simulation. To study the effect of the SFCC on the contribution of the DG unit, the point of measurement for fault current is considered at the load side where fault has happened. Placement of the device in main feeder, and load feeder location is also studied briefly.

2. SFCC SPECIFICATIONS

The main topology is similar to a full-wave rectifier, called a bridge, the operational principle can be explained as a rectifier. The superconducting coil has no resistance and large inductance. The voltage drop is caused by just

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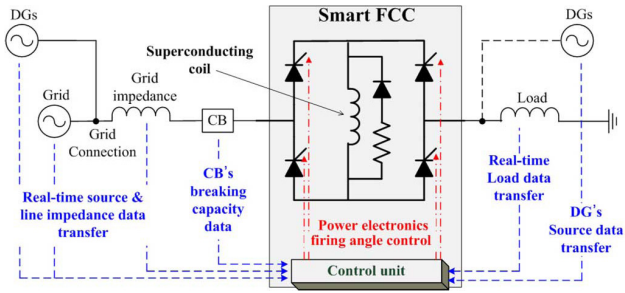


Fig. 1. Schematic drawing showing the smart FCC and location in a grid with grid-connected DG's.

thyristors, or any other solid-state if replaced, since the coil is superconducting state and almost zero ac loss. Fig. 1. Shows the structure of the SFCC and its operation procedure [1].

when a fault occurs, the coil current should be increased. at this time, the large inductance of the coil reduces an abrupt surge at the first swing. After the first swing of half cycle, a control unit supplies controlled gate signals to the four thyristors. These gate signal delay can adjust the fault current level. In a range of 0 to 180 degrees, the delay angle can be selected. For example, if the delay is 0 degree, this FCC operates like a bridge-type SFCL employing power diodes, so-called a dc reactor type SFCL. If the delay is 180 degrees, there is no signal to any thyristors, which means line current is cut off [1].

3. SIMULATION ON SFCC LOCATIONS

The location of the SFCC in power grid is a considerable concern due to the deviation of the current which is streaming through SFCC when it is applied to different places; it is momentous as critical current of the superconducting coil may be breached. In modern power grids, huge amount of electricity demands required system buses to be more interconnected in order to maintain the reliability of the system, avoid circuit element short circuit stresses and so on. The most significant obstacle in Bus-tie situations is the enormous rise in fault currents especially in presence of DG units. In order to overcome this problem, a SFCC in Bus-tie location seems to be beneficial [3].

3.1. Three main locations

At distribution level, there are various locations for a fault current limiter to be installed in. Three main locations are: main feeder location which is the connection between the main sources of power at transmission level to the distribution level; load feeder location which transmit the electric power for the loads at the end of the distribution line; Bus-tie location which allows two separate buses to be interconnected considering power and voltage stability.

For the sake of the accuracy, the characteristics of all lines and transformers and loads for three simulated locations are considered the same. The electric power of the system was modeled as a single generator with no impedance to conduct the properties of an infinite bus with

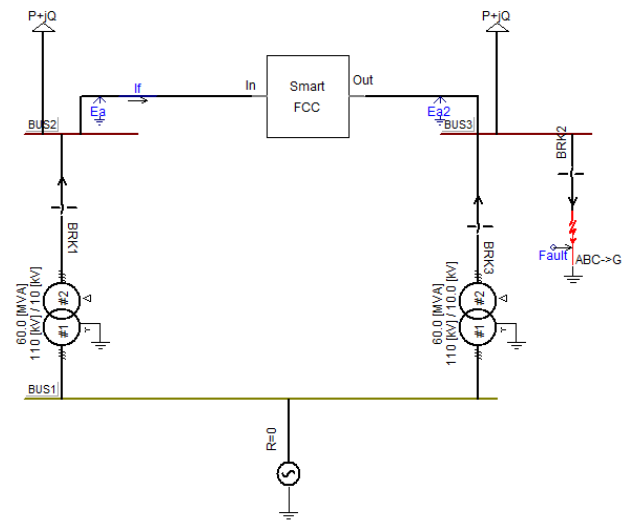


Fig. 2. Schematic view of simulated Bus-tie SFCC in absence of distributed generation.

voltage magnitude of 110 kV. The main system is connected to the low voltage side via two 110/10 kV, 60 MVA/ph step-down transformers. Two identical loads with real power of 17 MW/ph and reactive power of 10.53 MVAR/ph are connected to bus2 and 3. Since there is no mutual impedance or capacitance between phases, the short length lines could be modeled as Pi circuit. The applied fault is a permanent three phase to ground fault which is applied to bus3 after 0.5s. In consideration of revealing the acceptable effect of SFCC on each of the locations, the simulation is performed once with SFCC and once without it.

3.2. Bus-tie location: no DGR

Fig. 2. Demonstrates the schematic view of SFCC in Bus-tie location when there is no distributed generation presents. Since the properties of the connection between higher voltage and lower voltage side are the same, the current from the source is distributed to two equal divisions. In this situation, Fault Current Controller is feasible to mitigate half of the current from the main upstream source. Fig. 3. (a) and (b) show the results for current wave form when SFCC is offline and online respectively. In case (a), right after the fault happens, the first half cycle abruptly surges to 18.5 kA and then it gradually declines to 14.1 kA due to the natural impedances of the grid. However, by using SFCC the first half cycle was mitigated to 16.3 kA due to the superconducting characteristics which was modeled as a nonlinear function in [2]. Finally the current is controlled and limited to 2.1 kA in about 0.2 s.

3.3. Bus-tie location: with DGR

Fig. 4. Exhibits the view of the circuit with a generator added to bus2 as a model for a small distributed generation unit. The characteristics of this generation unit are as below; power magnitude: 10MW, voltage magnitude: 3.5 kV, resistance of 1 Ω , inductance of 0.1 H. The SFCC in this condition is eligible to control total fault current of DG

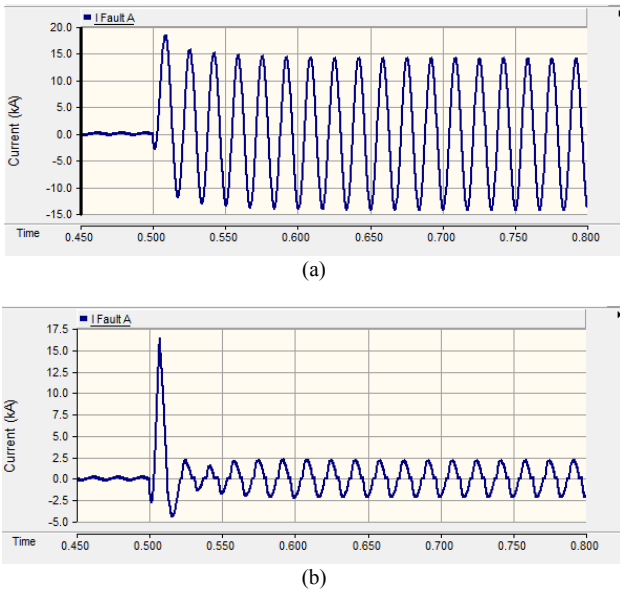


Fig. 3. Current wave form with no DG when (a) SFCC is not present in Bus-tie location and (b) SFCC is present.

and half of the current of upstream power source. Fig. 5. (a) and (b) Show the effect of a small distributed generation on fault current when SFCC is not in the circuit and when it is working, respectively. As it is exposed in the waveforms, the fault current is almost doubled when there is another source of generation besides the main source. In first half cycle, the current hits the highest point at 44.3 kA but eventually it is slightly decreased to 39 kA. By applying the SFCC in the system, the superconducting coil managed to control the first half cycle to 29.3 kA and the fault current was plunged to 4.3 kA.

3.4. Load feeder location

In this model, the SFCC was applied to the load at bus3 which is connected to the distributed source by an interconnection. SFCC protects the load from any fault current which is injected to the load from main source and DG unit. Since in the practical power system the numbers of loads which need to be protected from faults are numerous, a SFCC which placed in load feeder seems to be unreasonable from the economical point of view. Fig. 6.

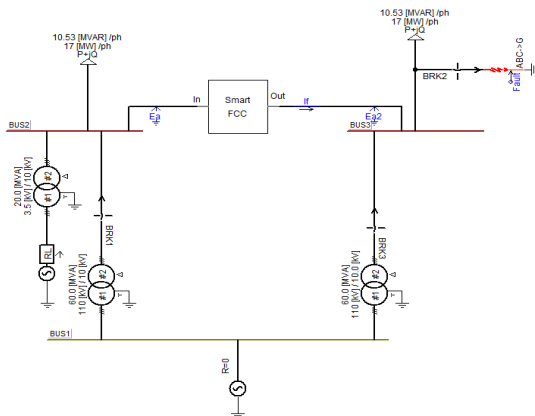


Fig. 4. view of simulated Bus-tie SFCC in presence of distributed generation.

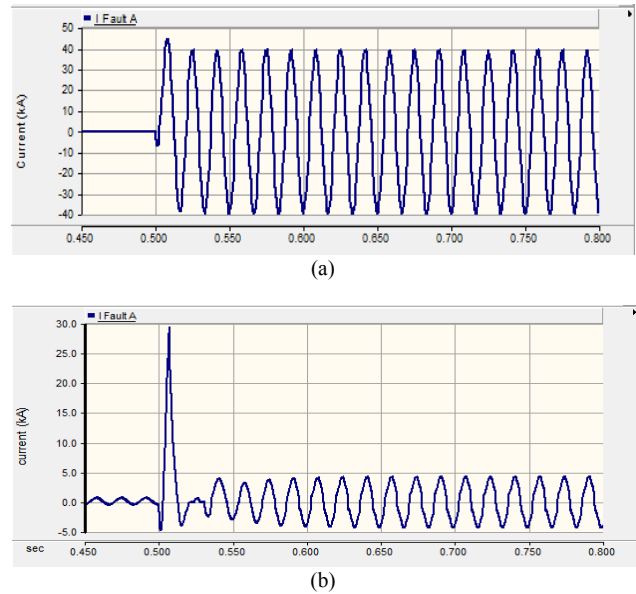


Fig. 5. Current wave form with DG when (a) SFCC is not present in Bus-tie location and (b) SFCC is present.

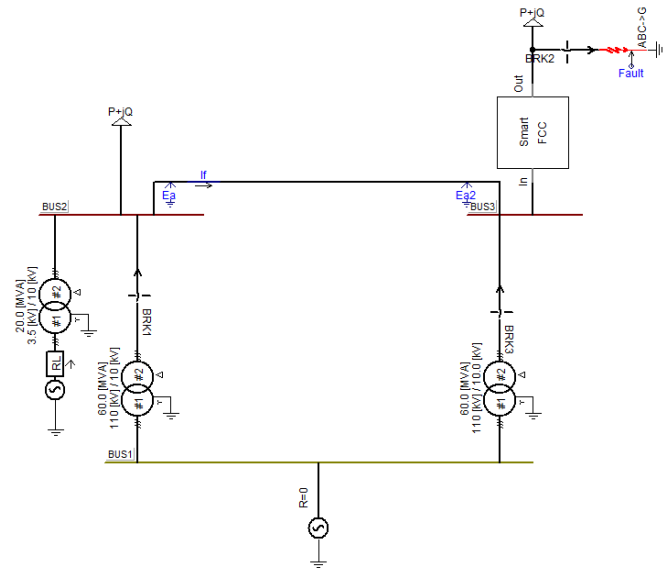


Fig. 6. View of simulated load feeder location SFCC in presence of distributed generation.

Displays the circuit in which the SFCC is placed in feeder location.

As a result of the simulation in this condition the waveforms are achieved and demonstrated in Fig. 7. The peak of the current at the first half cycle when SFCC is not operating is about 44.3 kA and it naturally dips and remains stable at about 39 kA. In the case of using SFCC in load feeder location, it can achieve current alleviation to about 4.45 kA. Nonetheless, the first half peak is lightened to 41.5 kA by using the superconducting coil. Although the final limited current after using SFCC in section 3.3 and 3.4 were properly close to each other, in practice the superconducting coil which has to be used in the device that is placed in load feeder, must be designed more precisely and with decent amount of inductance to be able to withstand

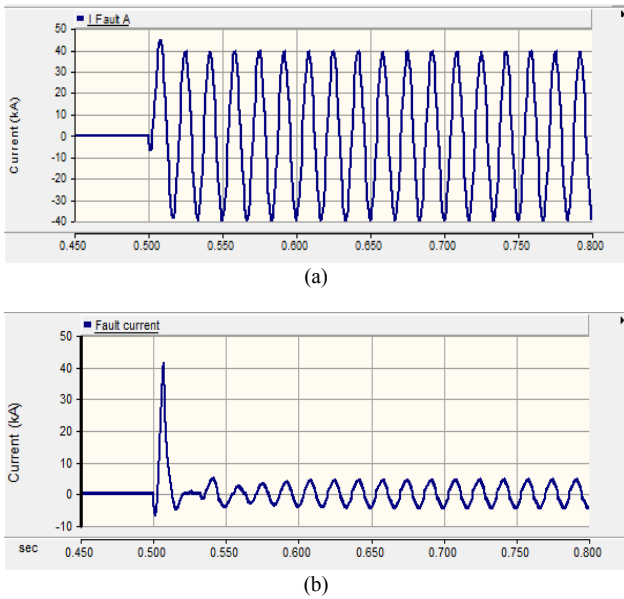


Fig. 7. Current wave form with DG when (a) SFCC is not present in load feeder location and (b) SFCC is present.

the higher fault currents. In consequence, in this position the cost of the SFCC is probably higher than that placed in Bus-tie location.

3.5. Main feeder location

Applying the SFCC to the main stream of electric current from the high voltage level gives the opportunity to limit the fault currents that occur beyond the distribution level. In this condition the SFCC only restrains total current of the upstream system and none from the DG unit. The schematic view of the circuit and the current waveforms are presented as follows.

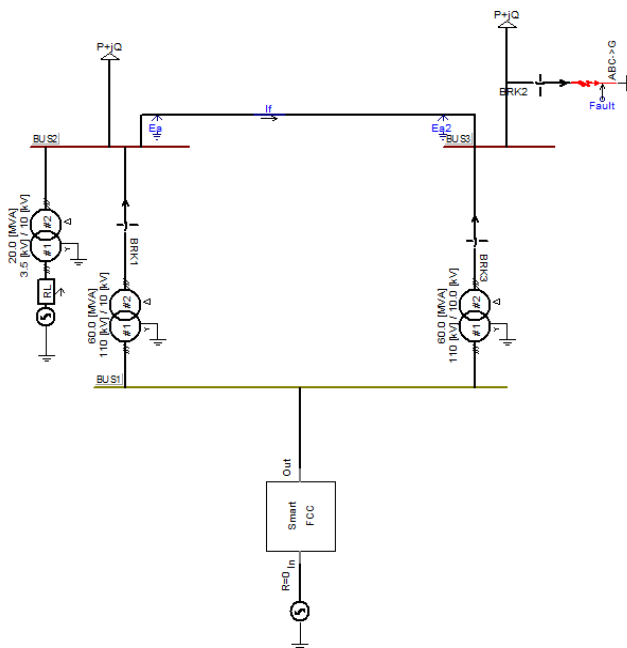


Fig. 8. view of simulated main feeder location SFCC in presence of distributed generation.

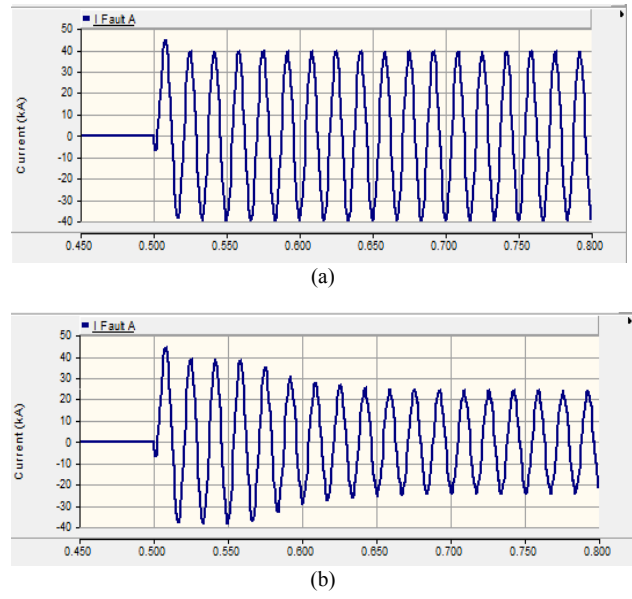


Fig. 9. Current wave form with DG when (a) SFCC is not present in main feeder location and (b) SFCC is present.

The fault current in this situation without SFCC rises to 44.3 kA in first half cycle. By using the Smart Fault Current Controller, it is declined to 24.04 kA. In Fig. 9. results show the improper location of using the SFCC when there is another source of power at distribution level beside main source. Due to the huge current injection from DG, strange behavior is seen up to four cycles; the waveform stays the same as case (a) for about 0.06 s then it is regulated to a level which is not desirable with the same characteristics of SFCC as in before cases.

4. CONCLUSION

Due to the restrictions of the software, the model for the SFCC has to be built in a unidirectional way, whereas in reality the full bridge thyristor rectifier is a bidirectional device; therefore, there should be more work done on the modeling area. The characteristics of the DG unit should be more in considerate for the simulations in future studies. However, based on this study, among three main locations at distribution level in power system, the Bus-tie location for SFCC is more convenient:

- 1- We can manage to limit the fault current more effectively than other locations, with less effort and cheaper structure in designing the superconducting coil.
- 2- In order to have legitimate mitigation of the fault current, the SFCC has to be installed in a way to oversee the total current of the distributed generation.

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