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Study of a SEPIC-input Self-driven Active Clamp ZVS Converter

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Abstract – This paper proposes a SEPIC-input, self-driven, active clamp ZVS converter, where an auxiliary winding and a RC delay circuit are employed to drive the active clamp switch and to achieve asymmetrical duty control without any other extra circuits. Based on the fixed dead time and the resonance between capacitors and inductors, both the main switch and the auxiliary switch can rule the ZVS operation. Detailed operation modes are presented to illustrate the self-driven and ZVS principles. Furthermore, an accurate state-space model and the transfer functions of the proposed converter have been presented and analyzed in order to optimize dynamic performance. The model provides efficient prediction of converter operations. Experimental results, based on a prototype with 80V input and 15V/20A output, are discussed to verify the transient and steady performance of the proposed converter.

Keywords: Self-driven, active clamp, small-signal model, ZVS converter

1. Introduction

The switching mode power supplies based on an active clamp transformer reset technique, offer high efficiency and reliable power-handing capability in numerous applications. The active clamp circuit can suppress voltage stress from power semiconductors, and absorb surge energy stored in the leakage inductance [1]-[3]. This technique also offers many other advantages including the ability to switch at zero voltage switching (ZVS), a wide range of input voltage and duty cycle operation beyond 50 percent [4], etc.

Its benefits have resulted into an overall improvement in performance. However, since the high-side active clamp switch is floating, an extra driver and isolated circuits are required [5]. This is troublesome as newer integrated circuits require power supplies in smaller packages and higher efficiency. Furthermore, to perform the ZVS operation of the converter, an asymmetrical duty control method with a fixed dead time should be applied. In general practice [6], it can be done by associating an extra controller with the main control loop, which is a little complex. On the other hand, the isolated SEPIC-input, active-clamp converter is one of the most attractive soft-switching converter topologies [8]-[9]. Although the converter has been presented in the past years, the detailed system model analysis has not been thoroughly discussed. In order to optimize dynamic performance, it is necessary to develop a valid small-signal model [10]-[18].

This paper proposes a SEPIC-input, self-driven, active clamp ZVS converter that utilizes a fixed-dead-time asymmetrical duty control mechanism. The converter uses only one auxiliary winding of the transformer to drive the active clamp switch. Moreover, the asymmetrical control can be easily operated in this self-driven circuit.

The objective of this paper is to present the working principles, modeling, analysis, and design of such converter and also to provide experimental results. These will be tackled in various sections of the paper. The operating principle and a detailed analysis of the converter are explained in Section II. Modeling and the method of analysis with the steady-state and small-signal model are presented in Section III. The obtained experimental results are featured in Section IV.

2. SYSTEM ANALYSIS

2.1 Circuit Description

The SEPIC-input, self-driven, active clamp forward-type converter is shown in Fig. 1. The main structure of the primary side is based on the SEPIC-input forward converter. It is made up of the input filter inductor Li, the main switch S1, the active clamp circuit, the transformer, and the self-driven circuit. The main structure of the secondary side is based on the transformer center-tapped rectifier. D1 and D2 denote the anti-parallel diodes across switches S1 and S2, respectively. Lr and Lm represent the leakage inductance

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and the magnetizing inductor of the transformer. Cr1 and Cr2 are the parasitic output capacitors of S1 and S2, respectively.

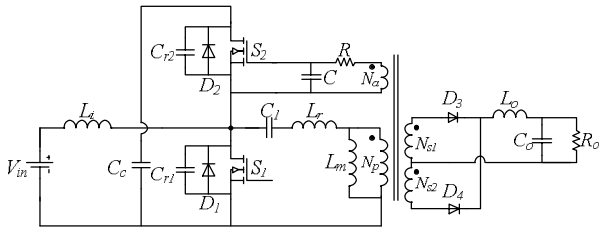


Fig. 1. Circuit of the SEPIC-input self-driven active clamp ZVS converter

The active clamp circuit, including the auxiliary switch S_2 and the clamp capacitor C_c, is used to absorb the surge energy from the leakage inductance, and reduce the voltage stress from the main switch S_1. The main switch S_1 achieves ZVS operation through the resonant capacitance C_{r1} and C_{r2}, the magnetizing inductance L_m, and the leakage inductance L_r. On the other hand, the resonance between C_c and L_r can facilitate ZVS operation for the active clamp switch S_2. N_p and N_a represent the winding number of the primary and auxiliary winding of the transformer, respectively. The proposed self-driven circuit, which consists of the coupled auxiliary winding and RC delay circuit, is used to drive S_2 and to generate fixed dead time, instead of extra driving circuits. The dead time is required to perform the ZVS operation of the switches S_1 and S_2 in this converter when they are both turned off.

2.2 The Operation Principles

In the system analysis, the following simplifying assumptions are used:

1) All switches and diodes used are ideal.

2) The capacitance C1 is large enough so that the voltage it is using is constant.

3) The output inductance filter is large enough that the output voltage and current are constant.

4) The parasitic output capacitors, Cr1 and Cr2, are small enough.

Based on the voltage-second product balance, the clamp capacitor voltage is given as

$$V_{Cc} = \frac{V_{in} D}{1 - D}. \tag{1}$$

There are 11 operation modes during one switching period in the proposed converter. The key waveforms of this converter are shown in Fig. 2, while the equivalent circuits for each mode are given in Fig. 3. The detailed analysis of this converter is explained below:

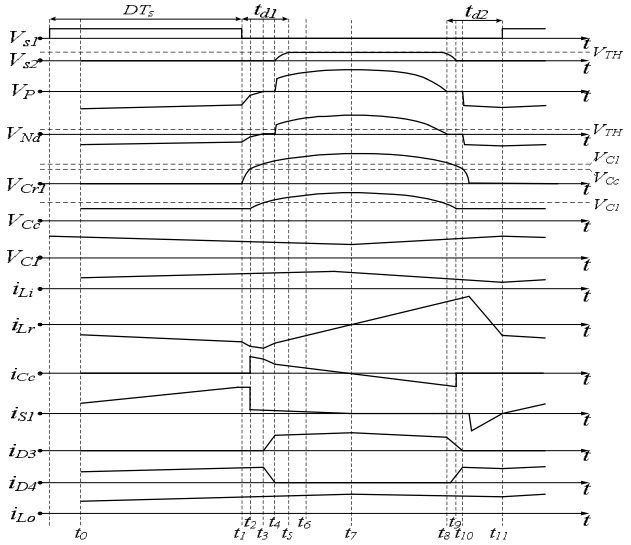
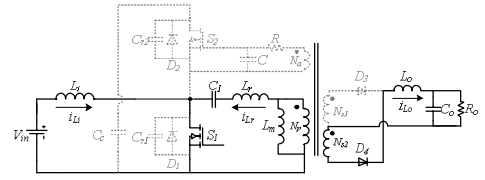
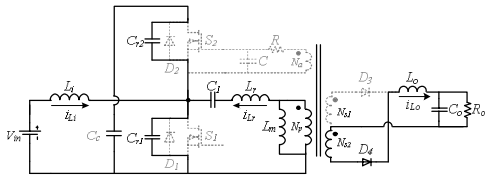


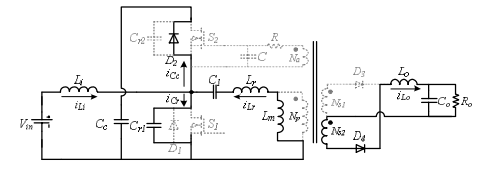
Fig. 2. Key waveforms of the self-driven active clamp forward converter



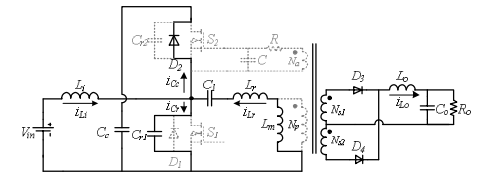
(a) Mode 1



(b) Mode 2

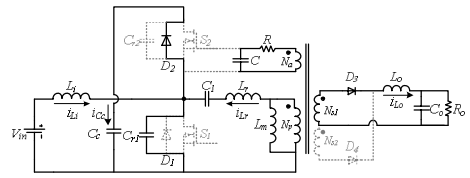


(c) Mode 3

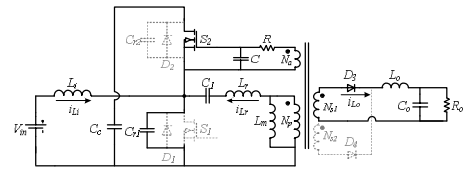


(d) Mode 4

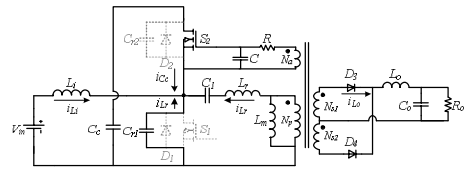
Fig. 3. The equivalent circuits of the 11 modes of the proposed converter



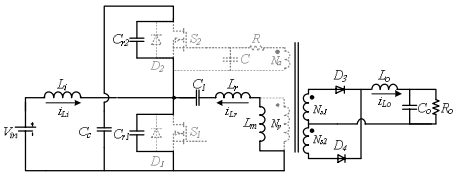
(e) Mode 5



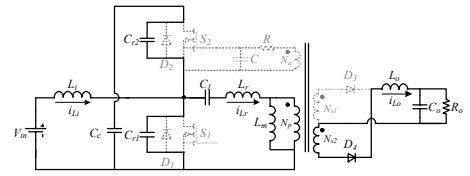
(f) Mode 6



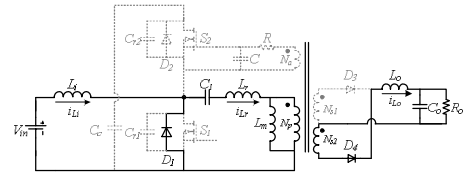
(g) Mode 7



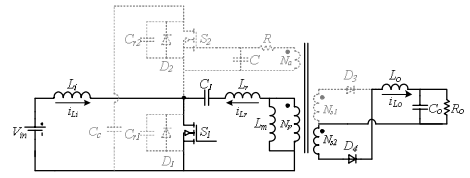
(h) Mode 8



(i) Mode 9



(j) Mode 10



(k) Mode 11

Fig. 3. The equivalent circuits of the 11 modes of the proposed converter (Continued)

Mode 1 ($t_0 \le t < t_1$): This mode begins at t_0 when the main switch S_1 is on. During this mode, the parasitic output capacitance voltage is V_{cr}=0. The input power is delivered to the input inductor L_i, which causes the inductance current i_{Li} to increase linearly. The magnetizing current i_{Lr} is linearly increasing as the capacitance voltage v_{c1} is applied to the output inductor L_o through the transformer. The primary winding voltage is $-V_{c1}$ so that the self-driven auxiliary winding voltage is $-N_a V_{c1}/N_p$ and the clamp switch S_2 is off. The output inductor current $i_{Lo}(t)$ flows through the diode D_4 while D_3 is turned off.

The input inductance current $i_{Li}(t)$,output inductance current $i_{Lo}(t)$ and the magnetizing current $i_{Lr}(t)$ are given as:

$$\begin{cases} i_{L_i}(t) = I_{L_i}(t_0) + \dfrac{V_{in}}{L_i}(t - t_0) \\ i_{L_o}(t) = N i_{Lr}(t) \\ i_{Lr}(t) = i_{C1}(t) = I_{Lr}(t_0) + \dfrac{V_{C1}(t)}{L_r}(t - t_0) \end{cases} \tag{2}$$

where $N=N_p/N_{s1}=N_p/N_{s2}$ is the winding ratio of the transformer.

This mode ends at $t=t_1$ when the main switch S_1 is turned off. *Mode 2* ($t_1 \le t < t_2$): At time $t=t_1$, the main switch S_1 is turned off. Since its parasitic output capacitor voltage V_{Cr} is zero, S_1 is operated by zero voltage turn-off. In this interval, i_{Lr} charges capacitor C_{r1} and discharges capacitor C_{r2} by resonating. The resonant circuit is composed of the resonant capacitors C_{r1} and C_{r2}, the leakage inductor L_r, and the magnetizing inductor L_m. Since C_{r1} and C_{r2} are very small, the transition interval is very short. Therefore, the charging operation of C_{r1} and the discharging operation of C_{r2} are processed quickly. The magnetizing current i_{Lr} tends to rise and V_{Cr2} decreases to zero quickly. The equations of the resonant capacitor voltage and inductor current are expressed as:

$$\begin{cases} V_{Cr}(t) \approx \dfrac{i_{Lr}(t_1)}{C_r}(t - t_1) \\ i_{Lr}(t) = i_{Lr}(t_1) + \dfrac{V_{C1}(t)}{L_r + L_m}(t - t_1). \end{cases} \tag{3}$$

Since the clamp voltages V_{Cc} varies according to different duty cycles, we can assume $V_{Cc}(t_2) > v_{C1}(t_2)$. This mode ends when the resonant capacitance voltage V_{Cr1} is equal the clamp voltage V_{C1} at t_2.

Mode 3 ($t_2 \le t < t_3$): This mode begins at time t_2 when $V_{Cr1}=V_{C1}$. Therefore, the primary side voltage V_P decreases to 0 while the secondary side diodes are both turned on. The rectifier is short-circuited, so the magnetizing current is

absorbed by the output stage. The diode current i_{D3} increases to output current while the diode current i_{D4} decreases to zero. Due to the resonance between C_{r1} and L_r, i_{Lr} increases to maximum. During this mode, the input power is delivered to L_i continually, while V_{c1} is still applied to L_o. The output voltage and the output inductance voltage $v_{Lo}(t)$ are given as:

$$\begin{cases} v_o(t) = \dfrac{1}{C_o}\int_{t_0}^{t_1} i_{C_o}(t)dt \\ v_{L_o}(t) = L_o \dfrac{di_{L_o}(t)}{dt} = -v_o(t) + \dfrac{V_{C1}(t)}{N}. \end{cases} \tag{4}$$

This mode ends when D_3 is turned on and D_4 is turned off.

Mode 4 ($t_3 \le t < t_4$): When $V_{Cr1}=V_{C1}=V_{Cc}$ at t_3, the anti-parallel diode across clamp switch S_2 is reversed as biased and conducted current. At the same time, a resonance with C_{r1}, C_c, L_r and L_m takes place. Therefore, the clamp capacitor C_c and the resonant capacitor C_{r1} are charged by i_{Lr}. Since the clamp capacitance C_c is much larger than C_{r1}, the resonance tends to be slower. The clamp capacitance voltage $V_{Cc}(t)$ and the output capacitance current $i_{Co}(t)$ are obtained by:

$$\begin{cases} V_{Cc}(t) = V_{Cc}(t_3)\cos\left(\dfrac{t-t_3}{\sqrt{L_r C_q}}\right) + i_{Lr}(t_3)\sqrt{\dfrac{L_r}{C_q}}\sin\left(\dfrac{t-t_3}{\sqrt{L_r C_q}}\right) \\ i_{C_0}(t) = i_{Lo}(t) - \dfrac{v_o(t)}{R} \end{cases} \tag{5}$$

where $C_q=C_{r1}+C_c$.

This mode ends when the resonant capacitance voltage V_{Cr1} reaches V_{c1}.

Mode 5 ($t_4 \le t < t_5$): At the end of mode 4, the rectifier diode D_4 is blocked, and D_3 is turned on. The voltage applied to the primary of the transformer reverses polarity, and tends to rise quickly. So is the self-driven auxiliary winding voltage V_{Na}. Because of the *RC* delay circuit, the gate-to-source voltage of S_2, $V_{S2,gs}$, increases slowly. In the delay interval, the capacitance voltage V_{Cr1} increases by resonating among C_{r1}, C_c, L_r and L_m, decreasing the resonant current i_{Lr}.

The energy stored in C_1 is transferred to supply the output power and to excite output inductor L_o. The output inductance current is given as:

$$i_{L_o}(t) = N i_{Lr}(t_4) + \frac{V_{C1}(t)N}{L_r}(t-t_4). \tag{6}$$

This mode ends when the delay interval ends and S_2 is turned on at ZVS.

Mode 6 ($t_5 \le t < t_6$): This mode begins when S_2 is turned on at ZVS by the self-driven circuit at time t_5. During this mode, the resonant circuit consistes of C_{r1}, C_c, L_r and L_m. Since the resonance, the magnetizing current i_{Lr} is decreased while the capacitance C_c and C_{r1} are charged. The primary voltage V_P and the self-driven auxiliary winding voltage V_{Na} are increased. On the other hand, the capacitance voltage V_{C1} is applied to the output inductor via the transformer, which causes i_{Lo} to increases.

The resonant capacitor voltage and magnetizing current are expressed as:

$$\begin{cases} V_{Cc}(t) = V_{Cc}(t)\cos(\dfrac{t-t_3}{\sqrt{L_q C_q}}) + i_{Lr}(t_3)\sqrt{\dfrac{L_q}{C_q}}\sin(\dfrac{t-t_3}{\sqrt{L_q C_q}}) \\ i_{Lr}(t) = i_{Lr}(t_3)\cos(\dfrac{t-t_3}{\sqrt{L_q C_q}}) - V_{Ccq}\sqrt{\dfrac{C_q}{L_q}}\sin(\dfrac{t-t_3}{\sqrt{L_q C_q}}) \end{cases} \tag{7}$$

where $L_q=L_r+L_m$.

This mode ends when the magnetizing current i_{Lr} equals 0 at time t_6.

Mode 7 ($t_6 \le t < t_7$): At time t_6 when $i_{Lr}=0$, the voltages V_{Cc} and V_{Cr1} are increased to resonant peak voltage. During this mode, the resonant circuit is composed of C_c, C_{r1}, L_r and L_m. The magnetizing current i_{Lr} changes its direction and is increased by resonance while the capacitance voltages V_{Cc} and V_{Cr1} are discharged. Therefore, the primary side voltage V_P is decreased. On the other hand, power stored in L_i is released to the capacitor C_1, by which L_i is reset. The output capacitance C_o is charged by L_o, and L_o is reset by the output power.

The primary side voltage and the output inductor current are given as:

$$\begin{cases} V_P(t) = V_{C1}(t) - V_{Cc}(t)\cos(\dfrac{t-t_4}{\sqrt{L_q C_q}}) \\ \qquad\qquad - i_{Lr}(t_4)\sqrt{\dfrac{L_q}{C_q}}\sin(\dfrac{t-t_4}{\sqrt{L_q C_q}}) \\ i_{L0}(t) = N\left(i_{Lr}(t) - \dfrac{C_q V_{C1}(t)}{L_q C_q + 1}(t-t_4)\right). \end{cases} \tag{8}$$

This mode ends when $V_{Cr1}=V_{Cc}$ are decreased to V_{C1} at time $t=t_7$.

Mode 8 ($t_7 \le t < t_8$): This mode begins when capacitance voltages V_{Cr1} and V_{Cc} are discharged to V_{C1}. Therefore, the primary voltage V_p and the auxiliary self-driven winding voltage V_{Na} are equal to 0 at time t_7. The rectifier is short-circuited. The secondary side diodes are both on, and the diode current i_{D3} is decreased from output inductance

current to 0 while the diode current i_{D4} is increased from 0 to output inductance current. In this interval, the resonant circuit is consisted of C_{r1}, C_c and L_r. As the *RC* delay circuit, the driving voltage of S_2 is decreased to the threshold voltage, turning off S_2, and ending this mode.

This interval is very critical for S_1 to achieve ZVS. The time interval can be expressed as:

$$\Delta t = \frac{\sqrt{L_q C_q}}{2}. \tag{9}$$

During this mode, the output inductance voltage $v_{Lo}(t)$ and input inductance voltage $v_{Li}(t)$ are:

$$\begin{cases} v_{L_i}(t) = v_{in}(t) - v_{C_1}(t) \\ v_{L_o}(t) = -v_o(t) - \dfrac{v_{C_c}(t)}{N} + \dfrac{v_{C_1}(t)}{N}. \end{cases} \tag{10}$$

Mode 9 ($t_8 \leq t < t_9$): At time t_8, the parasitic output capacitance voltage of S_2 is zero, and S_2 is operated by zero voltage turn-off. The capacitance current i_{Cc} is zero, and the resonant circuit is reduced to C_{r1} and L_r. This mode ends when diode current i_{D3} reaches to zero, and i_{D4} is equal the output inductance current.

Mode 10 ($t_9 \leq t < t_{10}$): This mode begins when the primary side voltage V_p reverses its polarity and begins to increase. The resonant capacitance voltage V_{cr1} decreases quickly by resonating among C_{r1}, L_r and L_m. In this mode, C_1 is charged by the input power and L_i. The power stored in the output inductor L_o is released to charge C_o and to supply output.

This mode ends when V_{cr1} reaches 0.

Mode 11 ($t_{10} \leq t < t_{11}$): When V_{cr1} reaches zero, the anti-parallel diode of the main switch S_1 is turned on. Therefore, the primary voltage V_p is increased, while i_{Lr} reverses its polarity and begins to increase. During this mode, the input power is delivered to inductor L_i while the capacitance voltage $V_{c1}(t)$ is applied to the output inductor L_o via diode D_4. This state ends when the main switch S_1 is turned on at ZVS.

2.3 The Key Issues to ZVS and the Self-driven Active Clamp

The key features of the proposed converter are the self-driven active clamp switch and the ZVS operation for both t he main and the auxiliary switches.

To ensure smooth ZVS operation of switch S_2 at mode 5, the condition of $t_{d1} > t_{m2}+t_{m3}+t_{m4}$ must be satisfied, where t_{d1} is the dead time on the positive-going-edge of V_{gs2}, and t_{m2}~t_{m5} represent the time intervals of mode 2~ mode 4, respectively. Therefore, before S_2 is turned on, the anti-parallel body diode D_2 of S_2 should be on by the resonance between C_{r1}, C_{r2}, L_r, and L_m. Since C_{r1}, C_{r2}, and L_r are so small, the resonance time between them can be neglected. For convenience, we can use the following approximate equation to estimate t_{d1}:

$$t_{d1} > \sqrt{L_q C_r}\,\sin^{-1}\left(\frac{-V_{Cc}}{i_{Lr}(t_4)}\sqrt{\frac{C_r}{L_q}}\right) \tag{11}$$

where $C_r = C_{r1} + C_{r2}$.

To ensure ZVS operation of switch S_1 at mode 11, V_{Cr1} sh ould be zero and S_2 should be turned off before S_1 is turned on. Therefore, the resonance time t_r of L_r, L_m, C_{r1}, and C_c sh ould be satisfied as

$$t_r = \sqrt{L_q C_q}\left(\pi - \sin^{-1}\left(\frac{-V_{Cc}}{i_{Lr}(t_2)}\sqrt{\frac{L_q}{C_q}}\right)\right) < (1-D)T_s - 2t_{d1}, \tag{12}$$

in which D is the duty cycle of S_1, and T_s is the switching pe riod. For convenience, we can calculate t_r as:

$$t_r = \pi\sqrt{L_q C_q} < (1-D)T_s - 2t_{d1}. \tag{13}$$

On the other hand, from Fig. 2, the positive-going-edge of V_{gs2} is expressed by

$$v_{gs2}(t) = \frac{N_a}{N_1}\left(v_{Cc}(t_7) - \frac{V_{in}}{1-D}e^{-\frac{t}{RC_{eq}}}\right) \tag{14}$$

where $C_{eq} = C_{iss} + C$, and C_{iss} is the input capacitance of S_2.

The auxiliary winding number N_a, which becomes the ke y parameter of S_2 to be self-driven, is determined from (1) , (11) and (14) as follows:

$$N_a = \frac{(1-D)N_1 V_{tn}}{DV_{in} - V_{in}e^{-\frac{t_{d1}}{RC_{eq}}}}. \tag{15}$$

3. Model Derivation

In this section, the state-space average modeling technique is applied to the proposed converter to develop small-signal and steady-state characteristics. The small-signal model of the converter is derived by performing the averaging process on the converter's steady-state waveforms.

3.1 Decomposition and Averaging

In order to optimize the dynamic performance of the proposed converter it is necessary to develop a valid small-signal model. We start by modeling the physical behavior of the proposed converter in Continuous Conduction Mode (CCM), and derive state-space equations for each mode of operation [19]-[24]. The dead times are neglected in this analysis for the sake of simplicity, because they are very short as compared to the other two main intervals in the switching cycle.

The following assumptions are made in regards to the proposed circuit:

1) The AC variations are much smaller in magnitude compared to the DC quiescent values.

2) The open loop crossover frequency of the converter is much smaller than the switching frequency.

3) The frequencies of variations of the converter inputs are much smaller than the switching frequency.

The circuit topology of the converter is shown in Fig. 4. Using normalized quantities, R_o denotes the output load. The resistance r_{Co} is the equivalent series resistance (ESR) of the output capacitor, while r_i and r_o are the internal resistance of the input inductor L_i and output inductor L_o, respectively. Note that although their values are very small, these resistors cannot be neglected in the modeling process as they are very critical to the cutoff frequency accuracy of the output low-pass filter.

The duty cycle D is defined by $D=t_{on}/T_s$, where t_{on} represents the interval within the switching period during which the S_1 is in conduction.

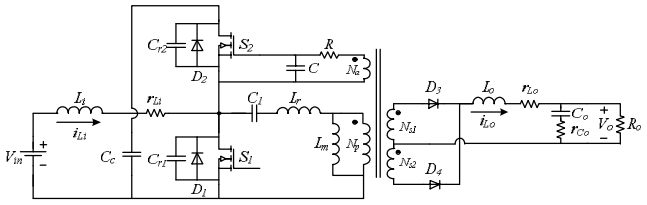


Fig. 4. Circuit of the SEPIC-input self-driven active clamp converter considering the parasitic resistances

3.2 State-Space Description

Since the proposed self-driven active clamp converter contains two inductors, L_i, and L_o, and three capacitors, C_c, C_1 and C_o, the state vector **x**(t) should comprise of the independent inductor currents $i_{Li}(t)$ and $i_{Lo}(t)$, as well as the capacitor voltages $v_{Cc}(t)$, $v_{C1}(t)$, and $v_{Co}(t)$. So, we can define the state vector as:

$$\mathbf{x}(t) = \left[i_{Li}(t) \;\; i_{Lo}(t) \;\; v_{Co}(t) \;\; v_{Cc}(t) \;\; v_{C1}(t) \right]^T . \tag{16}$$

As there are no coupled inductors, the matrix **K** is diagonal, and simply contains the values of capacitance and inductance.

$$\mathbf{K} = diag \left[L_i \;\; L_o \;\; C_o \;\; C_c \;\; C_1 \right]. \tag{17}$$

The input voltage v_{in} is typically assigned as the input vector **u**(t), and the output voltage v_o as the output vector **y**(t).

$$\mathbf{u}(t) = \left[v_{in}(t) \right] \tag{18}$$

$$\mathbf{y}(t) = \left[v_o(t) \right]. \tag{19}$$

During a switching cycle, the converter changes its state and corresponding equivalent circuit every time one of the switches or diodes commences conduction, or ceases to conduct current. Due to the operating action of the switches, S_1 and S_2, the converter will exhibit two different equivalent circuits in one switching period. The first state exists when S_1 is on and S_2 is off for a time interval DT_s and is shown in Fig. 5(a). The second state, as shown in Fig. 5(b), is obtained when S_1 is off and S_2 is on for a time interval $(1-D)T_s$.

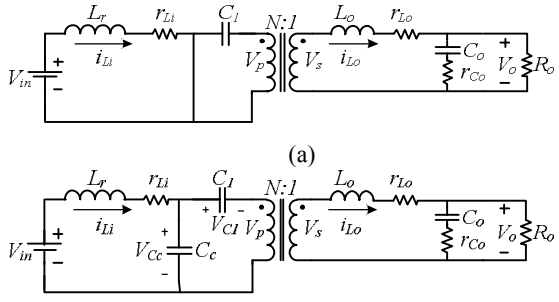


Fig. 5. Equivalent circuits of the proposed converter: (a) during state 1, (b) during state 2

To derive the state-space equations, from the operating principles analysis in Section II, rewrite the inductor voltages and capacitor currents as linear combinations of the elements of **x**(t) and **u**(t), as follows:

$$\begin{cases} i_{C_0}(t) = \dfrac{i_{Lo}R}{R + r_{C_0}} - \dfrac{v_{C_0}(t)}{R + r_{C_0}} \\ i_{C_1}(t) = \dfrac{-i_{Lo}}{N} \\ v_{L_i}(t) = v_{in}(t) - i_{Li}(t) r_i \\ v_{L_o}(t) = -v_o(t) - i_{Lo}(t) r_o + \dfrac{v_{C_1}(t)}{N}. \end{cases} \tag{20}$$

It is also necessary to express **y**(t) as linear combinations

of the elements of **x**(t) and **u**(t). The output circuit is driven by two independent signals $v_{Co}(t)$ and $i_{Lo}(t)$. Thus, $v_o(t)$ can be computed by superposition.

$$v_o(t) = i_{Lo}(r_{Co} \| R) + \frac{v_{Co}(t)R}{R + r_{Co}}. \tag{21}$$

Equations(20), and (21) are the description of the state (a). These equations can be derived in the following state-space form:

$$\begin{cases} \mathbf{K}\dfrac{d\mathbf{x}(t)}{dt} = \mathbf{A_1}\mathbf{x}(t) + \mathbf{B_1}\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C_1}\mathbf{x}(t) \end{cases} \tag{22}$$

where the respective matrices are

$$\begin{cases} \mathbf{A_1} = \begin{bmatrix} -r_i & 0 & 0 & 0 & 0 \\ 0 & -\left(\dfrac{Rr_{Co}}{R+r_{Co}} + r_q\right) & -\dfrac{R}{R+r_{Co}} & \dfrac{1}{N} & 0 \\ 0 & \dfrac{R}{R+r_{Co}} & -\dfrac{1}{R+r_{Co}} & 0 & 0 \\ 0 & -\dfrac{1}{N} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \\ \mathbf{B_1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}^T \\ \mathbf{C_1} = \begin{bmatrix} 0 & \dfrac{Rr_{Co}}{R+r_{Co}} & \dfrac{R}{R+r_{Co}} & 0 & 0 \end{bmatrix} \end{cases} \tag{23}$$

and

$$r_q = \left(\frac{Rr_{Co}}{R+r_{Co}}\right) + r_{Lo}. \tag{24}$$

Similarly, in the State II when S_1 is off and S_2 is on, the in ductance voltages, capacitance currents, and converter outp ut voltage are given by:

$$\begin{cases} v_{L_i}(t) = v_{in}(t) - i_{Li}(t)r_i - v_{C_1}(t) \\ v_{L_o}(t) = -v_o(t) - i_{Lo}(t)r_q - \dfrac{v_{C_c}(t)}{N} + \dfrac{v_{C_1}(t)}{N} \\ i_{C_o}(t) = \dfrac{i_{Lo}R}{R+r_{C_o}} - \dfrac{v_{C_o}(t)}{R+r_{C_o}} \\ i_{C_c}(t) = \dfrac{i_{Lo}}{N} \\ i_{C_1}(t) = i_{Li}(t) - \dfrac{i_{Lo}}{N} \\ v_o(t) = i_{Lo}(r_{Co} \| R) + \dfrac{R}{R+r_{Co}} v_{Co}(t). \end{cases} \tag{25}$$

The state equations can be written as follows in state-space form

$$\begin{cases} \mathbf{K}\dfrac{d\mathbf{x}(t)}{dt} = \mathbf{A}_2\mathbf{x}(t) + \mathbf{B}_2\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}_2\mathbf{x}(t) \end{cases} \tag{26}$$

where

$$\begin{cases} \mathbf{A}_2 = \begin{bmatrix} -r_i & 0 & 0 & 0 & -1 \\ 0 & -\left(\dfrac{Rr_{Co}}{R+r_{Co}} + r_q\right) & -\dfrac{R}{R+r_{Co}} & -\dfrac{1}{N} & \dfrac{1}{N} \\ 0 & \dfrac{R}{R+r_{Co}} & -\dfrac{1}{R+r_{Co}} & 0 & 0 \\ 0 & \dfrac{1}{N} & 0 & 0 & 0 \\ 1 & -\dfrac{1}{N} & 0 & 0 & 0 \end{bmatrix} \\ \mathbf{B}_2 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}^T \\ \mathbf{C}_2 = \begin{bmatrix} 0 & \dfrac{Rr_{Co}}{R+r_{Co}} & \dfrac{R}{R+r_{Co}} & 0 & 0 \end{bmatrix}. \end{cases} \tag{27}$$

3.3 Steady-State Model and Small-Signal Model

Suppose that the converter is driven at a steady-state that is a quiescent operating point (*I, V*) and with quiescent input voltage $v_{in}(t)=V_{in}$ as well as duty ratio $d(t)=D$. During one switching period, by inserting disturbances at the input voltage and duty-cycle, the total averaged quantities of the converter can be expressed as the sums of the DC and AC components.

$$\begin{cases} i_i(t) = I_i + \hat{i}_i(t) \\ v_{in}(t) = V_{in} + \hat{v}_{in}(t) \\ i_o(t) = I_o + \hat{v}_o(t) \\ v_o(t) = V_o + \hat{v}_o(t) \\ d(t) = D + \hat{d}(t). \end{cases} \tag{28}$$

By applying the averaging technique, the perturbation yields the steady-state and linear small-signal state-space equations:

$$\begin{cases} \mathbf{0} = \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} = \mathbf{CX} + \mathbf{EU} \end{cases} \tag{29}$$

$$\begin{cases} \mathbf{K}\dfrac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \left[(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})\mathbf{U}\right]\hat{d}(t) \\ \hat{\mathbf{y}}(t) = \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \left[(\mathbf{C_1} - \mathbf{C_2})\mathbf{X} + (\mathbf{E_1} - \mathbf{E_2})\mathbf{U}\right]\hat{d}(t) \end{cases} \tag{30}$$

where **X, U** are the steady-state values and **x**, **u**, $\hat{d}(t)$ are the small-signal perturbations of the state, the averaged matrices are:

$$\begin{cases} \mathbf{A} = D\mathbf{A_1} + D'\mathbf{A_2} \\ \quad = \begin{bmatrix} -r_i & 0 & 0 & 0 & -D' \\ 0 & -\left(\dfrac{Rr_{Co}}{R+r_{Co}} + r_q\right) & -\dfrac{R}{R+r_{Co}} & \dfrac{D-D'}{N} & \dfrac{D'}{N} \\ 0 & \dfrac{R}{R+r_{Co}} & -\dfrac{1}{R+r_{Co}} & 0 & 0 \\ 0 & -\dfrac{D-D'}{N} & 0 & 0 & 0 \\ D' & -\dfrac{D'}{N} & 0 & 0 & 0 \end{bmatrix} \\ \mathbf{B} = D\mathbf{B_1} + D'\mathbf{B_2} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}^T \\ \mathbf{C} = D\mathbf{C_1} + D'\mathbf{C_2} = \begin{bmatrix} 0 & \dfrac{Rr_{Co}}{R+r_{Co}} & \dfrac{R}{R+r_{Co}} & 0 & 0 \end{bmatrix} \end{cases} \tag{31}$$

and

$$D' = 1 - D\,. \tag{32}$$

The vector coefficients of $\hat{d}(t)$ in (30) are:

$$\begin{cases} (\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})\mathbf{U} = \begin{bmatrix} V_{C1} \\ \dfrac{2V_{Cc} - V_{C1}}{N} \\ 0 \\ -\dfrac{2I_{Lo}}{N} \\ -I_{Li} + \dfrac{I_{Lo}}{N} \end{bmatrix} \\ (\mathbf{C_1} - \mathbf{C_2})\mathbf{X} + (\mathbf{E_1} - \mathbf{E_2})\mathbf{U} = \mathbf{0}\,. \end{cases} \tag{33}$$

From the steady-state equations, the DC input-to-output voltage transfer function can be expressed as:

$$G_{VDC} \equiv \frac{V_o}{V_{in}} = \frac{2NRD}{N^2\left(R + r_{Lo}\right) + 2Dr_{Li}}\,. \tag{34}$$

If r_{Li} and r_{Lo} are assumed to be zero, the conversion ratio of the converter will become:

$$\frac{V_o}{V_{in}} \approx \frac{2D}{N}\,. \tag{35}$$

3.4 Transfer Functions

Given the small-signal equations, the control-to-output transfer function $G_{vd}(s)$ is found by applying the Laplace transform:

where

$$\begin{aligned} G_{vd}(s) &\equiv \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{v_{in}(s)=0} = \mathbf{C(sI - A)^{-1}B + D} \\ &= \frac{a_{d0}s^4 + a_{d1}s^3 + a_{d2}s^2 + a_{d3}s + a_{d4}}{b_0 s^5 + b_1 s^4 + b_2 s^3 + b_3 s^2 + b_4 s + b_5} \end{aligned} \tag{36}$$

where

$$\begin{cases} a_{d0} = NL_iRC_oC_1C_c(2V_{C_1} - V_{Cc}) \\ a_{d1} = NC_1C_c[2L_iC_o(1-2D)V_o + RC_or_{Li}r_{Co}(2V_{C_1} - V_{Cc}) \\ \qquad + L_iR(2V_{C1} - V_{Cc})] \\ a_{d2} = C_o[NRC_1D'^2(1 + r_{Co}(2V_{C_1} - V_{Cc})) \\ \qquad + 2C_cr_{Li}r_{Co}V_o(1-2D)] \\ a_{d3} = NRC_1D'^2(1 + (2V_{C_1} - V_{Cc})) \\ \qquad + 2V_o(1-2D)(C_or_{Co}D'^2 + C_crL_i) \\ a_{d4} = 2D'^2V_o(1-2D) \end{cases} \tag{37}$$

and

$$\begin{cases} b_0 = N^2L_iL_oC_oC_1C_c(R + r_{Co}) \\ b_1 = N^2C_1C_o\left[L_iL_o + C_c(R + r_{Co})(L_ir_q + L_or_{Li})\right] \\ b_2 = C_oC_c(R + r_{Co})\left(Li(1-2D)^2 + N^2C_1r_{Li}r_q\right) + N^2C_1 \\ \quad \left[L_oC_oD'^2(R + r_{Co}) + C_c(L_ir_q + L_or_{Li}) + \dfrac{L_iC_oR^2}{(R + r_{Co})}\right] \\ b_3 = N^2C_o(R + r_{Co})\left(C_cr_{Li}(1-2D)^2 + C_1r_qD'^2\right) + C_cL_i \\ \quad (1-2D)^2 + N^2C_1\left[C_cr_{Li}r_q + L_oD'^2 + \dfrac{R^2C_oC_c}{(R + r_{Co})}\right] \\ b_4 = (1-2D)^2\left(C_o(R + r_{Co}) + C_cr_{Li}\right) + N^2RC_1D'^2 \\ \quad \left(\dfrac{r_{Lo}}{R} + \dfrac{R}{R + r_{Co}}\right) \\ b_5 = D'^2V_o(1-2D)\,. \end{cases} \tag{38}$$

The input-to-output voltage transfer function is found by setting duty cycle variations $\hat{d}(s)$ to zero:

$$\begin{aligned} G_{vg}(s) &\equiv \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} = \mathbf{C(sI - B)^{-1}A} \\ &= \frac{a_{i0}s^4 + a_{i1}s^3 + a_{i2}s^2 + a_{i3}s + a_{i4}}{b_0 s^5 + b_1 s^4 + b_2 s^3 + b_3 s^2 + b_4 s + b_5} \end{aligned} \tag{39}$$

where

$$\begin{cases} a_{i0} = a_{i1} = a_{i3} = 0 \\ a_{i2} = NRD'^2C_1r_{Co}C_o \\ a_{i4} = NRD'^2C_1\,. \end{cases} \tag{40}$$

3.5 Simulation Results

In the circuit shown in Fig. 1, the following parameters in Table 1 are assigned to simulation.

Table 1. Simulation parameters

Parameter	Value
Input voltage V_{in}	80V
Output voltage V_o	15V

Input inductor L_i	220uH
Output inductor L_o	21uH
Output capacitor C_o	1880uF
Capacitor C_1	2640uF
Clamp capacitor C_c	1uF
Internal resistance r_o	0.32 Ω
Internal resistance r_i	0.64 Ω
ESR r_{Co}	0.03 Ω
Load R_o	0.75Ω

Therefore, the input-to-output transfer function $G_{vg}(s)$ can be obtained by (39) and the coefficients are

$$\begin{cases} a_{i2} = 1.08\times10^{12} \\ a_{i4} = 1.91\times10^{16} \end{cases}, \begin{cases} b_0 = 1 \\ b_1 = 2.02\times10^{4} \\ b_2 = 2.42\times10^{9} \\ b_3 = 4.31\times10^{13} \\ b_4 = 8.28\times10^{16} \\ b_5 = 1.42\times10^{18} \end{cases} \tag{41}$$

Simulations are performed by using MATLAB software. Fig. 6 shows the bode magnitude and phase plots of $G_{vg}(s)$.

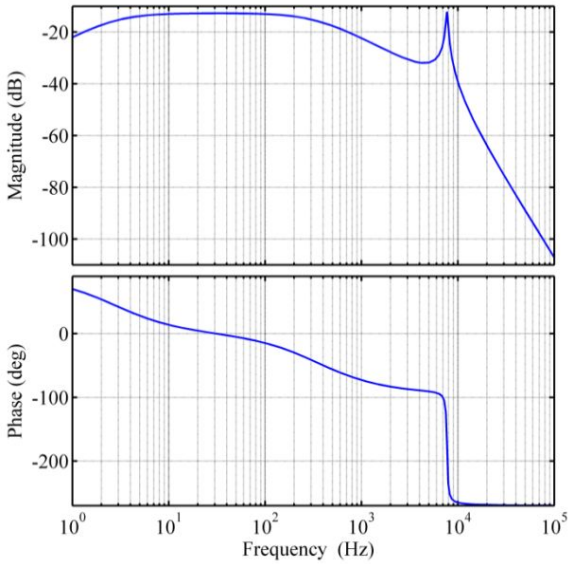


Fig. 6. Graphical construction of the input-to-output transfer function

At low frequency, the magnitude first increases, and then decreases as the frequency increases. The phase function begins at 90° and decreases up to -270° at high frequency. From the plots, we can also obtain the corner frequency occurring at 7.4 kHz, which is contributed by the filter of internal resistance r_i, r_o, the ESR r_{Co}, and the output capacitor C_o, as well as the resonance between the clamp capacitor C_c and the input inductor L_i.

Substituting the parameters to (36), yields the open loop control-to-output transfer function as (36) and the coefficients are:

$$\begin{cases} a_{d0} = 2.24\times10^{3} \\ a_{d1} = 4.66\times10^{8} \\ a_{d2} = 8.88\times10^{13} \\ a_{d3} = 9.59\times10^{17} \\ a_{d4} = 4.25\times10^{19} \end{cases}. \tag{42}$$

Fig. 7 shows the Bode diagram of the open loop control-to-output transfer function. We can get the phase margin of -44° at a crossover frequency of 8.45 kHz and the gain margin of -15 dB at 7.82 kHz. It is remarkable that this open loop converter is not stable. From the plot, we can also obtain that the peak formed by the output *RC* filter and the resonance between C_c and L_i, which is critical to the stability of the converter. In addition, resonant peaks caused by L_m, L_o, and C_o, C_1 which are in the low frequency range, are eliminated by the internal resistance r_i, r_o, and the ESR r_{Co}. Due to the right half-plane zero at 10.3 kHz contributed by r_{Co} and C_c, there is an inversion in phase characteristics and the transfer plot is approaching -20 dB/dec at high frequency.

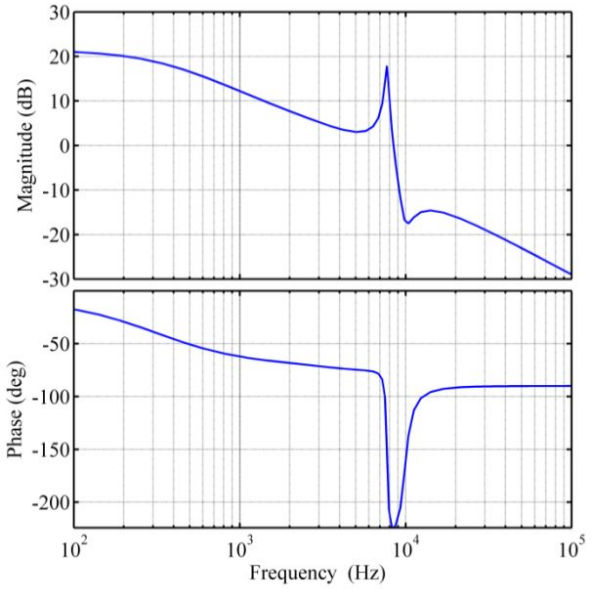


Fig. 7. Graphical construction of the control-to-output transfer function

3.6 Stability Analysis

To design a regulator system that meets design goals toward the rejection of disturbances, transient response, and stability, a 2-pole, 1-zero loop compensator circuit shown in Fig. 8 is considered. The compensator consists of isolated circuit, error amplifier, and a PWM comparator.

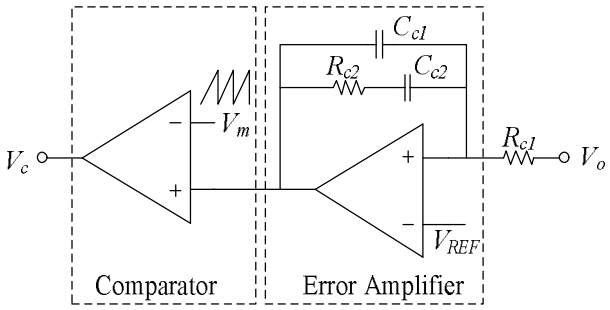


Fig. 8. A 2-pole and 1-zero compensator

The transfer function of the compensator $A(s)$ is:

$$A(s) = \frac{R_{c2}C_{c1}s + 1}{R_{c1}R_{c2}C_{c1}C_{c2}s^2 + R_{c1}(C_{c1} + C_{c3})s}. \tag{43}$$

Therefore, the loop gain of the proposed converter is:

$$T(s) \equiv A_c \frac{\hat{v}_o(s)}{\hat{d}(s)} \frac{A(s)}{V_m} \tag{44}$$

where A_c is the coefficient of the signal amplification, and V_m is the magnitude of the saw tooth wave in the comparator. In this paper, we designed the compensator parameters as R_{c1}=1.9kΩ, R_{c2}=2kΩ, C_{c1}=220uF, and C_{c2} =180uF.

From (36) and TABLE I, the loop gain of the converter $T(s)$ is expressed as:

$$T(s) = \frac{a_{t0}s^5 + a_{t1}s^4 + a_{t2}s^3 + a_{t3}s^2 + a_{t4}s^1 + a_{t5}}{b_{t0}s^7 + b_{t1}s^6 + b_{t2}s^5 + b_{t3}s^4 + b_{t4}s^3 + b_{t5}s^2 + b_{t6}s + b_{t7}} \tag{45}$$

where

$$\begin{cases} a_{t0} = 25.67 \\ a_{t1} = 5.92\times10^5 \\ a_{t2} = 1.03\times10^{11} \\ a_{t3} = 1.33\times10^{15} \\ a_{t4} = 2.54\times10^{18} \\ a_{t5} = 1.11\times10^{20}, \end{cases} \tag{46}$$

and

$$\begin{cases} b_0 = 4.51\times10^{-7} \\ b_1 = 0.01 \\ b_2 = 1138 \\ b_3 = 2.5\times10^7 \\ b_4 = 1.36\times10^{11} \\ b_5 = 1.89\times10^4 \\ b_6 = 3.23\times10^{15} \\ b_7 = 0. \end{cases} \tag{47}$$

The loop gain plot of the magnitude and the phase characteristics as functions of frequency f is shown in Fig. 9. It shows that the crossover frequency is 1.23 kHz with the phase margin 42.5°, and the gain margin is 13.2 dB at 7.38 kHz. The loop gain slope is -20 dB/dec at high frequency, and the phase shift is approaching -180°. It should be noted that the compensator provides the gain slope -20 dB/dec at the crossover frequency and a phase compensation at the middle frequency range, which are good for ripple rejection. From the diagram, we can also see that the loop gain function contains the same corner at 7.4 kHz. However, the high peak influence is highly damped by the compensator. Therefore, the compensator satisfies the performance required by the converter.

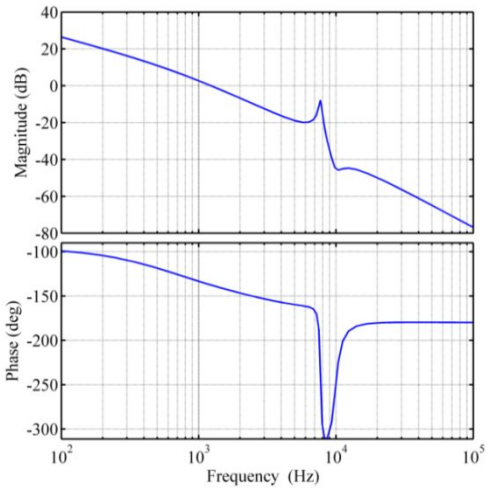


Fig. 9. Loop gain of the proposed converter

4. Experimental results

The proposed self-driven active clamp ZVS converter provides fewer components without degradation in performance. In order to verify the theoretical analysis of the proposed self-driven active clamp ZVS converter, a prototype converter has been built and tested. The prototype of the proposed converter is given in Fig. 10.

Fig. 10. Photograph of the prototype converter

Since the switching frequency of the prototype converter is 55kHz, that is the switching period is about 18us, the dead time t_{d1} and t_{d2} are chosen as 0.5us according to (11). So, in the RC delay circuit, R is chosen to be 8Ω while C is 47nF.

As illustrated in Section II, in this proposed converter, the transformer leakage inductance, magnetizing inductance and the clamp capacitance are very important as S_2 is turned off by the resonance in mode 8. The output voltage of this prototype is 15V and the input voltage is 80V, as discussed in (35), the transformer winding ratio is chosen as 4.5, and the duty cycle is 0.42. From (12) and (13), L_r, L_m and C_c are designed as 1.41uH, 168uH and 0.22uF, respectively.

Auxiliary winding number N_a can be calculated by (16) with the parameters given in TABLE II. As stated in (15), the calculated value of N_a is 1.9, and it is finally chosen 2 as an integer value.

The parameters and some specifications of the prototype converter are listed in Table 2.

Table 2. Parameters of the prototype

Parameter	Value
Input voltage V_{in}	80V
Output voltage V_o	15V
Rated power P	300W
Switching frequency f_s	55kHz
Input capacitor of switches C_{iss}	10.88nF
Output capacitor of switches C_{oss}	700pF
Delay resistor R	8Ω
Delay capacitor C	47nF
Switch S_1, S_2	IRFP4768PbF
Transformer ratio N	4.5

Fig. 11 provides the measured results of the gate voltage and the drain voltage of the main switch S_1 and auxiliary switch S_2 at the rated output power. It is shown that before the switches S_1 and S_2 are turned on, the drain voltages v_{ds1} and v_{ds2} are zero. Therefore, the ZVS operation is achieved for S_1 and S_2 as illustrated in Section II. From the figure, we can see that the measured peak-to-peak value of v_{ds2} is about 110V, which concurs with the theoretical result of 111.1V.

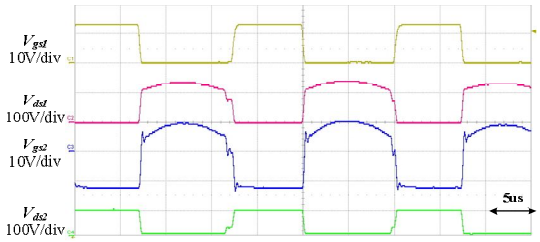


Fig. 11. Experimental waveforms of the gate and drain voltages of S_1 and S_2 with V_{in}=80V and V_o=15V

In Fig. 12, the primary voltage V_p, the auxiliary self-driven winding voltage V_{Na}, and the drain-to-source signal v_{ds2} are presented, which can illustrate the principle of the self-driven. It is clear that the waveform shapes of V_p and V_{Na} are the same. When the primary voltage is positive, the driving signal v_{ds2} decreases after the designed dead time and S_2 is turned on at ZVS. When V_{Na} is decreased to the threshold voltage by resonating, S_2 is turned off after a dead time.

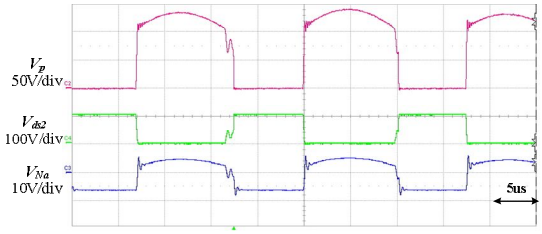


Fig. 12. Measured waveforms of V_p, V_{Na} and v_{gs2} with V_{in}=8 and V_o=15V

With the input voltage 80V and output voltage 15V, the two dead time durations, t_{d1} and t_{d2}, are shown in Fig. 13 and Fig. 14, respectively. Based on the waveforms, t_{d1} is measured as 0.45 us, while t_{d2} is 0.38 us, which are very close to the chosen values discussed above. Therefore, ZVS conditions can be achieved by resonating between inductors and capacitors during the dead times.

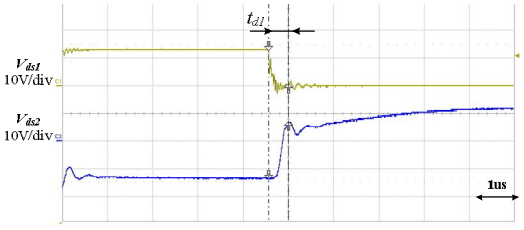


Fig. 13. Experimental waveforms comparing two drive signals to measure dead time t_{d1}

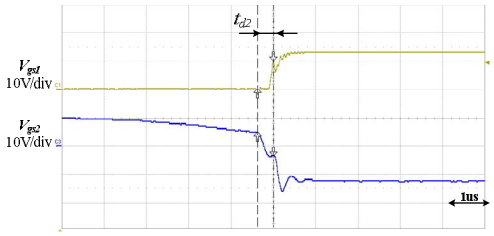
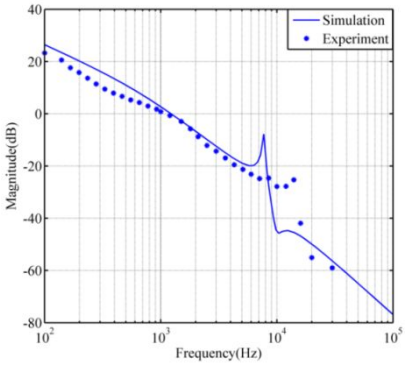
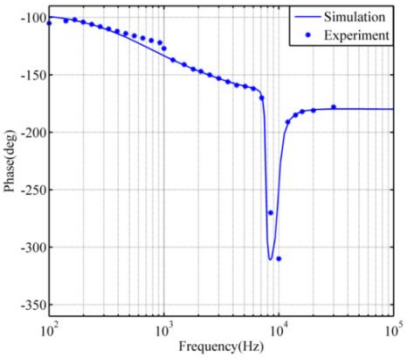


Fig. 14. Experimental waveforms comparing two drive signals to measure dead time t_{d2}

Fig. 15 shows the theoretical and experimental comparison of the loop gain. The dashed lines represent the theoretical magnitude and phase responses while the dotted lines show the measured results.



(a) Magnitude characteristics



(b) Phase characteristics

Fig. 15. Calculated and measured results of the loop gain

It can be seen that the theoretical analysis matches the full range of frequencies. It also proved the feasibility and correctness of the modeling technique. The deviations of the corner frequency between the analytically derived result and the measurements may be caused by the parasitic capacitance of switches S_1 and S_2. As the loop crossover is much lower than the corner frequency, the presented model is deemed to be suitable for practical applications.

When the load current I_o alternately varies between 0.5A and 6A with a period of 12ms, the waveform of output voltage V_o is shown in Fig. 16. Based on the result, we can see that after the transient response time (about 2 ms), the output voltage tends to be steady-state.

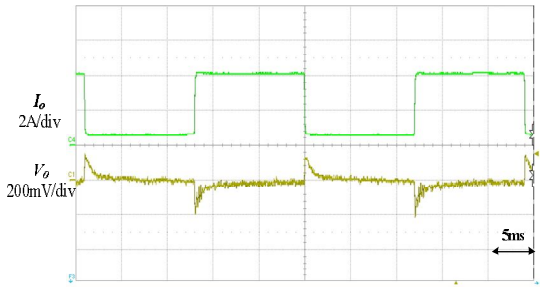


Fig. 16. The output voltage transient response for the variation of load current with V_{in}=80V

The load regulation characteristics of the proposed converter are provided in Fig. 17. Based on the result, it can be seen that the proposed converter was well controlled with the self-driven active clamp circuit. Likewise, it tends to indicated that the calculated auxiliary winding number is sufficient to drive the active clamp switch.

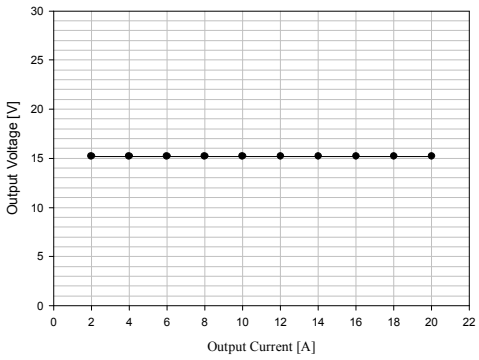


Fig. 17. Load regulation

Fig. 18 shows the achieved efficiency curve of the active clamp prototype employing the self-driven circuit with the input voltage 80V, output voltage 15V and output current ranging from 1A to 20A. The efficiency at full load is about 91%.

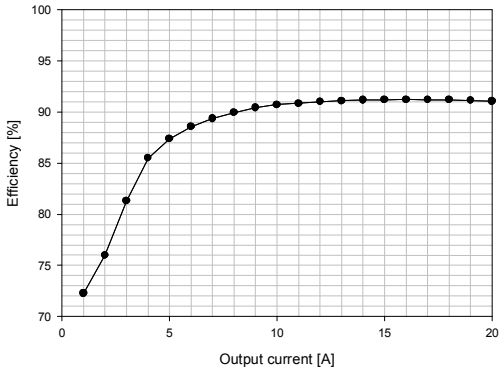


Fig. 18. Achieved efficiency of the proposed converter

5. Conclusion

A SEPIC-input self-driven active clamp ZVS forward converter is proposed in this paper. With the simple auxiliary self-driven circuit, the active clamp switch can perform asymmetrical duty control and ZVS operation easily. It also makes the converter more reliable. The mathematical analysis of the detailed circuit operation modes is presented, and key issues about the self-driven design are discussed in this paper. Furthermore, the state-space modeling of the proposed converter has been provided in order to optimize dynamic performance. The small-signal model is then derived to study steady-state and transient characteristic simulations. The experimental results, based on a laboratory prototype circuit (15V/20A), are provided to verify the effectiveness and performance of the proposed converter. We achieved consistency good agreement between theoretical prediction and experimental data in both the gain and the phase up to one-tenth of the switching frequency. Because of these properties, the proposed converter is expected to find wide applications in DC power supply systems.

References

[1] Bor-Ren Lin, Kevin Huang, David Wang. "Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier", IEEE Transactions on Circuit And Systems, Vol. 53, No.6, pp. 1310-1319, June 2006.

[2] Juan M. Rivas, Yehui Han, Olivia Leitermann, Anthony D. Sagneri, David J. Perreault. "A high-frequency resonant inverter topology with low voltage stress", IEEE Transactions on Power Electronics, Vol. 23, No.4, pp. 1759-1771, July 2008.

[3] Heldwem M.L. Ferrari de Souza, A. Barbi, I, "A primary side clamping circuit applied to the ZVS-PWM asymmetrical half-bridge converter", Power Electronics Specialists Conference, 2000 .PESC 00. 2000 IEEE 31st annual, Vol.1, pp.199-204.

[4] Shijia Yang, Zhaoming Qian, Qian Ouyang, Fang Z. Peng. "An Improved Active-clamp ZVS Forward Converter Circuit", in Proc. 23th Annu. Applied Power Electronics Conf., Feb. 2008, pp. 318-322.

[5] Bum-sun Lim, Hee-Jun Kim, and Won-Sum Chung, "A self-driven active clamp forward converter using the auxiliary winding of the power transformer", IEEE Transactions on Circuit And Systems, Vol. 51, No.10, pp. 549-551, October 2004.

[6] Y. –H. Leu and C. –L. Chen, "Improved asymmetrical half-bridge converter using a tapped output inductor filter", IEEE Proc. Electric Power Applications, Vol.150, No.4, pp.417-423, July 2003.

[7] Keun-Wook Lee, Seong-Wook Choi, Byoung-Hee Lee, Gun-Woo Moon. "Current boosted active clamp forward converter without output filter", in Proc. Energy Conversion Congress and Exposition, Sept. 2009, pp. 2873-2880.

[8] Satoshi Tomioka, Tamotsu Ninomiya, Hiroto Terashi. "Interleaved-Boost-Input Type Isolated Full Bridge PFC Converter", in Proc. Power Electronics and Drives Systems, Nov. 2005, pp. 146 - 151.

[9] T. Tanitteerapan. "Analysis of power factor correction isolated SEPIC rectifiers using inductor detection technique", in Proc. Circuits and Systems, July 2004, pp.25-28.

[10] Y. Karimi, V.R. Nasirian, M. Ahmadian, J. Yaghoobi, M.R. Zolghadri, M. Ferdowsi. "Small-signal model development for a Cúk converter while operating in DCVM for both DC and AC input voltages", in Proc. Energy Conversion Congress and Exposition, Oct. 2010, pp. 2980-2984.

[11] S.Korotkov, V. Meleshin, A. Nemchinov, and S. Fraidlin, "Small-signal modeling of soft-switched asymmetrical half-bridge dc/dc converter", in Proc. 10th Annu. Applied Power Electronics Conf., Mar. 1995, pp.707-711.

[12] M. Masihuzzaman, N. Lakshminarasamma, V. Ramanarayanan. "Steady-state stability of current mode active-clamp ZVS DC–DC converters", IEEE Transactions on Power Electronics, Vol. 253, No.6, pp. 1546-1555, June 2010.

[13] L.K. Wong, T.K. Man, "Small signal modeling of open-loop SEPIC converters", IET Power Electron., Vol. 3, pp.858-868, Nov. 2010.

[14] Vuthchhay Eng, Chanin Bunlaksananusorn. "Modeling of a SEPIC converter operating in discontinuous conduction mode", in Proc. Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, May 2009, pp. 140-143.

[15] Brian T. Irving, Yuri Panov, Milan M. Jovanovic. "Small-signal model of variable-frequency flyback converter", in Proc. 18th Annu. Applied Power Electronics Conf., Feb. 2003, pp. 977 - 982.

[16] Richard Redl. "High-frequency extension of the small-signal model of the constant-frequency current-mode-controlled converter", in Proc. 6th Annu. Applied Power Electronics Conf., Mar. 1991, pp. 466 - 472.

[17] Richard Tymerski, Duwang Li. "State-space models for current programmed pulse width-modulated converters", IEEE Transactions on Power Electronics, Vol. 8, No.3, pp. 271-178, Jul 1993.

[18] Steffen Rohner, Jens Weber, Steffen Bernet. "Continuous model of Modular Multilevel Converter with experimental verification", in Proc. Energy Conversion Congress and Exposition, Sept. 2011, pp. 4021-4028.

[19] Hand Fortin Blanchette, Tarek Ould-Bachir, Jean-Pierre David. "A State-Space Modeling Approach for the FPGA-based Real-Time Simulation of High Switching Frequency Power Converters", IEEE Transactions on Industrial Electronics, Vol.PP, No.99, pp.1, Dec. 2012.

[20] Mohammed S. Agamy, Jain. "A small signal state space model of single stage three level resonant AC/DC converters", in Proc. Power Electronics Specialists Conf., June 2008, pp. 1407 – 1413.

[21] Andressa C. Schittler, Douglas Pappis, Cassiano Rech. Alexandre Campos, Marco A. Dalla Cosra. "Generalized state-space model for the interleaved buck converter", in Proc. Power Electronics Conf. (COBEP), Sept. 2011, pp. 451 – 457.

[22] Richard Redl. "High-frequency extension of the small-signal model of the constant-frequency current-mode-controlled converter", in Proc. 6th Annu. Applied Power Electronics Conf., Mar. 1991, pp.466-472.

[23] Martin Rentzsch, Frank Gleisberg, Henry Guldner, Frank Benecke, Chester Ditmanson. "Closed analytical model of a 20 kV

output voltage, 800 W output power series-parallel-resonant converter with Walton Cockroft multiplier", in Proc. Power Electronics Specialists Conf., June 2008, pp. 1923 – 1929.

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