http://dx.doi.org/10.11142/jicems.2013.2.2.197
Journal of International Conference on Electrical Machines and Systems Vol. 2, No. 2, pp. 197 ~201 , 2013 **197**

Cascaded H-bridge Multilevel Inverter employing Front-end Flyback Converter with Single Independent DC Voltage Source

Ki-du Kim*, Gyou-tak Bae* and Feel-soon Kang**

Abstract – Cascaded H-bridge multilevel inverter requires independent DC voltage sources to produce multi output voltage levels. When it needs to generate more levels in the output voltage wave, the number of independent DC voltage sources usually limits its extension. To solve this problem, we propose a cascaded H-bridge multilevel inverter employing a front-end flyback converter for unifying input DC voltage sources. After theoretical analysis of the proposed circuit, we verify the validity of the proposed inverter using computer-aided simulations and experiments.

Keywords: Cascaded H-bridge Multilevel Inverter, Flyback Converter, Transformer, Inverters, Multilevel systems

1. Introduction

Cascaded H-bridge multilevel inverter has been studied for high voltage applications since it has merits in high reliability, modularity, and number of components [1]-[8]. Usually multilevel inverter is focusing on a generation of a high voltage using lower voltage rating devices connected in series. Also it has a potential advantage to get a high quality output voltage by producing multi levels in the output voltage wave. However, it increases the number of independent DC voltage sources and switching components resulted in the increase of complexity problem and system cost. To solve this problem, many researchers have been studied to reduce the number of components. However, it generally focuses on reducing the number of switching components [4]-[8].

In this paper, we present a cascaded H-bridge multilevel inverter adopting a front-end flyback converter to unify independent DC voltage sources. The flyback converter employs a transformer operated in high switching frequency, and it has one primary winding and two secondary windings. The secondary of the transformer in the general flyback converter consists of one diode and an output capacitor. In the proposed method, the diode is substituted for an active switch to control the output voltage in a constant value. Most of all, we can obtain our goal that is to drive the cascaded H-bridge multilevel inverter with a single independent DC voltage source. Because the transformer is operated in high switching frequency, it does not increase size and volume of the system. After theoretical analysis, the validity of the proposed approach is proved by computer-aided simulations and experiments.

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Received 7 May 2013 ; Accepted 15 May 2013

2. Proposed approach for unifying independent input DC Voltage Sources

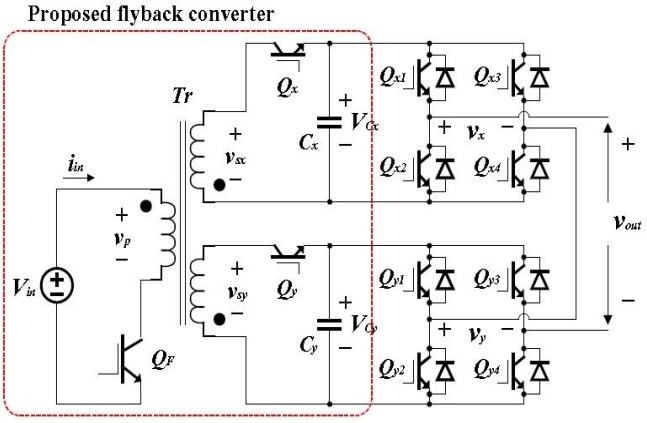


Fig. 1. Cascaded H-bridge multilevel inverter with the proposed front-end flyback converter.

Fig. 1 shows a circuit configuration of the cascaded H-bridge multilevel inverter with the proposed front-end flyback converter. The front-end flyback converter has a high frequency transformer which has two secondary windings to synthesize the upper and lower voltage sources. Amplitude of DC input voltage, duty ratio of switch QF, turn-ratio of the transformer determine voltage across two capacitors located in the secondary of the transformer.

2.1 Operational Mode

Operational mode of the proposed flyback converter is divided into two modes due to the state of switch Q_F. Fig. 2 shows two operational modes. It includes a magnetizing inductance (L_m) of the primary winding. The input current flows through the primary winding and the magnetizing inductance, when Q_F is turned on and Q_x and Q_y are in off state. During this mode, there is no energy transfer to the secondary as shown in Fig. 2(a). And the magnetizing inductance saves energy for the next mode. At mode 2, Q_F is turned off and Q_x and Q_y are turned on at the same time. Then the stored energy is transferred to the secondary of the transformer via the two secondary switches as shown in Fig. 2(b). During this period, Q_x and Q_y are automatically turned off, if voltage across the capacitor reaches to a preset voltage command value as given in Fig. 3. By this manner, voltage across the capacitor (C_x and C_y) is maintained in a constant value. If the secondary circuit of the flyback converter employs diodes instead of active switches like the traditional flyback circuit, it is impossible to maintain voltage across the capacitor constantly when the load is unbalanced.

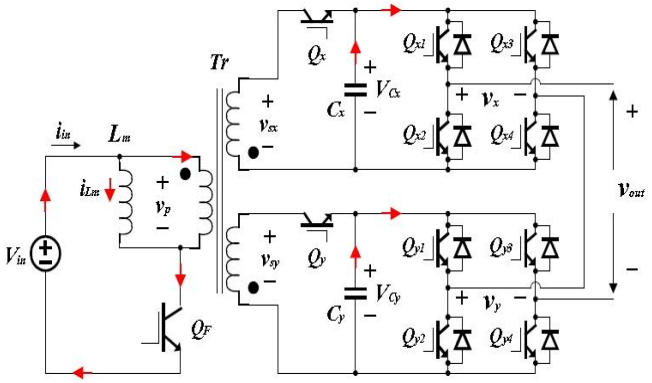


Fig. 2. Operational mode, (a) Mode 1, Q_F = ON, (b) Mode 2, Q_F = OFF.

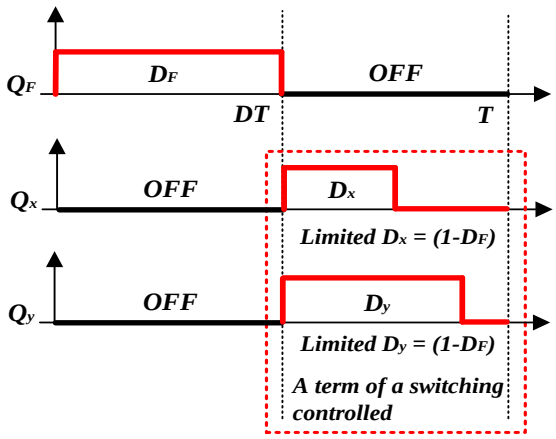


Fig. 3. Control signal for Q_F , Qx and Qy

2.2 Relationship Between Input and Output Voltage by Duty-ratio of Q_F

Voltage across the capacitor in the secondary of the transformer is obtained by applying volt-sec. balance theory to the magnetizing inductance of the transformer.

$$v_{cx} = \frac{N_2}{N_1} \cdot \frac{D_F}{D_x} \cdot V_{in} \tag{1}$$

$$v_{cy} = \frac{N_2}{N_1} \cdot \frac{D_F}{D_y} \cdot V_{in} \tag{2}$$

where, V_{in} is the input DC voltage. D_F is duty ratio of Q_F. D_x and D_y are the duty ratio of the Q_x and Q_y, respectively. N_1 and N_2 are turn ratio of the primary and the secondary windings of the transformer. To maintain the capacitor voltage constantly, it needs to control duty ratio of the switches (Q_x and Q_y). Each duty ratio of the switches is defined by

$$D_{x(y)} \leq 1 - D_F < 0.5 \tag{3}$$

The secondary switches are working when the primary switch is turned off. And these switches are turned off when voltage across the capacitor reaches to a preset command value. Considering a pure resistive load, voltage ripple in each capacitor can be obtained by

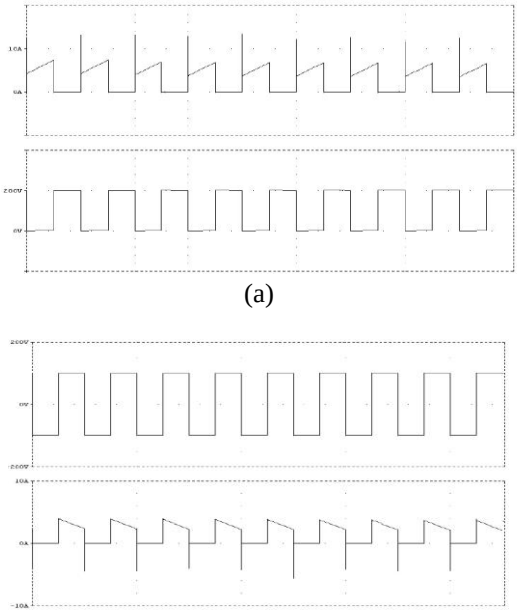
$$\Delta v_{cy} = \frac{\Delta Q_{Cx}}{C_x} = \frac{V_{Cx} \cdot D_F}{RC_x \cdot f_s} \tag{4}$$

$$\Delta v_{cy} = \frac{\Delta Q_{Cy}}{C_y} = \frac{V_{Cy} \cdot D_F}{RC_y \cdot f_s} \tag{5}$$

where, ΔQ means the variation of electric charge in a capacitor. f_S is the switching frequency of Q_F. D_F means the duty ratio of Q_F.

3. Simulation Results

To verify the validity of the proposed approach, we performed computer-aided simulations using PSpice. In this simulation, input voltage is set to DC 100[V], turn-ratio of the transformer is set to the same value so the output capacitor voltage is controlled by the duty ratio of the switch QF in a step-up condition. Switching frequency of all switches are 20[kHz], and maximum duty cycle is limited at 24[μs]. The target output voltage of the multilevel inverter is set to AC 220[V], 60[Hz]. And it was considered to a pure resistive load.

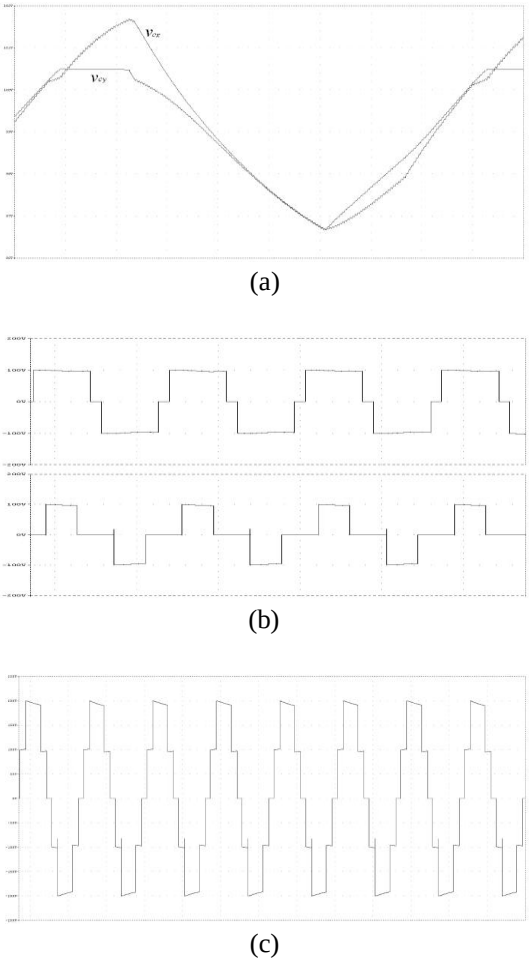


(a)

(b)

Fig. 4. Simulation results, (a) Drain current and voltage across the switch Q_F, (b) Secondary voltage of the transformer and switch Q_x current.

Fig. 4(a) is simulation results for the primary switch Q_F. It shows a drain current of the switch Q_F and voltage across the switch in sequence. Here, voltage stress of the switch Q_F becomes twice of the input voltage because of the induced voltage from the secondary of the transformer. The secondary voltage of the transformer is given in the upper side of Fig. 4(b), and the lower waveform is a current flowing through the secondary switch Q_x. The source of the switch current is the energy stored in the magnetizing inductance during the prior mode. The duty cycle of Q_x and Q_y will be changed by the capacitor voltage depending on a load condition of multilevel inverter. In case of the switch Q_y, it has the same waveform when output capacitor voltage C_x and C_y have the same value.



(a)

(b)

(c)

Fig. 5. Simulation results, (a) Voltage across the secondary capacitor (v_{Cx} and v_{Cy}), (b) Terminal voltage of each H-bridge module (v_x and v_y), (c) Output voltage (V_{out}).

Fig. 5(a) shows voltage across the secondary capacitor (v_{Cx} and v_{Cy}). The amplitude of the upper capacitor voltage (v_{Cx}) varies from 101.7 [V] to 97.7 [V]. The maximum deviation is about 4 [V]. Because the target voltage of the capacitor is set to 100 [V], we can say the voltage ripple is regulated in 4 [%]. On the other hand, the amplitude of the lower capacitor voltage (v_{Cy}) changes between 100.5 [V] and 97.7 [V]. Because the maximum deviation is about 2.8 [V], the voltage ripple of the lower capacitor is regulated in 2.8 [%]. Fig. 5(b) shows terminal voltages of each H-bridge module. As shown in this figure, voltage ripple of the capacitor is slightly appeared in the terminal voltage waves. Fig. 5(c) shows an output voltage, which is synthesized by the sum of each H-bridge voltage. In this simulation, since we used two H-bridge module, the output voltage has five voltage levels.

4. Experiment Results

To verify the validity of the proposed approach, we implemented experiments using a prototype. Input voltage is set to DC 48[V] by accumulation of 4 batteries of 12[V] connected in series. Switching device is Power MOSFET IRFP360 (Vds=400V, Id=23A, Rds(on)=0.20Ω) by IXYS. EE7166 (AL value=9500) was used for high frequency transformer. DSP based controller was designed by TMS320F28335. Parameters are listed in Table. 1

Table 1. Parameters for a prototype.

Parameter	Value
Input voltage, V_{in}	DC 48[V]
Magnetizing inductance, L_m	300[μH]
Leakage inductance, $L_{leakage}$	2[μH]
Switching frequency, f_S	20[kHz]
Turns-ratio	1:1:1
Maximum Duty-ratio, D	0.4
Capacitor, C_x,C_y	1000[μF]
load	200[Ω]

Fig. 6 shows experiment results for voltage and current of switching devices. Fig. 6(a) shows voltage across QF and input current which is stored in the magnetizing inductance of the transformer during ON state of QF. When QF turns on, Qx and Qy are turned off. Therefore, there are no current flowing through Qx and Qy as shown in Fig. 6(b) and 6(c).

When QF turns off, Qx and Qy start to flow current depending on voltage levels of capacitor Cx and Cy. By controlling of duty-ratio of Qx and Qy, voltage across Cx and Cy are maintained constantly.

Fig. 7 shows each terminal voltage (vx and vy) of H-bridge module and output voltage (vout). The output voltage is controlled by PD (Phase disposition) method. Here, ma is set to 1 so voltage across Cx and Cy are controlled as 48[V]. Generally, cascaded H-bridge multilevel inverter generating 5-levels need two independent DC voltage sources. One is for generating Vdc level, and the other are used to generate 2Vdc voltage level, therefore, each DC voltage source has different power capacities. Hence, Vdc level is covered by capacitor Cy, and 2Vdc is charged by Cx. So voltage ripple of Cy is larger than that of Cx. But in the proposed approach, voltage across Cx and Cy are controlled by Qx and Qy as in a constant value.

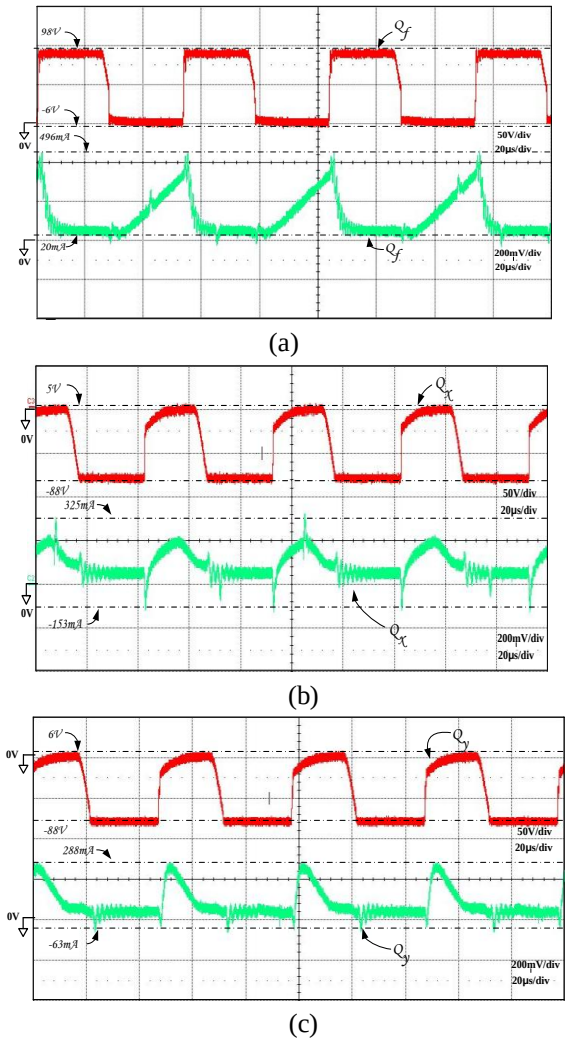


Fig. 6. Experiment results, (a) voltage across Q_F and drain current of Q_F, (b) voltage across Q_x and drain current of Q_x, (c) voltage across Q_y and drain current of Q_y from top to bottom.

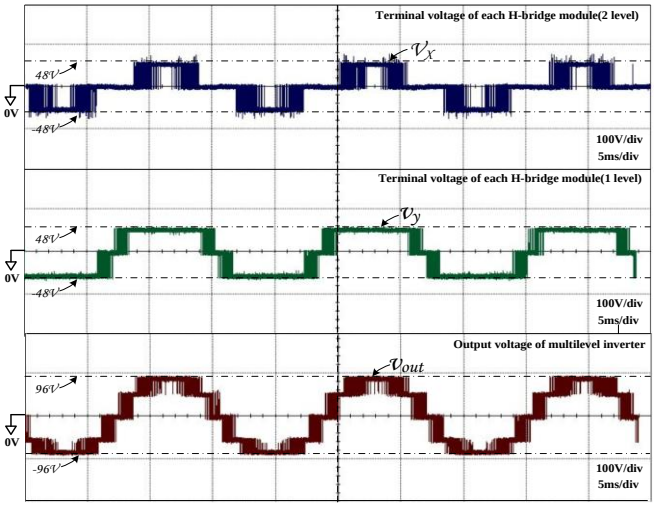


Fig. 7. Experiment results of v_x, v_y, and v_{out}.

5. Conclusion

We proposed a cascaded H-bridge multilevel inverter employing a front-end flyback converter to unify independent DC voltage sources. Topologically, in the proposed approach, the diode of the general flyback converter is substituted for an active switch to control the output voltage in a constant value. Most of all, we can obtain our goal that is to drive the cascaded H-bridge multilevel inverter with a single independent DC voltage source without increasing size and volume of the system, since the transformer is operated in high switching frequency. After theoretical analysis, the validity of the proposed approach is proved by computer-aided simulations and experiment using a prototype.

Acknowledgements

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology(No.2012-006120)

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