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Unification of Buck-boost and Flyback Converter for Driving Cascaded H-bridge Multilevel Inverter with Single Independent DC Voltage Source

Seong-hye Kim*, Han-Tae Kim*, Jin-soo Park* and Feel-soon Kang**

Abstract – It presents a unification of buck-boost and flyback converter for driving a cascaded H-bridge multilevel inverter with a single independent DC voltage source. Cascaded H-bridge multilevel inverter is useful to make many output voltage levels for sinusoidal waveform by combining two or more H-bridge modules. However, each H-bridge module needs an independent DC voltage source to generate multi levels in an output voltage. This topological characteristic brings a demerit of increasing the number of independent DC voltage sources when it needs to increase the number of output voltage levels. To solve this problem, we propose a converter combining a buck-boost converter with a flyback converter. The proposed converter provides independent DC voltage sources at back-end two H-bridge modules. After analyzing theoretical operation of the circuit topology, the validity of the proposed approach is verified by computer-aided simulations using PSIM and experiments.

Keywords: Buck-boost converter, cascaded H-bridge multilevel inverter, transformer, Inverters, Multilevel systems

1. Introduction

Cascaded H-bridge multilevel inverter has advantages in number of components, high reliability, and simplicity [1]-[6]. The primary purpose of the multilevel inverter is the production of higher output voltage by synthesizing low voltage of several inverter modules connected in series. If the number of module increases, it generates lots of voltage levels resulted in improving total harmonic distortion of output voltage. However, it results an increase of system cost and complexity problems due to the large number of switching devices and other components. To solve the above mentioned problem, several researches implemented and reported [7]-[9]. Among them, cascaded-transformer based multilevel inverter seems to be the best choice to reduce the number of switches and input voltage sources. In [8], it synthesizes 27 levels in the output voltage. It consists of an independent DC voltage source, three H-bridge cells connected to a cascaded transformer. Because the operating frequency of the transformer is low, the size and volume will be increased. Moreover, the transformer will decrease the system efficiency. So we can notice that the use of low frequency transformer is not the best way to improve performance of single DC voltage sourced multilevel inverter.

To solve the problem, we propose a converter combining a buck-boost converter with a flyback converter. It focuses on minimizing of the independent DC input voltage sources in a traditional cascaded H-bridge multilevel inverter. After theoretical analyses, the validity of the proposed approach is verified through computer-aided simulations using PSIM and experiments.

2. Proposed Front-end Buck-boost Converter for Single DC Voltage Sourced Multilevel Inverter

2.1 Circuit Configuration of Conventional Cascaded H-bridge Multilevel Inverter

A circuit configuration of a conventional cascaded H-bridge multilevel inverter is shown as Fig. 1. Each H-bridge cell has an independent DC voltage source of Vdc. An output terminal point of each module is connected each other in series. As a result, the output voltage is determined by (1). And the number of output voltage levels (N) is obtained by (2).

$$v_{out} = \sum_{n=1}^{k} v_n \tag{1}$$

$$N = 2k + 1 \tag{2}$$

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where k is the number of H-bridge cells.

We can realize that this kind of multilevel inverter is advantageous in the viewpoint of modularity and simplicity. A large number of output voltage levels ensure that output voltage is close to a sinusoidal wave. However, in Eq. (2), when it increases the number of H-bridge module (k) in order to generate more output voltage levels, it results in the increase of the number of switches and independent DC voltage sources. It needs 4k switches and k independent DC voltage sources to generate N output voltage levels.

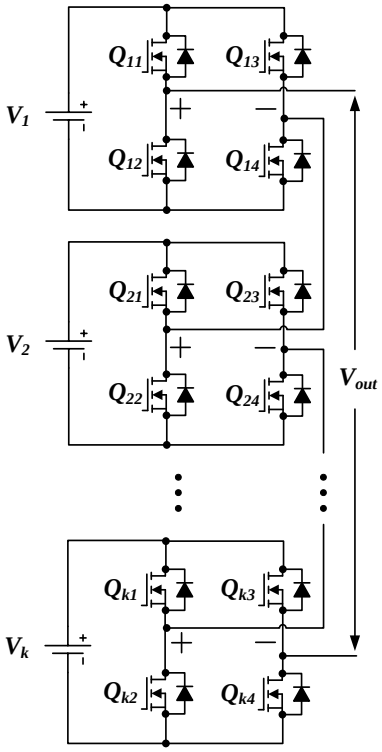


Fig. 1. Circuit configuration of a general cascaded H-bridge multilevel inverter

2.2 Traditional Buck-boost and Flyback Converter

As mentioned above, H-bridge module increases volume of the system by the need of independent DC voltage source per a cell. Thus, it needs to find a way to reduce the number of independent DC voltage sources. To solve this problem, we will employ a DC-to-DC converter which can generate multiple independent DC voltage sources. It is based on a unified configuration of buck-boost and flyback converter. Before explaining the proposed converter, we review the conventional buck-boost and flyback converter.

Fig. 2(a) and Fig. 2(b) show traditional buck-boost and flyback converter, respectively. Both converters have a similar structure except a magnetic element. That is a galvanic isolation. Depending on operation of Q_{sw}, diode currents flowing through D_x (i_{Dx}) and D_y (i_{Dy}) are given in Fig. 2(c). Both waveforms have same slope and amplitude on the assumption that every design specification is equal. When Q_{sw} turned on, the energy of input source is charged to a magnetic component; inductance of the inductor L and magnetizing inductance of the transformer Tr. When Q_{sw} turned off, each energy saved in the magnetic components starts to discharge into back-end capacitor C_x and C_y. At this viewpoint, we try to combine each DC voltage source using a transformer. It means that a transformer plays two roles. One is an inductor for a buck-boost converter, and the other is a transformer for a flyback converter. So it is adaptable to a cascaded H-bridge multilevel inverter which needs two independent DC voltage sources.

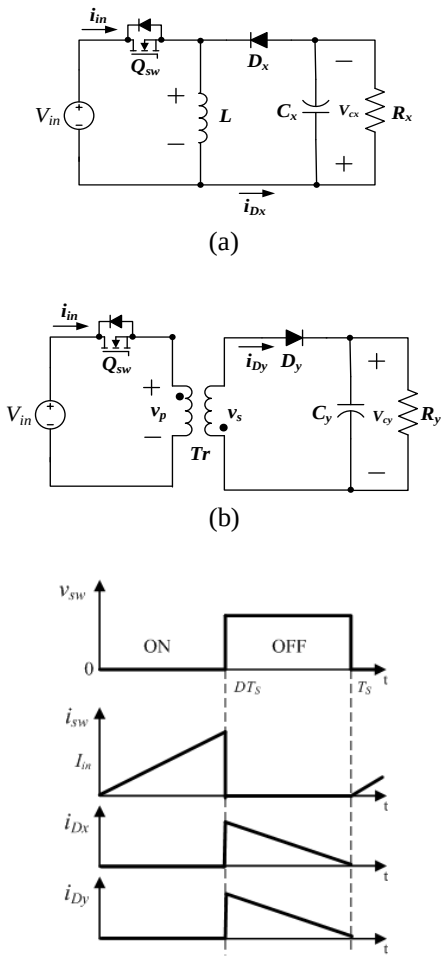


Fig. 2. Circuit configurations and key waveforms, (a) buck-boost converter, (b) flyback converter, (c) voltage across switch, switch current, and diode currents

2.3 Cascaded H-bridge Multilevel Inverter Employing a Front-end Unified Converter

Fig. 3 shows a cascaded H-bridge multilevel inverter with the proposed converter. It has a single DC voltage

source, one transformer, and two H-bridge cells. The upper capacitor is charged by a buck-boost operated circuit. The inductor of the buck-boost converter is substituted for a transformer operated in high frequency. And the lower capacitor is charged by flyback operated circuit.

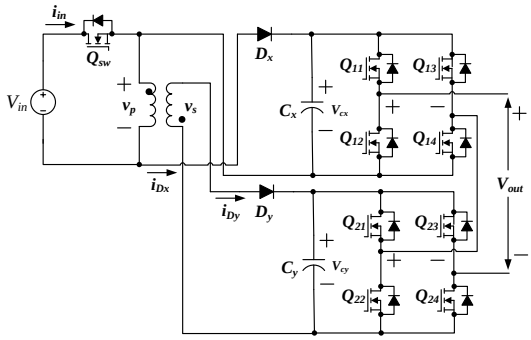
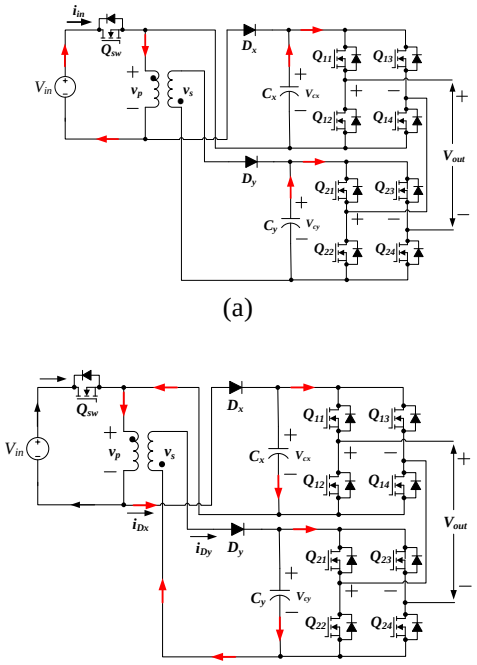


Fig. 3. Proposed circuit configuration

By switching Q_{sw}, it provides energy into upper (C_x) and lower (C_y) capacitor regardless of a back-end inverting operation. The primary current of the transformer (i_p) is applied from an input current (i_{in}) by turning Q_{sw} on, as shown in Fig. 4(a). During this interval, the primary current of transformer and magnetizing current increase simultaneously. Voltage across the upper and the lower capacitors (v_x and v_y) discharge into each H-bridge cell. In this period, there is no current flowing through D_x and D_y. When Q_{sw} turns off, the stored energy in the magnetizing inductance discharges into back-end capacitors. The upper capacitor C_x starts to save in the non-insulating way. And the lower capacitor C_y charges by the secondary of the transformer as shown in Fig. 4(b).

The upper and lower diode currents look like those of given in Fig. 2(c). In the proposed circuit, the slope of the upper diode current (i_{Dx}) is larger than that of the lower diode current (i_{Dy}) in the early period because the upper load directly leads the current of upper diode D_x (i_{Dx}) from magnetizing inductance while the current of lower diode D_y (i_{Dy}) is the remaining energy of magnetizing inductance.

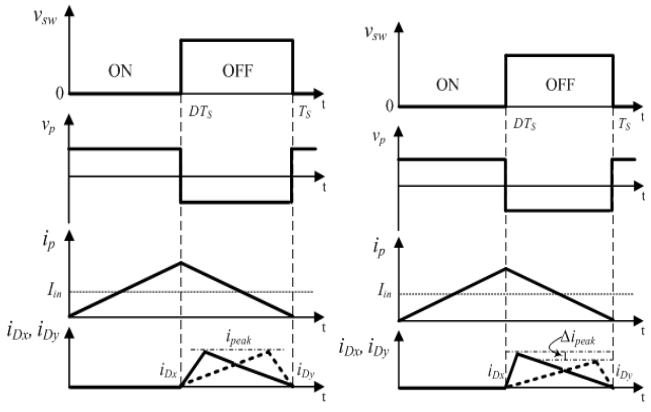
As shown in Fig. 5(a) and (b), they have different slope between the upper diode and lower diode current. Fig. 5(a) is when two loads with the same value are connected with each H-bridge cell. We notice that peak current flowing through diode of each cell is equal while rising or falling incline of i_{Dx} and i_{Dy} is dissimilar but they are symmetry in the vertical axis. This is the reason why the upper H-bridge module is non-isolation configuration with a power source so the magnetizing energy stored in the primary of the transformer is directly discharging to load through a wheeling diode D_x. On the other hand, the lower H-bride cell is isolation structure with an input source. Therefore the remained magnetizing energy of the upper H-bridge cell discharges to a load by wheeling diode D_y. Fig. 5(b) shows diode current waveform of D_x and D_y in the proposed inverter. It is the case of when different loads are connected. It means that the upper and the lower capacitor need different power to supply energy to load because of multilevel generating. This is reason why the slope and peak value of current flowing through diode are different that of Fig. 5(a), which has same peak value and dissimilar slop.



(a)

(b)

Fig. 4. Operational mode, (a) Q_{sw} = ON, (b) Q_{sw} = OFF



(a) (b)

Fig. 5. Key waveform, (a) with the same parallel load cells, (b) with upper and lower H-bride cells supplying a different power to load

By applying voltage-second balancing theory to the primary of the transformer, the upper circuit shows the following relation.

$$V_{in} \cdot D \cdot T_s = V_{Cx} \cdot (1 - D) \cdot T_s \tag{3}$$

From Eq. (3), voltage across the upper capacitor can be obtained by Eq. (4).

$$V_{Cx} = \frac{D}{(1 - D)} \cdot V_{in} \tag{4}$$

From Eq. (4), we can notice that it is equal to that of the traditional buck-boost converter. By applying voltage-second balancing theory to the primary of the transformer, the lower circuit shows the following relation.

$$V_{in} \cdot D \cdot T_s = \frac{N_1}{N_2} \cdot V_{Cy} \cdot (1 - D) \cdot T_s \tag{5}$$

From Eq. (5), voltage across the lower capacitor can be obtained by

$$V_{Cy} = \frac{N_2}{N_1} \cdot \frac{D}{(1 - D)} \cdot V_{in} \tag{6}$$

From Eq. (6), we can notice that it is equal to that of the traditional flyback converter. It is also equivalent to that of a buck-boost converter except the term of turn-ratio. If we set equal turn-ratio to the transformer, Eq. (4) becomes Eq. (6). It means the proposed circuit can be controlled like a buck-boost converter.

3. Simulation Results

We performed computer-aided simulations to verify the validity of the proposed circuit operation. In this simulation, input voltage is set to DC 100[V], and output voltage is set to AC 200[V] with 60[Hz] operating frequency. Turns-ratio of the transformer is set to 1:1. Switching frequency of input switch (Q_{sw}) is set to 20[kHz]. The simulation was implemented by PSIM with consideration for pure resistive load.

Fig. 6 shows voltage across input switch (Q_{sw}) with input current. Due to the induced voltage from the secondary of the transformer, voltage stress of the input switch becomes two fold of the input voltage source. Fig. 7 shows voltage and current of the transformer. Because turn-ratio of the transformer is set equally, voltage across the primary and secondary has the same waveform. From the primary current waveform, we can find the magnetizing current when the input switch turned on. The upper and lower diode currents by magnetizing inductance of transformer are given in Fig. 8. When the input switch turns off, these currents start to charge the upper and lower capacitors. Because the energy source of currents is the magnetizing inductance of the transformer, the demagnetizing current is divided and charges two capacitors. At this time, diode current of between upper and lower capacitors is not equal because upper capacitor always supplies energy for ±1 level. So power of upper capacitor is consumed more than lower capacitor. From Fig. 9, we know that the output voltage can be obtained with 5 levels by using these capacitor voltage sources.

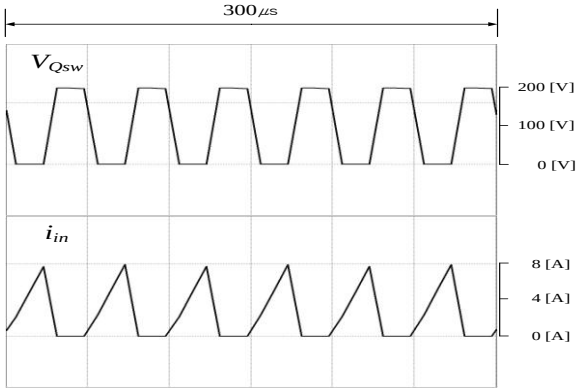


Fig. 6. Voltage across Q_{sw} and input current

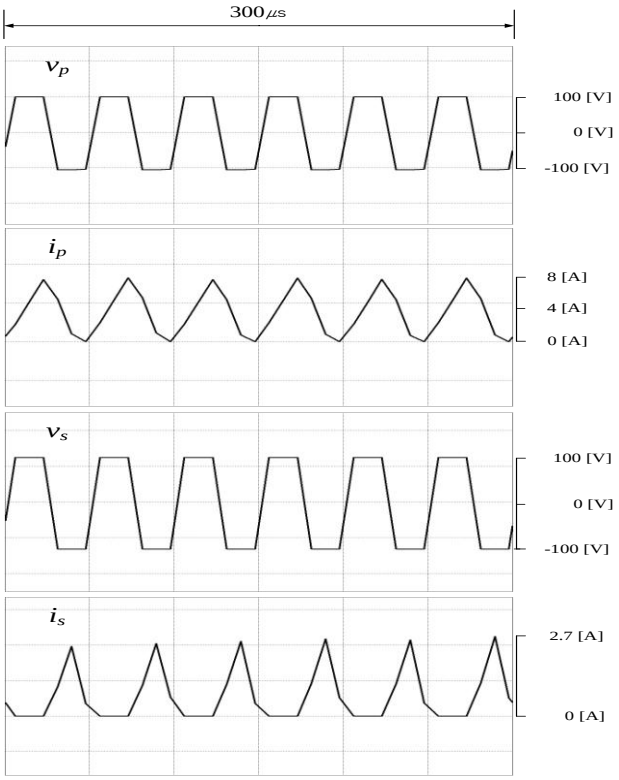


Fig. 7. Primary and secondary voltage of transformer with current

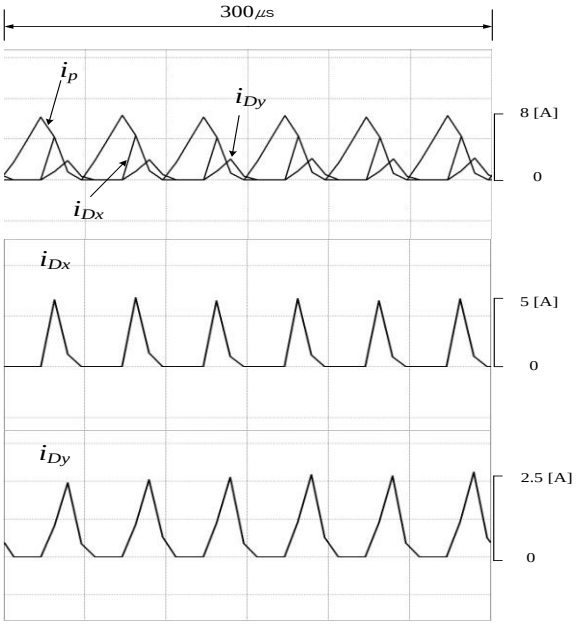


Fig. 8. Upper and lower diode current by magnetizing in ductance of transformer

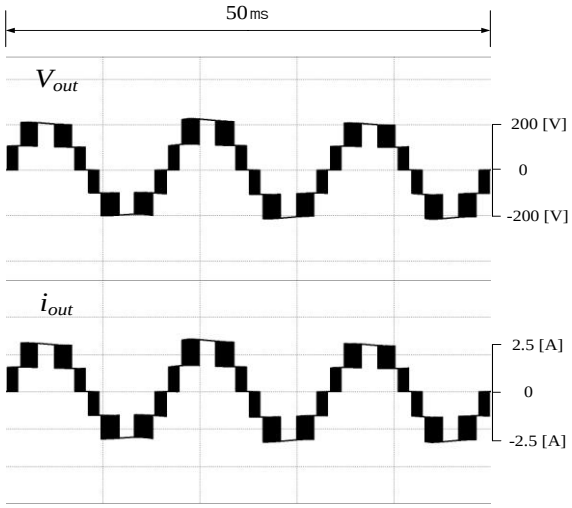


Fig. 9. 5-levels output voltage and current

4. Experiment Results

We carry out experiments for a validity of proposed inverter. A prototype of 200[W] is designed and controlled by a digital controller using a DSP 28335. Specifications of prototype are listed in Table 1. The experiment was implemented with consideration of pure resistance load.

Fig. 10 shows voltage across Q_{sw} and input current. Q_{sw} is operated by the signal of DSP 28335. Duty ratio of Q_{sw} is limited at 0.5 for supplying energy to the upper and lower capacitor. When the switch Q_{sw} turns on, the input current flows through the primary of the transformer. Fig. 11 shows the primary and secondary voltage of transformer with current.

Table 1. Specifications of prototype.

Component	value
Input Voltage, V_{in}	50 [V]
Output Power, P_o	200 [W]
Output voltage, V_o (peak)	100 [V]
Switching frequency, f_s	20 [kHz]
Duty Ratio, D	0.5
Transformer primary to secondary turn ratio N_1:N_2	1:1
Peak diode voltage on the upper and lower cell, D_x, D_y	40 [V]
Capacitor, C_x, C_y	1000 [μF]

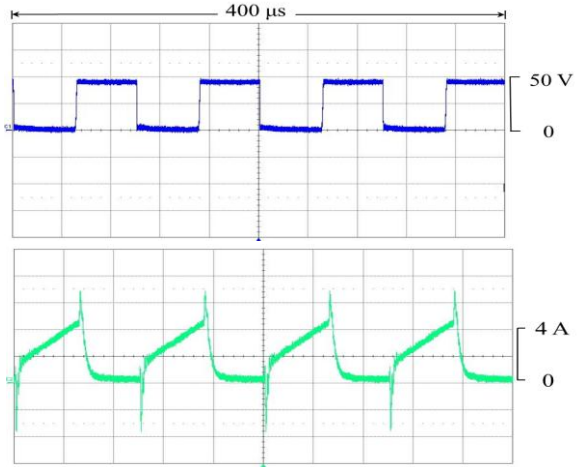


Fig. 10. Voltage across Q_{sw} and input current

Because turn-ratio is set to 1:1, voltages across the primary and the secondary of the transformer have the same waveform. The secondary current reduces the slope and peak value compared to that of the primary current.

Fig. 12 shows the upper (i_{Dx}) and the lower (i_{Dy}) diode current. The lower capacitor (C_y) supplies energy when the output voltage generates $\pm 2V_{dc}$, and the upper capacitor (C_x) discharges when the output voltage is $\pm V_{dc}$ for synthesizing a basic level. Hence, the peak of the upper diode current is higher than that of the lower.

Fig. 13 shows an output voltage and current waveforms with a pure resistive load of 200[W]. Output voltage has five voltage levels. The upper capacitor voltage synthesizes a basic voltage level ($\pm V_{dc}$) and the lower capacitor adds $\pm V_{dc}$ to the basic voltage level so the output voltage level becomes five levels as $-2V_{dc}$, $-V_{dc}$, 0, V_{dc}, $2V_{dc}$. As shown in Fig. 13, voltage across the lower capacitor is slightly lower than that of the upper because of conversion loss by the

transformer.

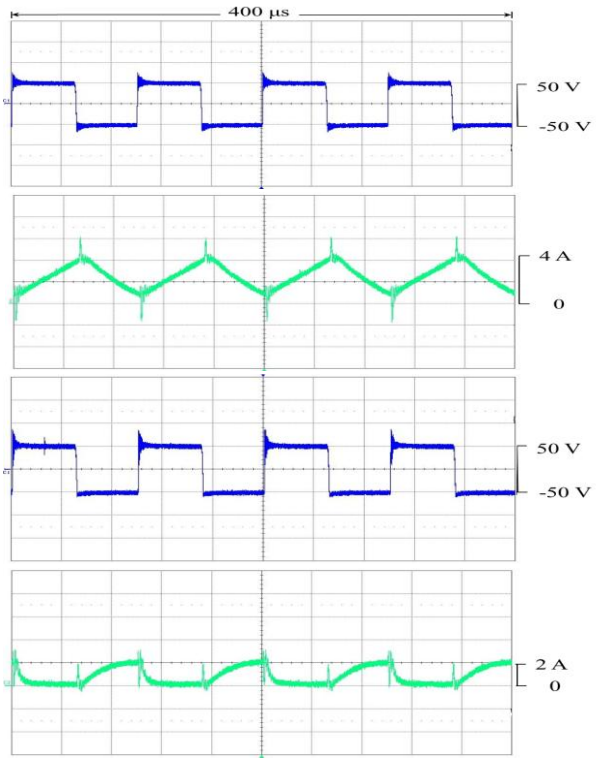


Fig. 11. Primary and secondary voltage of transformer with current

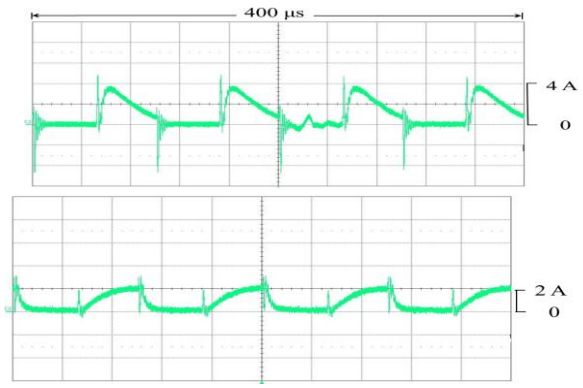


Fig. 12. Upper (i_{Dx}) and lower (i_{Dy}) diode currents

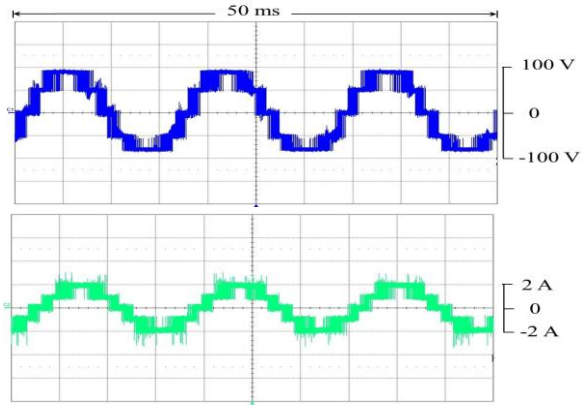


Fig. 13. 5-levels output voltage and current

5. Conclusion

For the application of cascaded H-bridge multilevel inverter with a single independent DC voltage source, we presented a unified DC-to-DC converter combining a buck-boost converter with a flyback converter. By employing the proposed converter to a cascaded H-bridge multilevel inverter, it can synthesize five output voltage levels with a single independent DC voltage source. After theoretical analyses, the validity of the proposed approach was verified by computer-aided simulations and experiments using a prototype of 200 [W].

Acknowledgements

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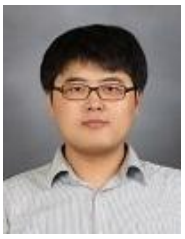

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