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Basic Characteristic of 5-level Inverter with Different Divided DC Link Voltage

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Abstract – This paper report on experimental results of 5-level inverter by DC divided link voltage. We have alreday reported that DC divided link valtage comes to be able to reduse harmonic of out line voltage. So we tested whether DC divided link voltage can reduce harmonics in experimental setup. This paper shows simulation results and experimental results. And we confirmed that DC divided link voltage can also apply in experimental setup.

Keywords: Multi-level, harmonic, Divided DC link voltage, Increase output voltage level

1. Introduction

Multi-connected inverters have been used for the sake of more high performance. Recently, multi-level converters for high power applications have been actively investigated. The converters have the attracting performance such as the high voltage withstand capability and realizing a near sinusoidal waveform. In particular, 3-level converters have been put to practical uses. The 5-level converters have better performance compared to the 3-level ones.

But the 5-level converters have certain problem such as unbalance of potential of P1, NPP, and N1, so each capacitor voltage must maintain to be constant. So, the 5-level inverter is controlled with PWM strategy. Our research is reducing higher harmonics. Usually, DC-Link Voltages are divided equality. Then, we can choose 4 pattern line to line Voltages. But, if this voltages are divided as a:b:b:a, we can select that 6 patterns. The output line voltages are approached more sinusoidal waves. It means that we can reduce the higher harmonics. The best ratio a:b is 1:2. Dividing DC link voltages for 1:2:2:1 can increase the output voltage pattern and reduce the higher harmonic.

Then we found some problems. That makes different losses in each IGBT. So, we propose 2-seriese connection of these IGBT to make the voltage uniformity [2]. After we have verified by simulation that the method of the above is valid, we investigated whether the experimental machine can also be applied in. Experimental setup was used for comparison carrier modulation for simplification program.

To accommodate experimental setup, simulation was also performed again using the comparison carrier modulation. Simulation results of this paper are to put the results of comparison carrier modulation.

2. Main circuit of 5-level inverter

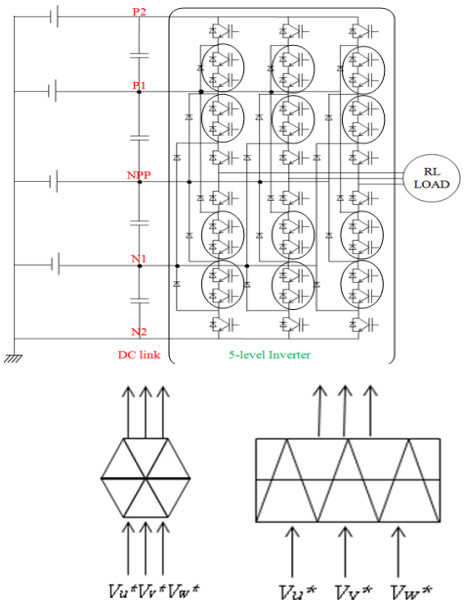

Fig. 1. Proposed Main Circuit of 5-level Inverter

Fig.1 shows the main circuit configuration of the 5-level double converter. Left side of this figure shows the DC link. We introduced a diode-clamped 5-level converter. Each phase consist of twelve switching devices (S1-S12), and six clamping diodes (D1-D6). Generally, the part is surrounded by a circle has an only one IGBT. To solve the problem of

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different losses of each IGBT, we connected two IGBTs in series. The DC link between the rectifier and the inverter consists of four capacitors connected in series. The 5-level double converter has five potentials (P2, P1, NPP, N1, and N2) in the DC link. Neutral point potential (NPP) corresponds to a neutral point of the DC link [1]. Output unit was connected RL Load.

3. Divided DC link voltage

Fig.2 and Fig.3 show DC-Link Voltages. Usually, DC-Link voltages are divided equality. Then, we can choose 4 pattern line Voltages as Fig2. But, if these voltages are divided as Fig3, we can select that 6 pattern. By select suitable ratio with a and b, the output line voltages are approached more sinusoidal waves. It means that we can reduce the higher harmonics.

In PWM method, same switching count in a control cycle. Fig4 shows 1 cycle of line voltage. The point of intersection both each levels potential and command voltage makes 6 rectangles. Then, these rectangles become the smallest, the method makes high performance. Coordinates of each apex defined $Z_0(x_0,y_0)$,.....,$Z_6(x_6,y_6)$.y is calculated the size of a and b. y is calculated the size of a and b. x is calculated $\sin^{-1}y$. Then the gross area of rectangles is calculated in following. By use of eq.[1], the best ratio of a:b is 1:2.

$$S = (x_1 - x_0)(y_1 - y_0) + (x_2 - x_1)(y_2 - y_1) + (x_3 - x_2)(y_3 - y_2) + (x_4 - x_3)(y_4 - y_3) + (x_5 - x_4)(y_5 - y_4) + (x_6 - x_5)(y_6 - y_5)$$
$$x_n = \sin^{-1}y_n \qquad [1]$$

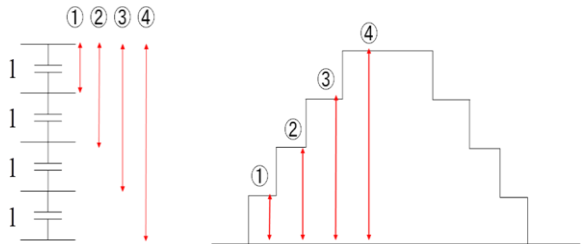


Fig. 2. DC Link Voltage and output voltage levels (conventional)

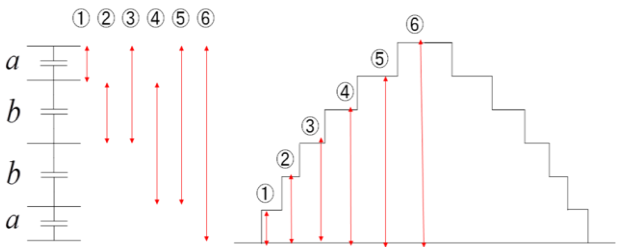


Fig. 3. DC Link Voltage and output voltage levels (proposed)

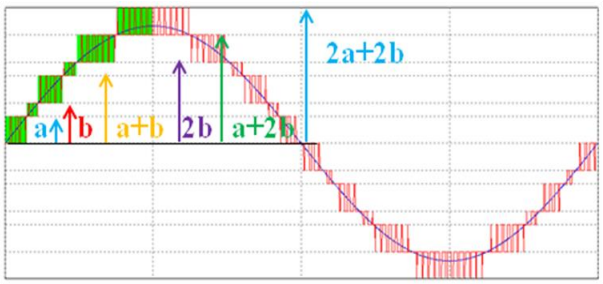
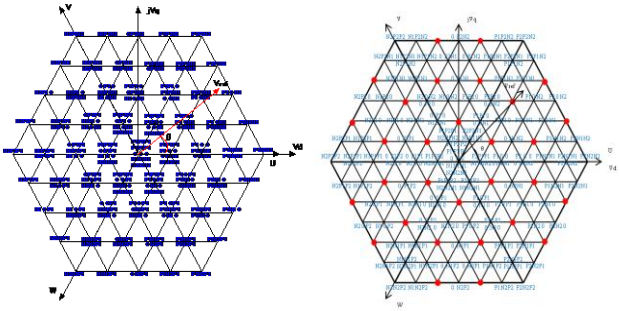


Fig. 4. 1cycle of output line voltage

4. Control method

We proposed that the modulation method of the 5-level inverter is the SVM with changing the ratio of DC link voltage. Fig.5 shows the space vector of the 5-level inverter. Conventional method (DC link voltage as 1:1:1:1) has 61 switching modes, on the other hand proposed method(DC link voltage as 1:2:2:1) has 97 switching modes. Proposed method has more switching modes and resolve density of switching modes overlap at the middle of hexagon. On the proposed method, modulation degree pitch and switching latitude are not concerned. Red point on the Fig.5 (proposed) is impossible output points. So output by half, the two points of point symmetry.



(a) Conventional (b) Proposed

Fig. 5. Space vector of 5-level inverter

5. Simulation result

Table.1 and Table.2 show simulation parameter and control condition. Table.3 shows THD analysis of Vuv. Fundamental frequency of the input and passing band of the band pass filter are 50 [Hz]. For an ac waveform that contains both the fundamental and harmonic components, the total harmonic distortion of the waveform is defined as follow.

$$THD = \frac{\sqrt{V^{*2}_{UV} - V^{2}_{UV}}}{V^{*}_{UV}} \qquad [2]$$

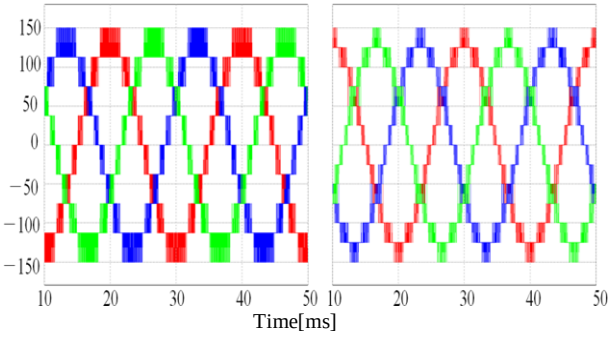
Where, Vuv is the fundamental component and V*uv is overall value of the wave form.

Table 1. Simulation Parameter

DC Link Voltage		Elements parameter	
P2	150[V]	R road	12.5[Ω]
P1	125[V](112.5[V])	L road	73.5[mH]
NPP	75[V]	Capacitor	9900[μF]
N1	25[V](37.5[V])		
N2	0[V]		

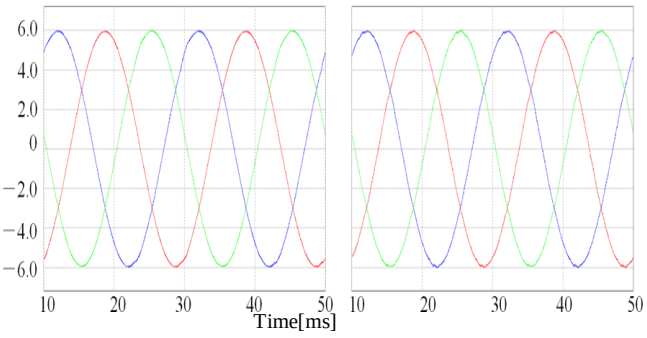
Table.2. Control Condition

Control Method	Carrier Comparison
Carrier Frequency	10[kHz]
Command Frequency	50[Hz]
Degree of Modulation	1



(a) conventional (b) proposed

Fig. 6. Output Line Voltage (3 phase)



(a) conventional (b) proposed

Fig. 7. Output Line Current (3 phase)

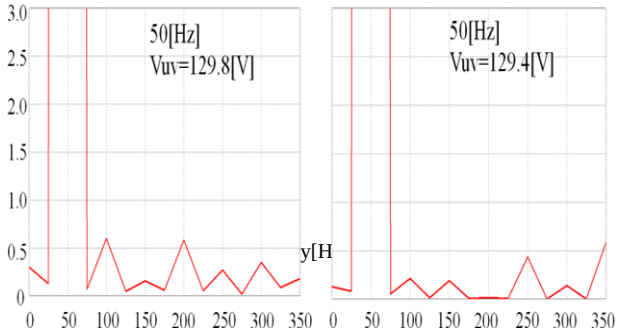


Fig. 8. Output Line Voltage(Vuv) FFT analysis (Comparison of harmonics for fundamental)

6. IGBT off voltage

Fig.8 and Fig.9 shows each IGBT off voltage. DC-link divided 1:2:2:1, each IGBT off-voltages have different values. Specially, S2 and S3 have fluctuated values while these device switched off. To avoid this problem, we proposed IGBT 2-series connection [3]. And by applying this method, it's possible to use same rating IGBT in divided DC link voltage.

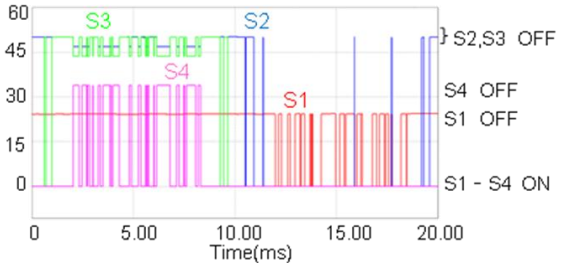


Fig. 9. IGBT off Voltage (conventional)

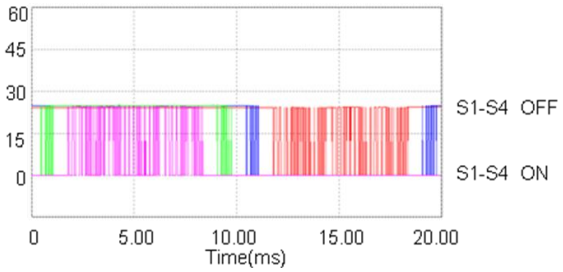
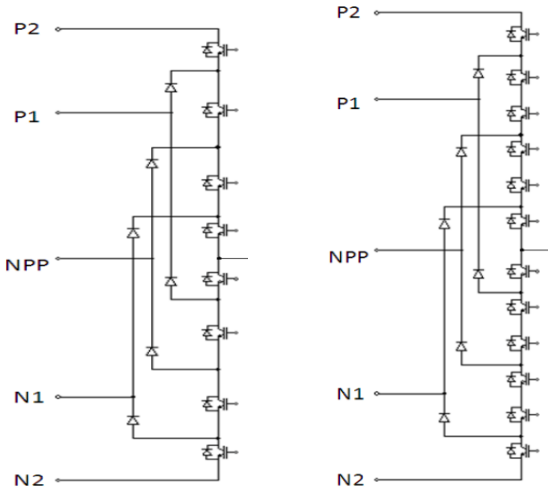


Fig. 10. IGBT off Voltage (2-series connection)

Table. 3. Control Condition

Control Method	Carrier Comparison
Carrier Frequency	10[kHz]
Command Frequency	50[Hz]
Dead Time	4[μs]



(a) Conventional (b) IGBT 2-series connection

Fig. 11. 1-phase circuit

7. Experimental configuration

Figure.11 shows system configuration of 5-level experimental setup. Experimental machine program install to FPGA from PC, then send signals to gate drive circuit. Finally send switching signal to inverters from gate drive circuit. Table.3 and Table.4 show experimental machine parameter and control condition.

Table.4 Experimental Setup Parameter

DC Link Voltage		Elements parameter	
P2	150[V]	R road	12.5[Ω]
P1	125[V](112.5[V])	L road	73.5[mH]
NPP	75[V]	Capacitor	9900[μF]
N1	25[V](37.5[V])		
N2	0[V]	IGBT	600[V]/100[A] (2MBI 100N-060)

Table. 5. Experimental Setup Control Condition

Control Method	Carrier Comparison
Carrier Frequency	10[kHz]
Command Frequency	50[Hz]
Dead Time	4[μs]

As of now, use of space vector modulation, malfunction or delay of the signal wave is a concern. So we applied carrier comparison modulation.

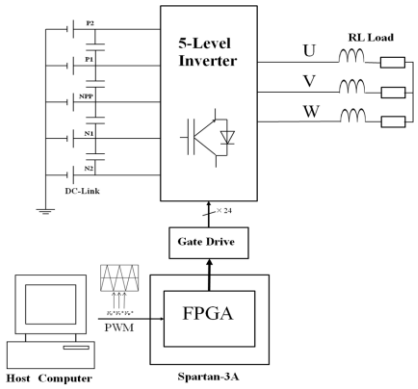


Fig. 12. Experimental Setup System Configuration

Table. 5. Experimental Setup Control Condition

8. Experimental Results

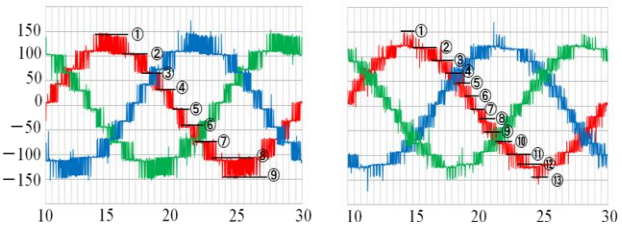
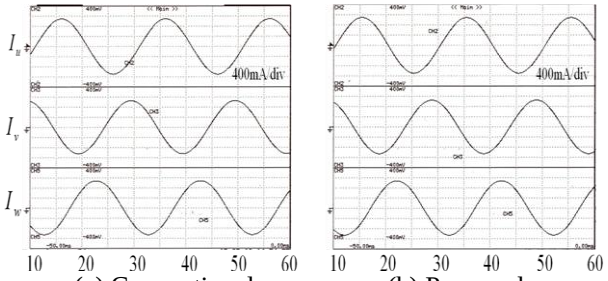
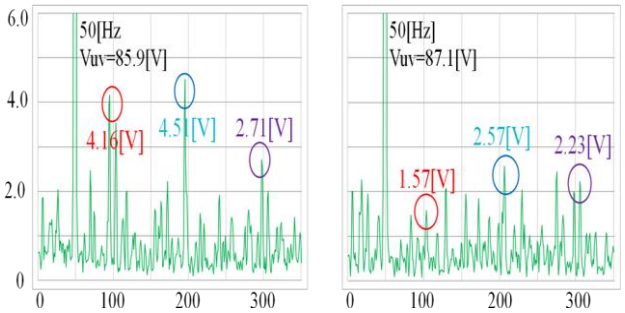


Fig. 13. Output Line Voltage (3phase)



(a) Conventional (b) Proposed

Fig. 14. Output Line Voltage (3phase)



(a) Conventional (b) Proposed

Fig. 15. Output Line Voltage(Vuv) FFT analysis (Comparison of harmonics for fundamental)

Table. 6. THD analysis

Conventional	Proposed
8.55[%]	5.64[%]

Fig.13 shows output line voltages. Proposal result's wave form also approached more sinusoidal forms than conventional. The number of output line levels 9 to 13. Figs.15 shows FFT analysis of line voltages. This result also indicates that the higher harmonics is decreased with output side. Harmonics for fundamental harmonic also reduced on experimental setup. From Fig.6 and Fig13, close to the simulation results were also obtained in actual experiments. On the other hand, since the surge voltage is generated in part, it is necessary to consider the dead time.

9. Conclusion

Dividing DC-link voltages at 1:2:2:1, the higher harmonics was reduced. Then we proved that it is possible to increase the number of voltage levels and the harmonic can be reduced by changing the voltage at the DC link in experimental machine. In this experiment, the series connection of IGBT was not carried out. So, the future it is necessary to perform experiments using a series connection IGBT. In addition, since the surge has occurred to switching, we investigate dead time. On the issue of using for large capacity, calculate the capacity of the DC link capacitor,

perform experiments using up to the limit the breakdown voltage of the IGBT. Finally, there is a need to create a program to apply the space vector modulation, then perform the experiment.

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